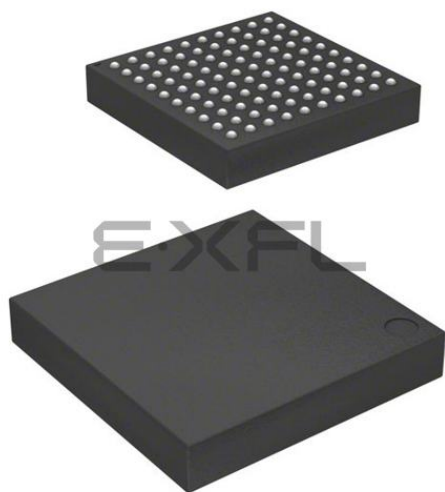




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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565ncddlj-20

Table 1.3 List of Products (3/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N4EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
RX65N (G version)	R5F565NEDGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NEDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565N9AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N9BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N9EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N9FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.5 to Table 1.10 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R		
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15	
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14	
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13	
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12	
11	PD6	PG1	VCC	P61	RX65N Group, RX651 Group PTLG0177KA-A (177-Pin TFLGA) (Upper Perspective View)							P81	P82	PC6	VCC	11	
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10	
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9	
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8	
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7	
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_ USB	USB0_ DP	6	
5	P46	P47	P45	P44	NC								PJ2	P12	VCC_ USB	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4	
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3	
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2	
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R		

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

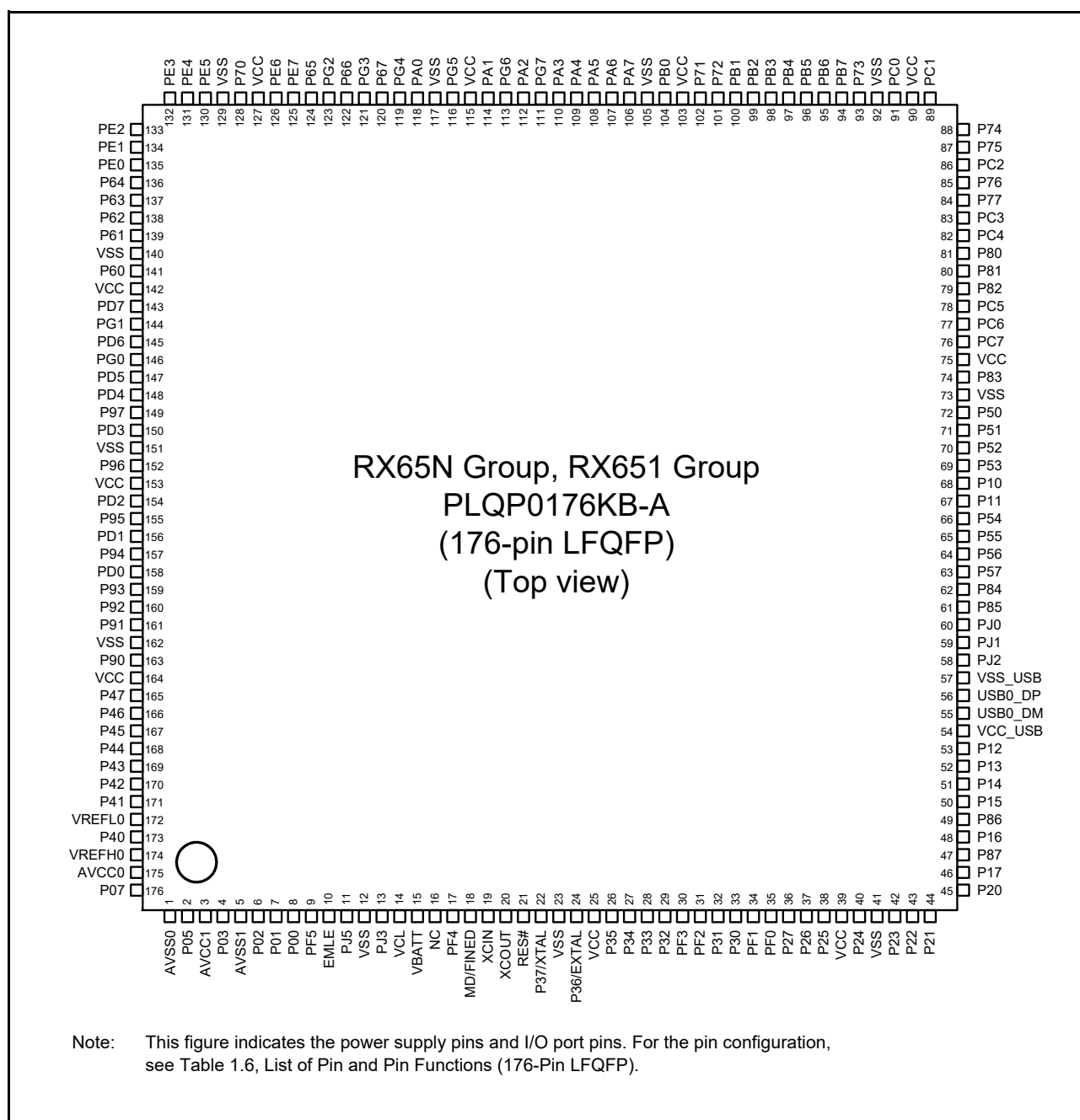
**Figure 1.5 Pin Assignment (176-Pin LFQFP)**

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (2/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
32		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
33		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
34	TCK	PF1			SCK1				
35	TDO	PF0			TXD1/SMOSI1/ SSDA1				
36		P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB- A				
37		P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
38		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD/HSYNC			ADTRG0 #
39	VCC								
40		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP/PIXCLK			
41	VSS								
42		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	SDHI_D1-C/PIXD7			
43		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCUR B	SDHI_D0-C/PIXD6			
44		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN	SDHI_CLK-C/ PIXD5		IRQ9	
45		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID	SDHI_CMD-C/ PIXD4		IRQ8	
46		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS	SDHI_D3-C/PIXD3		IRQ7	ADTRG1 #
47		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10	SDHI_D2-C/PIXD2			
48		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
49		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10	PIXD1			
50		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS	PIXD0		IRQ5	

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (2 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0036h	SYSTM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK		Clock Generation Circuit
0008 0037h	SYSTM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK		Clock Generation Circuit
0008 003Ch	SYSTM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK		Clock Generation Circuit
0008 0040h	SYSTM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK		Clock Generation Circuit
0008 0041h	SYSTM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK		Clock Generation Circuit
0008 00A0h	SYSTM	Operating Power Control Register	OPCCR	8	8	3 ICLK		Low Power Consumption
0008 00A1h	SYSTM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK		Low Power Consumption
0008 00A2h	SYSTM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00A3h	SYSTM	Sub-Clock Oscillator Wait Control Register	SOSCWTCR	8	8	3 ICLK		Clock Generation Circuit
0008 00C0h	SYSTM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets
0008 00C2h	SYSTM	Software Reset Register	SWRR	16	16	3 ICLK		Resets
0008 00E0h	SYSTM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA
0008 00E1h	SYSTM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK		LVDA
0008 00E2h	SYSTM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK		LVDA
0008 00E3h	SYSTM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK		LVDA
0008 03FEh	SYSTM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	2 ICLK		Flash
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	2 ICLK		Flash
0008 101Ch	SYSTM	ROM Wait Cycle Setting Register	ROMWT	8	8	2 ICLK		Clock Generation Circuit
0008 1200h	RAM	RAM Operating Mode Control Register	RAMMODE	8	8	2 ICLK		RAM
0008 1201h	RAM	RAM Error Status Register	RAMSTS	8	8	2 ICLK		RAM
0008 1204h	RAM	RAM Protection Register	RAMPRCR	8	8	2 ICLK		RAM
0008 1208h	RAM	RAM Error Address Capture Register	RAMECAD	32	32	2 ICLK		RAM
0008 1240h	RAM	Expansion RAM Operating Mode Control Register	EXRAMMODE	8	8	2 ICLK		RAM
0008 1241h	RAM	Expansion RAM Error Status Register	EXRAMSTS	8	8	2 ICLK		RAM
0008 1244h	RAM	Expansion RAM Protection Register	EXRAMPRCR	8	8	2 ICLK		RAM

Table 4.1 List of I/O Registers (Address Order) (12 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 79D2h	ICU	Software Configurable Interrupt A Source Select Register 210	SLIAR210	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D3h	ICU	Software Configurable Interrupt A Source Select Register 211	SLIAR211	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D4h	ICU	Software Configurable Interrupt A Source Select Register 212	SLIAR212	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D5h	ICU	Software Configurable Interrupt A Source Select Register 213	SLIAR213	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D6h	ICU	Software Configurable Interrupt A Source Select Register 214	SLIAR214	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D7h	ICU	Software Configurable Interrupt A Source Select Register 215	SLIAR215	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D8h	ICU	Software Configurable Interrupt A Source Select Register 216	SLIAR216	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D9h	ICU	Software Configurable Interrupt A Source Select Register 217	SLIAR217	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DAh	ICU	Software Configurable Interrupt A Source Select Register 218	SLIAR218	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DBh	ICU	Software Configurable Interrupt A Source Select Register 219	SLIAR219	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DCh	ICU	Software Configurable Interrupt A Source Select Register 220	SLIAR220	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DDh	ICU	Software Configurable Interrupt A Source Select Register 221	SLIAR221	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DEh	ICU	Software Configurable Interrupt A Source Select Register 222	SLIAR222	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DFh	ICU	Software Configurable Interrupt A Source Select Register 223	SLIAR223	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E0h	ICU	Software Configurable Interrupt A Source Select Register 224	SLIAR224	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E1h	ICU	Software Configurable Interrupt A Source Select Register 225	SLIAR225	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E2h	ICU	Software Configurable Interrupt A Source Select Register 226	SLIAR226	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E3h	ICU	Software Configurable Interrupt A Source Select Register 227	SLIAR227	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E4h	ICU	Software Configurable Interrupt A Source Select Register 228	SLIAR228	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E5h	ICU	Software Configurable Interrupt A Source Select Register 229	SLIAR229	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E6h	ICU	Software Configurable Interrupt A Source Select Register 230	SLIAR230	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E7h	ICU	Software Configurable Interrupt A Source Select Register 231	SLIAR231	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E8h	ICU	Software Configurable Interrupt A Source Select Register 232	SLIAR232	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E9h	ICU	Software Configurable Interrupt A Source Select Register 233	SLIAR233	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EAh	ICU	Software Configurable Interrupt A Source Select Register 234	SLIAR234	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EBh	ICU	Software Configurable Interrupt A Source Select Register 235	SLIAR235	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79ECh	ICU	Software Configurable Interrupt A Source Select Register 236	SLIAR236	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EDh	ICU	Software Configurable Interrupt A Source Select Register 237	SLIAR237	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EEh	ICU	Software Configurable Interrupt A Source Select Register 238	SLIAR238	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EFh	ICU	Software Configurable Interrupt A Source Select Register 239	SLIAR239	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F0h	ICU	Software Configurable Interrupt A Source Select Register 240	SLIAR240	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (13 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 79F1h	ICU	Software Configurable Interrupt A Source Select Register 241	SLIAR241	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F2h	ICU	Software Configurable Interrupt A Source Select Register 242	SLIAR242	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F3h	ICU	Software Configurable Interrupt A Source Select Register 243	SLIAR243	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F4h	ICU	Software Configurable Interrupt A Source Select Register 244	SLIAR244	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F5h	ICU	Software Configurable Interrupt A Source Select Register 245	SLIAR245	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F6h	ICU	Software Configurable Interrupt A Source Select Register 246	SLIAR246	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F7h	ICU	Software Configurable Interrupt A Source Select Register 247	SLIAR247	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F8h	ICU	Software Configurable Interrupt A Source Select Register 248	SLIAR248	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F9h	ICU	Software Configurable Interrupt A Source Select Register 249	SLIAR249	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FAh	ICU	Software Configurable Interrupt A Source Select Register 250	SLIAR250	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FBh	ICU	Software Configurable Interrupt A Source Select Register 251	SLIAR251	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FCh	ICU	Software Configurable Interrupt A Source Select Register 252	SLIAR252	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FDh	ICU	Software Configurable Interrupt A Source Select Register 253	SLIAR253	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FEh	ICU	Software Configurable Interrupt A Source Select Register 254	SLIAR254	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FFh	ICU	Software Configurable Interrupt A Source Select Register 255	SLIAR255	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7A00h	ICU	Software Configurable Interrupt Source Select Register Write Protect Register	SLIPRCR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 7A01h	ICU	EXDMAC Trigger Select Register	SELEXDR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSMPR	8	8	2, 3 PCLKB	2 ICLK	IWDTa

Table 4.1 List of I/O Registers (Address Order) (20 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9110h	S12AD1	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9112h	S12AD1	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9114h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9116h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9118h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 911Ah	S12AD1	A/D Temperature Sensor Data Register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 911Ch	S12AD1	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 911Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9120h	S12AD1	A/D Data Register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9122h	S12AD1	A/D Data Register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9124h	S12AD1	A/D Data Register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9126h	S12AD1	A/D Data Register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9128h	S12AD1	A/D Data Register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 912Ah	S12AD1	A/D Data Register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 912Ch	S12AD1	A/D Data Register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 912Eh	S12AD1	A/D Data Register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9130h	S12AD1	A/D Data Register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9132h	S12AD1	A/D Data Register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9134h	S12AD1	A/D Data Register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9136h	S12AD1	A/D Data Register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9138h	S12AD1	A/D Data Register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 913Ah	S12AD1	A/D Data Register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 913Ch	S12AD1	A/D Data Register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 913Eh	S12AD1	A/D Data Register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9140h	S12AD1	A/D Data Register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9142h	S12AD1	A/D Data Register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9144h	S12AD1	A/D Data Register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9146h	S12AD1	A/D Data Register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9148h	S12AD1	A/D Data Register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9163h	S12AD1	A/D Conversion Time Setting Protection Release Register	ADSAMPR	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 916Eh	S12AD1	A/D Conversion Time Setting Register	ADSAM	16	16	2, 3 PCLKB	2 ICLK	S12AD Fa

Table 4.1 List of I/O Registers (Address Order) (28 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (41 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B8h	MPC	PF0 Pin Function Control Register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B9h	MPC	PF1 Pin Function Control Register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1BDh	MPC	PF5 Pin Function Control Register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D0h	MPC	PJ0 Pin Function Control Register	PJ0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D1h	MPC	PJ1 Pin Function Control Register	PJ1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D2h	MPC	PJ2 Pin Function Control Register	PJ2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D5h	MPC	PJ5 Pin Function Control Register	PJ5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C280h	SYSTM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption

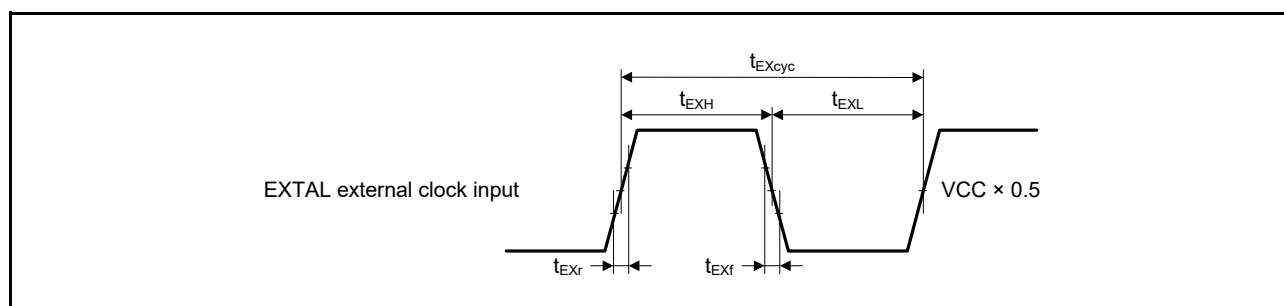
Table 4.1 List of I/O Registers (Address Order) (57 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 011Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0120h	RSPI0	RSPI Data Control Register 2	SPDCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0140h	RSPI1	RSPI Control Register	SPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0141h	RSPI1	RSPI Slave Select Polarity Register	SSLP	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0142h	RSPI1	RSPI Pin Control Register	SPPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0143h	RSPI1	RSPI Status Register	SPSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0144h	RSPI1	RSPI Data Register	SPDR	32	8, 16, 32	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0148h	RSPI1	RSPI Sequence Control Register	SPSCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0149h	RSPI1	RSPI Sequence Status Register	SPSSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Ah	RSPI1	RSPI Bit Rate Register	SPBR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Bh	RSPI1	RSPI Data Control Register	SPDCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Ch	RSPI1	RSPI Clock Delay Register	SPCKD	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Dh	RSPI1	RSPI Slave Select Negation Delay Register	SSLND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Eh	RSPI1	RSPI Next-Access Delay Register	SPND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 014Fh	RSPI1	RSPI Control Register 2	SPCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0150h	RSPI1	RSPI Command Register 0	SPCMD0	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0152h	RSPI1	RSPI Command Register 1	SPCMD1	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0154h	RSPI1	RSPI Command Register 2	SPCMD2	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0156h	RSPI1	RSPI Command Register 3	SPCMD3	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0158h	RSPI1	RSPI Command Register 4	SPCMD4	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 015Ah	RSPI1	RSPI Command Register 5	SPCMD5	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 015Ch	RSPI1	RSPI Command Register 6	SPCMD6	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 015Eh	RSPI1	RSPI Command Register 7	SPCMD7	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0160h	RSPI1	RSPI Data Control Register 2	SPDCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0300h	RSPI2	RSPI Control Register	SPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0301h	RSPI2	RSPI Slave Select Polarity Register	SSLP	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0302h	RSPI2	RSPI Pin Control Register	SPPCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0303h	RSPI2	RSPI Status Register	SPSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0304h	RSPI2	RSPI Data Register	SPDR	32	8, 16, 32	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0308h	RSPI2	RSPI Sequence Control Register	SPSCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0309h	RSPI2	RSPI Sequence Status Register	SPSSR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Ah	RSPI2	RSPI Bit Rate Register	SPBR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Bh	RSPI2	RSPI Data Control Register	SPDCR	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Ch	RSPI2	RSPI Clock Delay Register	SPCKD	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Dh	RSPI2	RSPI Slave Select Negation Delay Register	SSLND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Eh	RSPI2	RSPI Next-Access Delay Register	SPND	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 030Fh	RSPI2	RSPI Control Register 2	SPCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0310h	RSPI2	RSPI Command Register 0	SPCMD0	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0312h	RSPI2	RSPI Command Register 1	SPCMD1	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0314h	RSPI2	RSPI Command Register 2	SPCMD2	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0316h	RSPI2	RSPI Command Register 3	SPCMD3	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0318h	RSPI2	RSPI Command Register 4	SPCMD4	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 031Ah	RSPI2	RSPI Command Register 5	SPCMD5	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 031Ch	RSPI2	RSPI Command Register 6	SPCMD6	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 031Eh	RSPI2	RSPI Command Register 7	SPCMD7	16	16	3, 4 PCLKA	1, 2 ICLK	RSPIc
000D 0320h	RSPI2	RSPI Data Control Register 2	SPDCR2	8	8	3, 4 PCLKA	1, 2 ICLK	RSPIc
000E 0000h to 000E 03FCh	GLCDC	Graphic 1 Color Look-up Table 0[0 to 255]	GR1CLUT0[0 to 255]	32	32	5, 6 PCLKA*7	1, 2 ICLK*7	GLCDC

Table 5.15 EXTAL Clock Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

**Figure 5.4 EXTAL External Clock Input Timing****Table 5.16 Main Clock Timing**

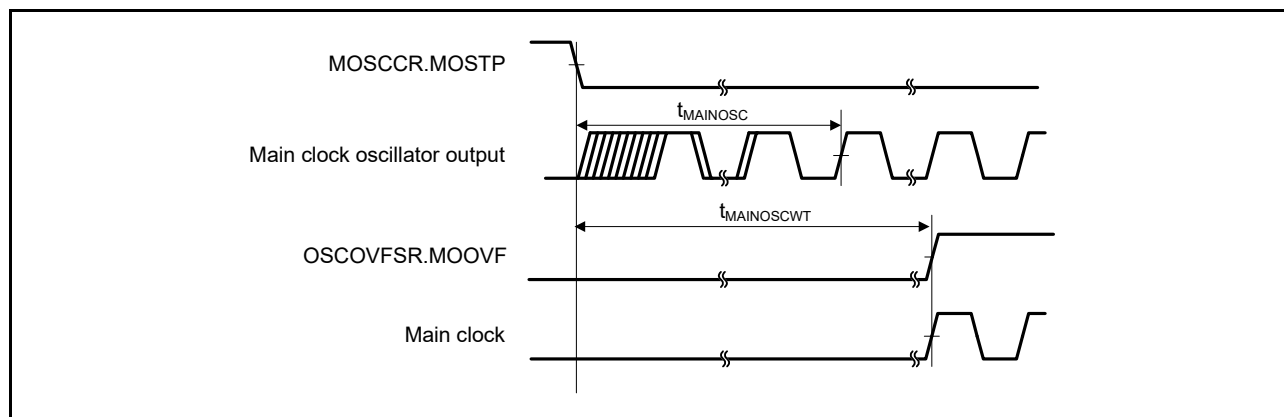
Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	Figure 5.5
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCW}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

$$t_{MAINOSCW} = [(MSTS[7:0] \text{ bits} \times 32) + 10] / f_{LOCO}$$

**Figure 5.5 Main Clock Oscillation Start Timing**

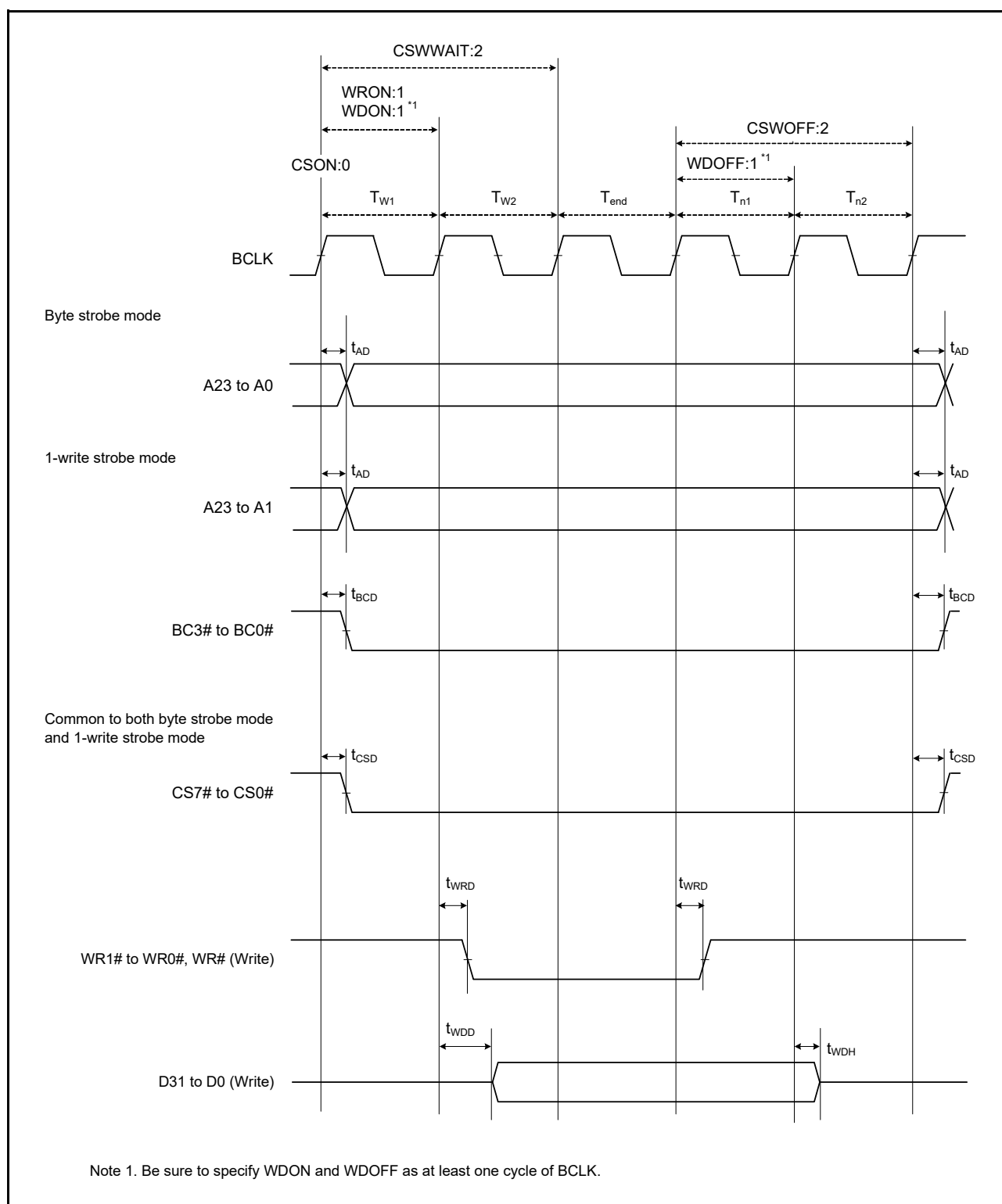


Figure 5.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

Table 5.30 MTU3 Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 5.38
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH} , t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 5.39
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc} : PCLKA cycle

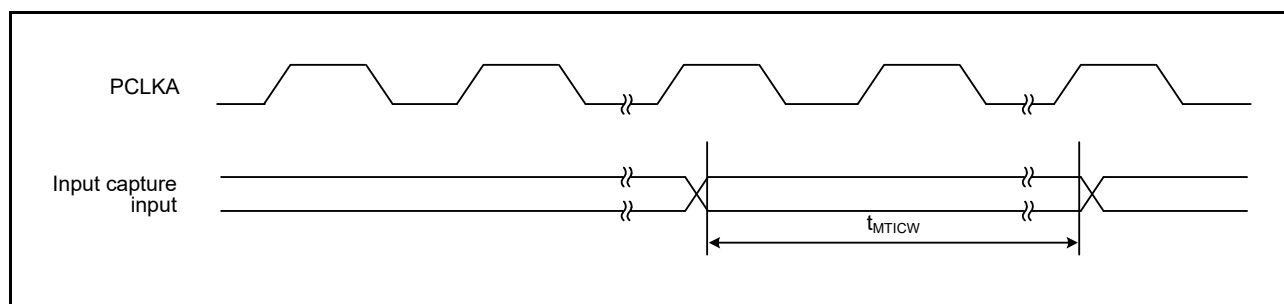
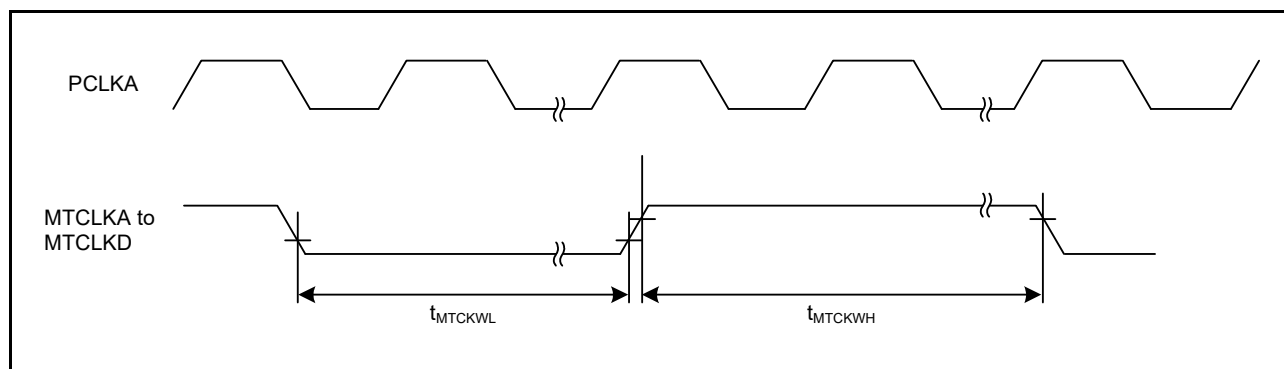
**Figure 5.38 MTU3 Input Capture Input Timing****Figure 5.39 MTU3 Clock Input Timing**

Table 5.31 POE3 Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
POE	POE# input pulse width	t_{POEW}	1.5	—	t_{PBcyc}	Figure 5.40

Note 1. t_{PBcyc} : PCLKB cycle

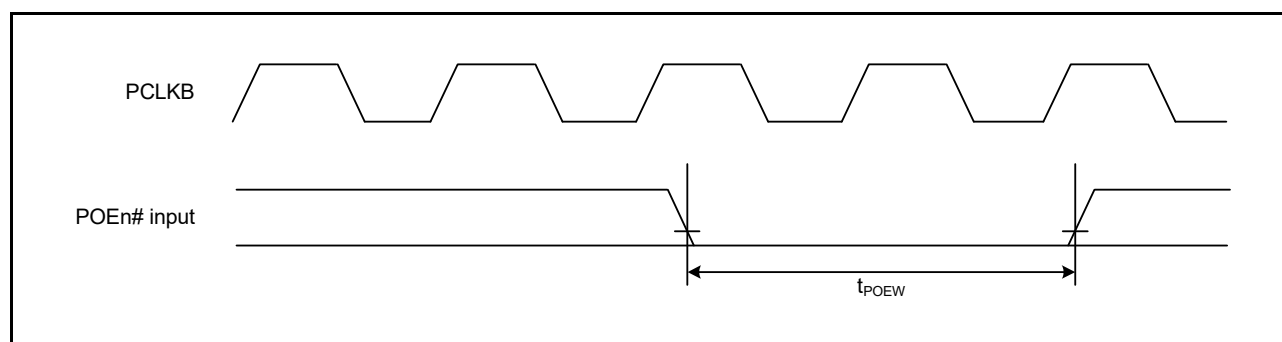
**Figure 5.40 POE# Input Timing**

Table 5.39 RIIC Timing (2)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.54
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 20$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle, t_{PBcyc} : PCLKB cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

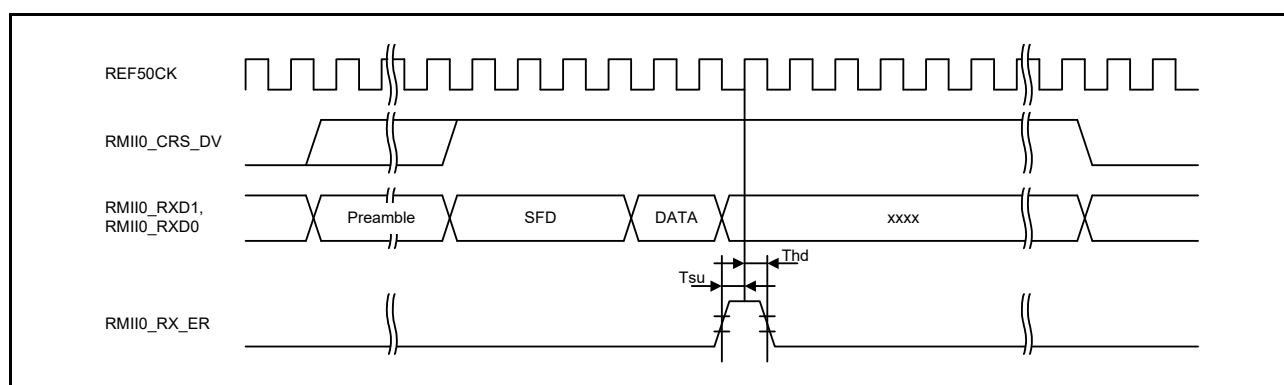


Figure 5.59 RMII Reception Timing (Error Occurrence)

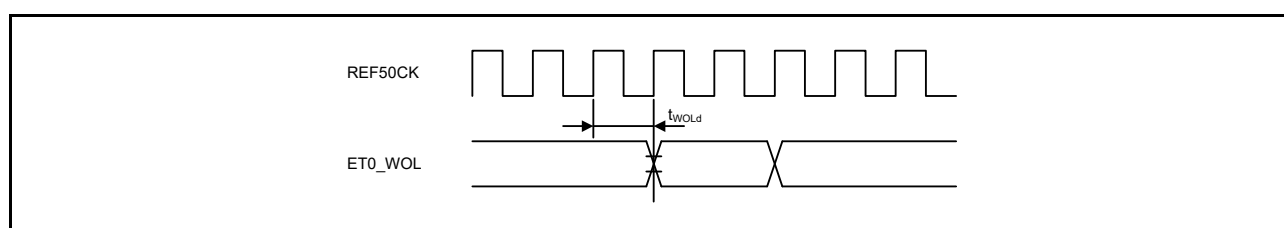


Figure 5.60 WOL Output Timing (RMII)

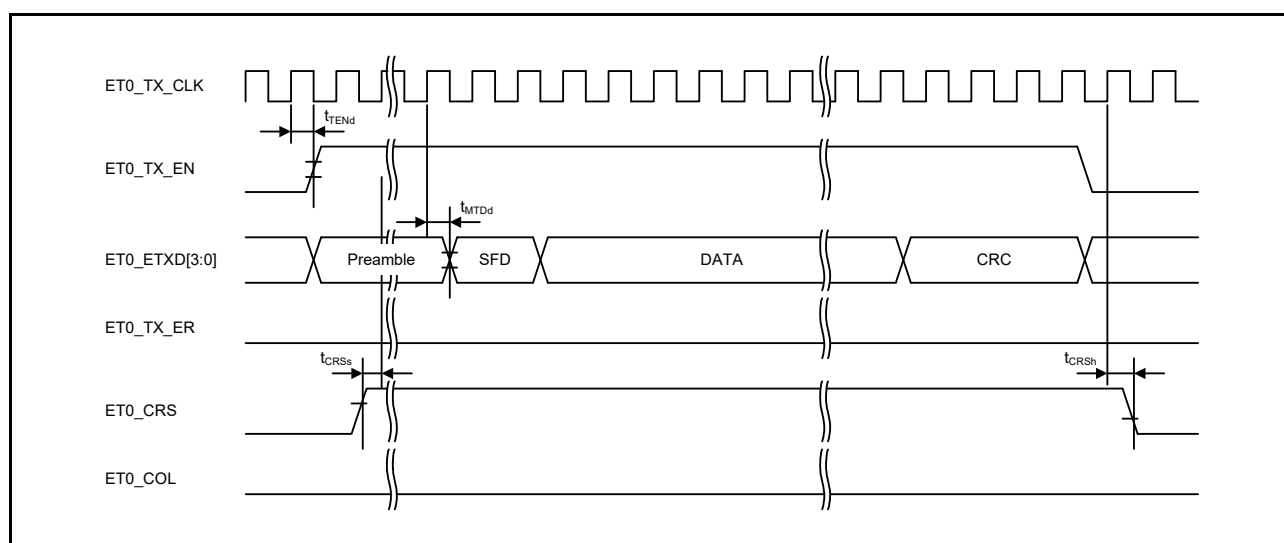


Figure 5.61 MII Transmission Timing (Normal Operation)

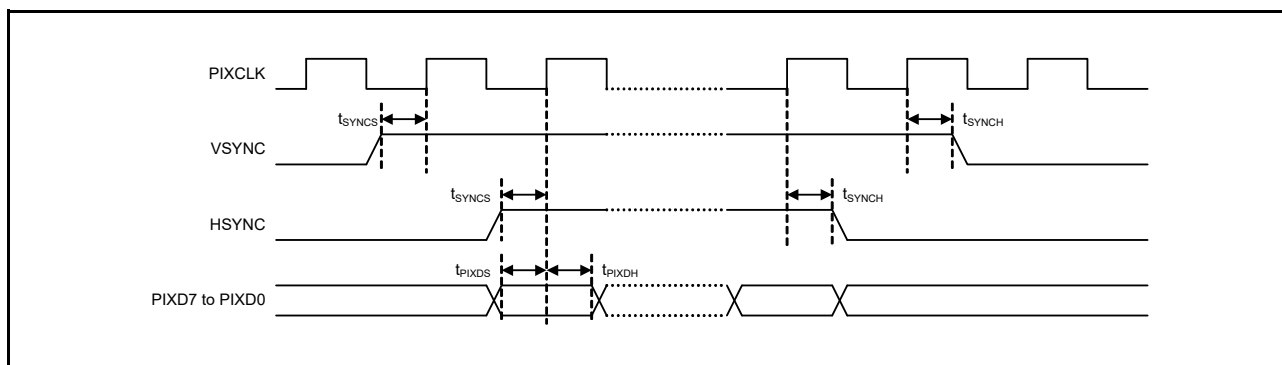


Figure 5.68 PDC AC Timing

Table 5.43 GLCDC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD_EXTCLK Input clock frequency	$t_{E_{cyc}}$	—	—	30*1	MHz	Figure 5.69
LCD_EXTCLK Input clock Low pulse width	t_{WL}	0.45	—	0.55	$t_{E_{cyc}}$	
LCD_EXTCLK Input clock High pulse width	t_{WH}	0.45	—	0.55	$t_{E_{cyc}}$	
LCD_CLK Output clock frequency	$t_{L_{cyc}}$	—	—	30*1	MHz	Figure 5.70
LCD_CLK Output clock Low pulse width	t_{LOL}	0.4	—	0.6	$t_{L_{cyc}}$	
LCD_CLK Output clock High pulse width	t_{LOH}	0.4	—	0.6	$t_{L_{cyc}}$	
LCD data output Delay timing	t_{DD}	-3.5^*2	—	4^*2	ns	Figure 5.71

Note 1. Parallel RGB888,666,565: Max. 27 MHz
 Serial RGB888: Max. 30 MHz (4x speed)

Note 2. We recommend using pins that have a letter ("A", "B", etc) to indicate group membership appended to their names as groups.
 For the GLCDC interface, the AC portion of the electrical characteristics is measured for each group.
 If we use group "A" and "B" combination, "LCD data output Delay timing (t_{DD})" is Min = -5.0 ns, Max = 5.5 ns.

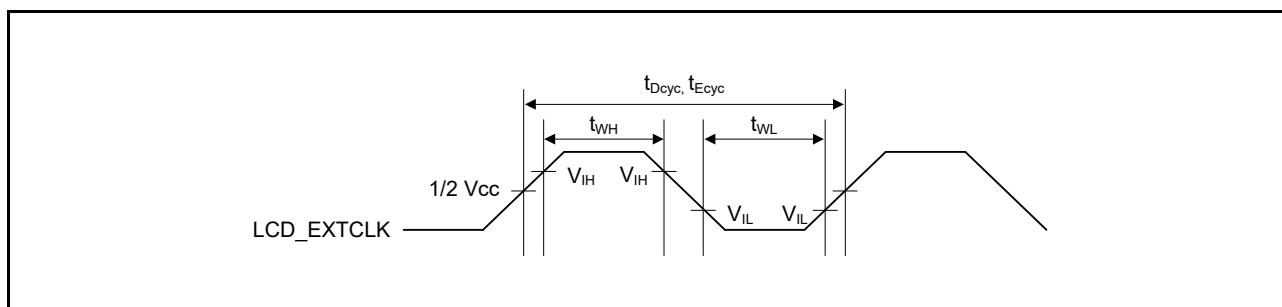


Figure 5.69 LCD_EXTCLK Clock Input Timing

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.51 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

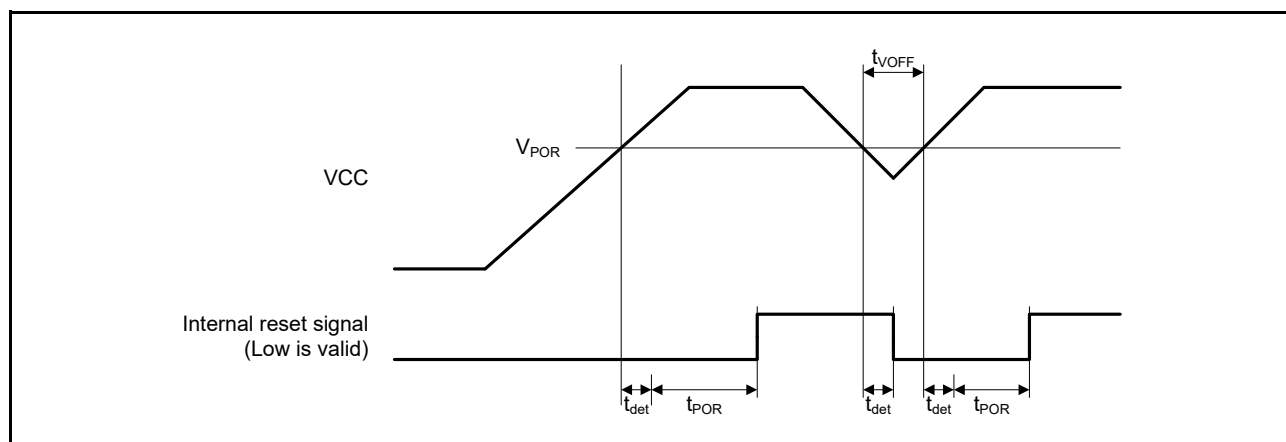
Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V _{POR}	2.5	2.6	2.7	V	Figure 5.76
		Low power consumption function enabled*2		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V _{det0_1}	2.84	2.94	3.04		Figure 5.77
			V _{det0_2}	2.77	2.87	2.97		
			V _{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V _{det1_1}	2.89	2.99	3.09		Figure 5.78
			V _{det1_2}	2.82	2.92	3.02		
			V _{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V _{det2_1}	2.89	2.99	3.09		Figure 5.79
			V _{det2_2}	2.82	2.92	3.02		
			V _{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t _{POR}	—	4.6	—	ms	Figure 5.76
	LVD0 reset time		t _{LVD0}	—	0.70	—		Figure 5.77
	LVD1 reset time		t _{LVD1}	—	0.57	—		Figure 5.78
	LVD2 reset time		t _{LVD2}	—	0.57	—		Figure 5.79
Minimum VCC down time			t _{VOFF}	200	—	—	μs	Figure 5.76, Figure 5.77
Response delay time			t _{det}	—	—	200	μs	Figure 5.76 to Figure 5.79
LVD operation stabilization time (after LVD is enabled)			T _{d(E-A)}	—	—	10	μs	Figure 5.78, Figure 5.79
Hysteresis width (LVD1 and LVD2)			V _{LVH}	—	70	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

**Figure 5.76 Power-on Reset Timing**