



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565neddfp-30

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565NEDDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDFC	PLQP0176KB-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDFC	PLQP0176KB-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NEDDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDFB	PLQP0144KA-B	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDFP	PLQP0100KB-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDFP	PLQP0100KB-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDFP	PLQP0100KB-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85

Table 1.3 List of Products (3/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N4EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565NEDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NEHDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565NCDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F565NCHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F565N9ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N9BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N9EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N9FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N7ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N7BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N7EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N7FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F565N4ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F565N4BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F565N4EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F565N4FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
RX65N (G version)	R5F565NEDGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NEDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NEHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565NCDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F565NCHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F565N9AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F565N9BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F565N9EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F565N9FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105

Table 1.3 List of Products (7/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX651 (D version)	R5F5651EDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651EHDJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F5651CDDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +85
	R5F5651CHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +85
	R5F56519ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56519BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56519EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56519FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56517ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56517BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56517EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56517FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
	R5F56514ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +85
	R5F56514BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +85
	R5F56514EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +85
	R5F56514FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +85
RX651 (G version)	R5F5651EDGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651EHGFC	PLQP0176KB-A*1	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651CDGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651CHGFC	PLQP0176KB-A*1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651EDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651EHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F5651CDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	−40 to +105
	R5F5651CHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	−40 to +105
	R5F56519AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F56519BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105
	R5F56519EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	−40 to +105
	R5F56519FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	−40 to +105
	R5F56517AGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	−40 to +105
	R5F56517BGFB	PLQP0144KA-B	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	−40 to +105

1.3 Block Diagram

Figure 1.2 shows a block diagram.

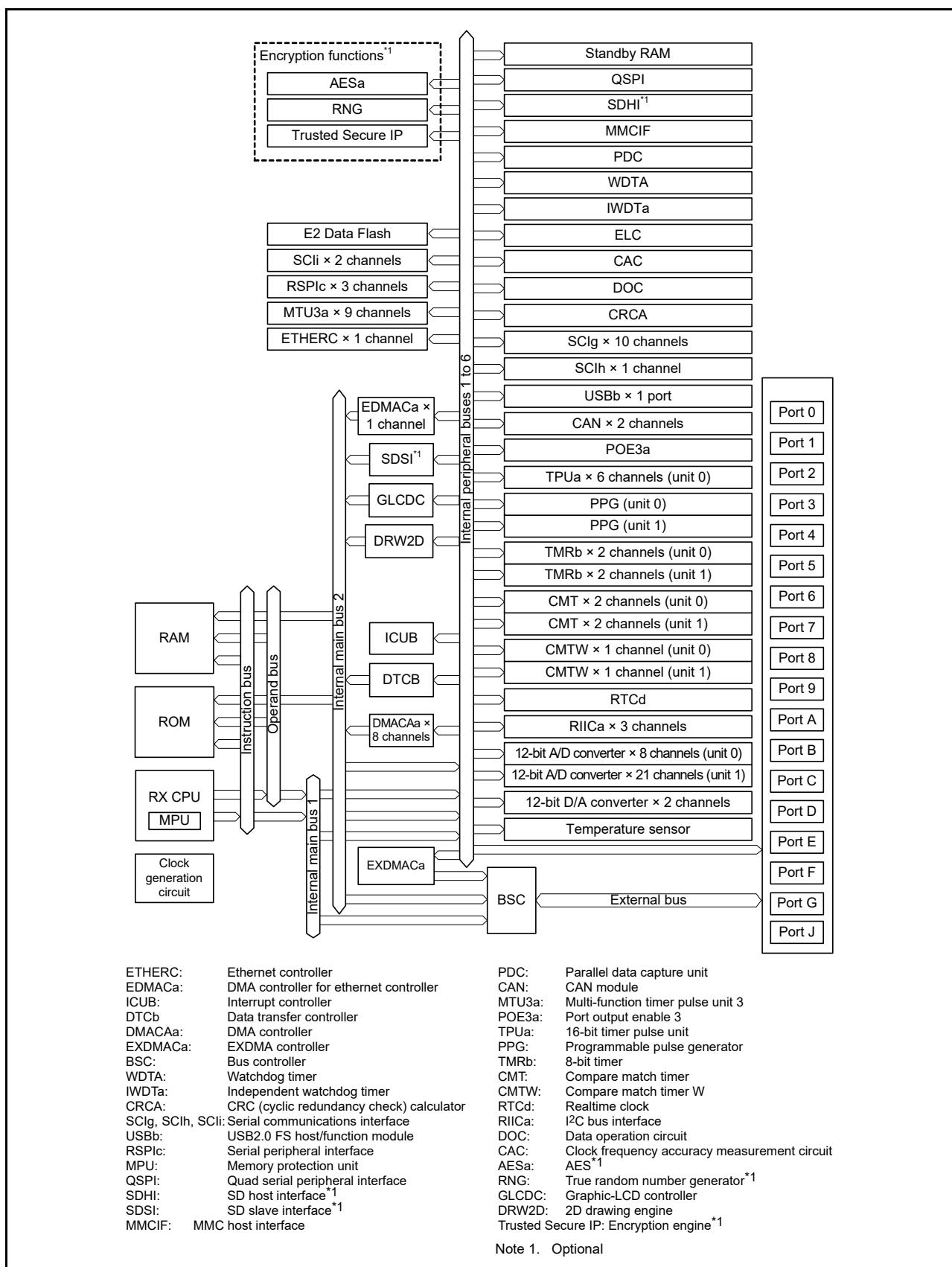


Figure 1.2 Block Diagram

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strobe signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU in the high impedance state

RX65N Group, RX651 Group
PTLG0100JA-A (100-Pin TFLGA)
(Upper Perspective View)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	AVCC1	AVSS0	AVSS1	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (100-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
H1	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
H2		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3				ADTRG0 #
H3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOU	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCUR B			IRQ6	ADTRG0 #
H4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMC12/ PO13	RXD1/SMISO1/ SSCL1/SCK3/ CRX1-DS			IRQ5	
H5		P55	D0[A0/D0]*1/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ CRX1			IRQ10	
H6		P54	ALE/D1[A1/ D1]*1/ EDACK0	MTIOC4B/ TMC11	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/CTX1				
H7	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF	ET0_COL/TXD8/ SMOSI8/SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A			IRQ14	
H8		PC6	D2[A2/D2]*1/ A22/CS1#	MTIOC3C/ MTCLKA/ TMC12/PO30/ TIC0	ET0_ETXD3/ RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A			IRQ13	
H9		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
H10		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMISO9/ SSDA9/ SMISO11/ SSDA11/TXD11	SDSI_D1-B			
J1		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN				
J2		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/SCL1*1/ USB0_EXICEN			IRQ9	
J3		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS			IRQ7	ADTRG1 #
J4		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]			IRQ3	ADTRG1 #
J5	VSS_USB								

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (1/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
1	AVCC1								
2	EMLE								
3	AVSS1								
4		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
5	VCL								
6	VBATT								
7	MD/FINED								
8	XCIN								
9	XCOUT								
10	RES#								
11	XTAL	P37							
12	VSS								
13	EXTAL	P36							
14	VCC								
15	UPSEL	P35						NMI	
16	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
17		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0			IRQ3-DS	
18		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN			IRQ2-DS	
19	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
20	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
21	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A				
22	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
23		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3				ADTRG0 #
24		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN				
25		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#				

Table 4.1 List of I/O Registers (Address Order) (7 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 3852h	BSC	CS5 Control Register	CS5CR	16	16	1, 2 BCLK		Buses
0008 385Ah	BSC	CS5 Recovery Cycle Register	CS5REC	16	16	1, 2 BCLK		Buses
0008 3862h	BSC	CS6 Control Register	CS6CR	16	16	1, 2 BCLK		Buses
0008 386Ah	BSC	CS6 Recovery Cycle Register	CS6REC	16	16	1, 2 BCLK		Buses
0008 3872h	BSC	CS7 Control Register	CS7CR	16	16	1, 2 BCLK		Buses
0008 387Ah	BSC	CS7 Recovery Cycle Register	CS7REC	16	16	1, 2 BCLK		Buses
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK		Buses
0008 3C00h	BSC	SDC Control Register	SDCCR	8	8	1, 2 BCLK		Buses
0008 3C01h	BSC	SDC Mode Register	SDCMOD	8	8	1, 2 BCLK		Buses
0008 3C02h	BSC	SDRAM Access Mode Register	SDAMOD	8	8	1, 2 BCLK		Buses
0008 3C10h	BSC	SDRAM Self-Refresh Control Register	SDSELF	8	8	1, 2 BCLK		Buses
0008 3C14h	BSC	SDRAM Refresh Control Register	SDRFCR	16	16	1, 2 BCLK		Buses
0008 3C16h	BSC	SDRAM Auto-Refresh Control Register	SDRFEN	8	8	1, 2 BCLK		Buses
0008 3C20h	BSC	SDRAM Initialization Sequence Control Register	SDICR	8	8	1, 2 BCLK		Buses
0008 3C24h	BSC	SDRAM Initialization Register	SDIR	16	16	1, 2 BCLK		Buses
0008 3C40h	BSC	SDRAM Address Register	SDADR	8	8	1, 2 BCLK		Buses
0008 3C44h	BSC	SDRAM Timing Register	SDTR	32	32	1, 2 BCLK		Buses
0008 3C48h	BSC	SDRAM Mode Register	SDMOD	16	16	1, 2 BCLK		Buses
0008 3C50h	BSC	SDRAM Status Register	SDSR	8	8	1, 2 BCLK		Buses
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK		MPU
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK		MPU
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK		MPU
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK		MPU
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK		MPU
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK		MPU
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK		MPU
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK		MPU
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK		MPU
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK		MPU
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK		MPU
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK		MPU
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK		MPU
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK		MPU
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK		MPU
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK		MPU
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK		MPU
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK		MPU
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK		MPU
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK		MPU
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK		MPU
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK		MPU
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK		MPU
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK		MPU
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK		MPU
0008 7010h to 0008 70FFh	ICU	Interrupt Request Registers 016 to 255	IR016 to 255	8	8	2 ICLK		ICUB
0008 711Ah to 0008 71FFh	ICU	DTC Transfer Request Enable Registers 026 to 255	DTCER026 to DTCER255	8	8	2 ICLK		ICUB
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Registers 02 to 1F	IER02 to IER1F	8	8	2 ICLK		ICUB

Table 4.1 List of I/O Registers (Address Order) (12 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 79D2h	ICU	Software Configurable Interrupt A Source Select Register 210	SLIAR210	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D3h	ICU	Software Configurable Interrupt A Source Select Register 211	SLIAR211	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D4h	ICU	Software Configurable Interrupt A Source Select Register 212	SLIAR212	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D5h	ICU	Software Configurable Interrupt A Source Select Register 213	SLIAR213	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D6h	ICU	Software Configurable Interrupt A Source Select Register 214	SLIAR214	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D7h	ICU	Software Configurable Interrupt A Source Select Register 215	SLIAR215	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D8h	ICU	Software Configurable Interrupt A Source Select Register 216	SLIAR216	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79D9h	ICU	Software Configurable Interrupt A Source Select Register 217	SLIAR217	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DAh	ICU	Software Configurable Interrupt A Source Select Register 218	SLIAR218	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DBh	ICU	Software Configurable Interrupt A Source Select Register 219	SLIAR219	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DCh	ICU	Software Configurable Interrupt A Source Select Register 220	SLIAR220	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DDh	ICU	Software Configurable Interrupt A Source Select Register 221	SLIAR221	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DEh	ICU	Software Configurable Interrupt A Source Select Register 222	SLIAR222	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79DFh	ICU	Software Configurable Interrupt A Source Select Register 223	SLIAR223	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E0h	ICU	Software Configurable Interrupt A Source Select Register 224	SLIAR224	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E1h	ICU	Software Configurable Interrupt A Source Select Register 225	SLIAR225	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E2h	ICU	Software Configurable Interrupt A Source Select Register 226	SLIAR226	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E3h	ICU	Software Configurable Interrupt A Source Select Register 227	SLIAR227	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E4h	ICU	Software Configurable Interrupt A Source Select Register 228	SLIAR228	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E5h	ICU	Software Configurable Interrupt A Source Select Register 229	SLIAR229	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E6h	ICU	Software Configurable Interrupt A Source Select Register 230	SLIAR230	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E7h	ICU	Software Configurable Interrupt A Source Select Register 231	SLIAR231	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E8h	ICU	Software Configurable Interrupt A Source Select Register 232	SLIAR232	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79E9h	ICU	Software Configurable Interrupt A Source Select Register 233	SLIAR233	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EAh	ICU	Software Configurable Interrupt A Source Select Register 234	SLIAR234	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EBh	ICU	Software Configurable Interrupt A Source Select Register 235	SLIAR235	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79ECh	ICU	Software Configurable Interrupt A Source Select Register 236	SLIAR236	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EDh	ICU	Software Configurable Interrupt A Source Select Register 237	SLIAR237	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EEh	ICU	Software Configurable Interrupt A Source Select Register 238	SLIAR238	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79EFh	ICU	Software Configurable Interrupt A Source Select Register 239	SLIAR239	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F0h	ICU	Software Configurable Interrupt A Source Select Register 240	SLIAR240	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB

Table 4.1 List of I/O Registers (Address Order) (17 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8320h	RIIC1	I ² C-bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8321h	RIIC1	I ² C-bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8322h	RIIC1	I ² C-bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8323h	RIIC1	I ² C-bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8324h	RIIC1	I ² C-bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8325h	RIIC1	I ² C-bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8326h	RIIC1	I ² C-bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8327h	RIIC1	I ² C-bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8328h	RIIC1	I ² C-bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8329h	RIIC1	I ² C-bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8330h	RIIC1	I ² C-bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8331h	RIIC1	I ² C-bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8332h	RIIC1	I ² C-bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8333h	RIIC1	I ² C-bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8340h	RIIC2	I ² C-bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8341h	RIIC2	I ² C-bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8342h	RIIC2	I ² C-bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8343h	RIIC2	I ² C-bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8344h	RIIC2	I ² C-bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8345h	RIIC2	I ² C-bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8346h	RIIC2	I ² C-bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8347h	RIIC2	I ² C-bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8348h	RIIC2	I ² C-bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8349h	RIIC2	I ² C-bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ah	RIIC2	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Bh	RIIC2	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ch	RIIC2	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Dh	RIIC2	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Eh	RIIC2	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Fh	RIIC2	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8350h	RIIC2	I ² C-bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8351h	RIIC2	I ² C-bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8352h	RIIC2	I ² C-bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8353h	RIIC2	I ² C-bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8500h	MMCIF	Command Setting Register	CECMDSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8508h	MMCIF	Argument Register	CEARG	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 850Ch	MMCIF	Automatically Issued CMD12 Argument Register	CEARGCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8510h	MMCIF	Command Control Register	CECMDCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8514h	MMCIF	Transfer Block Setting Register	CEBLOCKSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8518h	MMCIF	Clock Control Register	CECLKCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 851Ch	MMCIF	Buffer Access Setting Register	CEBUFACC	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8520h	MMCIF	Response Register 3	CERESP3	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8524h	MMCIF	Response Register 2	CERESP2	32	32	2, 3 PCLKB	2 ICLK	MMCIF

Table 4.1 List of I/O Registers (Address Order) (22 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 91E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E4h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E5h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E6h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E7h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E8h	S12AD1	A/D Sampling State Register 8	ADSSTR8	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91E9h	S12AD1	A/D Sampling State Register 9	ADSSTR9	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EAh	S12AD1	A/D Sampling State Register 10	ADSSTR10	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EBh	S12AD1	A/D Sampling State Register 11	ADSSTR11	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91ECh	S12AD1	A/D Sampling State Register 12	ADSSTR12	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EDh	S12AD1	A/D Sampling State Register 13	ADSSTR13	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EEh	S12AD1	A/D Sampling State Register 14	ADSSTR14	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 91EFh	S12AD1	A/D Sampling State Register 15	ADSSTR15	8	8	2, 3 PCLKB	2 ICLK	S12AD Fa
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Set Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E24h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 2	SPBMUL2	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E28h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 3	SPBMUL3	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 A000h	SCIO	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, SCli
0008 A001h	SCIO	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (28 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0C9h	SCI6	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CAh	SCI6	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CBh	SCI6	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CCh	SCI6	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SClh, SCli

Table 4.1 List of I/O Registers (Address Order) (30 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0EEh	SCI7	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0F0h	SCI7	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0F1h	SCI7	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0F0h	SCI7	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A0F2h	SCI7	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A106h	SMCI8	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A109h	SCI8	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A10Ah	SCI8	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A10Bh	SCI8	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A10Ch	SCI8	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h, SC1i
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h, SC1i

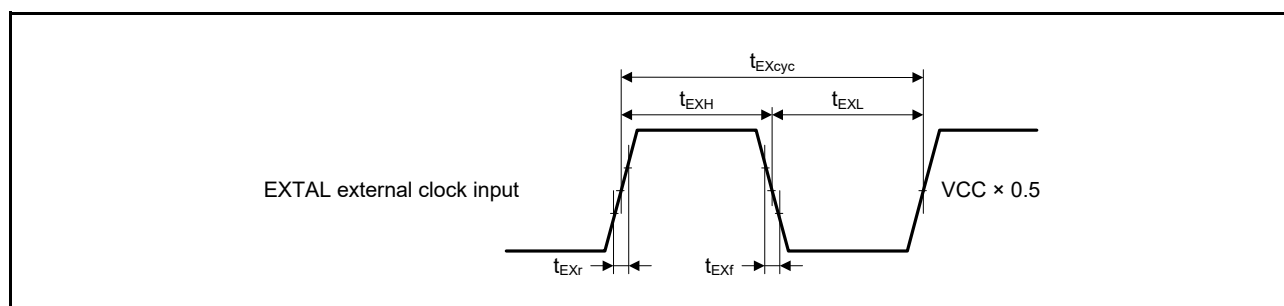
Table 4.1 List of I/O Registers (Address Order) (42 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C283h	SYSTEM	Deep Standby Interrupt Enable Register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C285h	SYSTEM	Deep Standby Interrupt Enable Register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C287h	SYSTEM	Deep Standby Interrupt Flag Register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C289h	SYSTEM	Deep Standby Interrupt Flag Register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Bh	SYSTEM	Deep Standby Interrupt Edge Register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Dh	SYSTEM	Deep Standby Interrupt Edge Register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-Speed On-Chip Oscillator Power Supply Control Register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C296h	FLASH	Flash P/E Protect Register	FWEPROR	8	8	2 ICLK		Flash
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA

Table 5.15 EXTAL Clock Timing

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

**Figure 5.4 EXTAL External Clock Input Timing****Table 5.16 Main Clock Timing**

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	Figure 5.5
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCW}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

$$t_{MAINOSCW} = [(MSTS[7:0] \text{ bits} \times 32) + 10] / f_{LOCO}$$

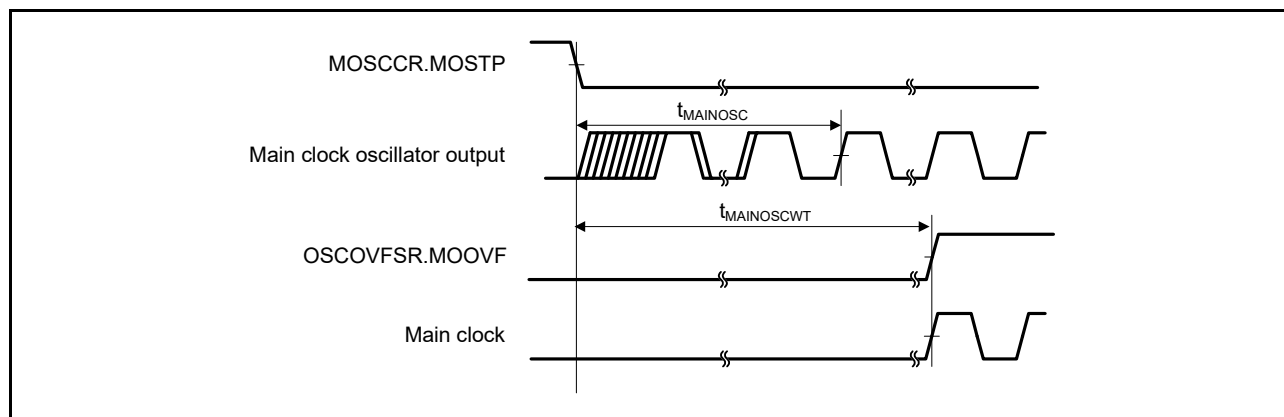
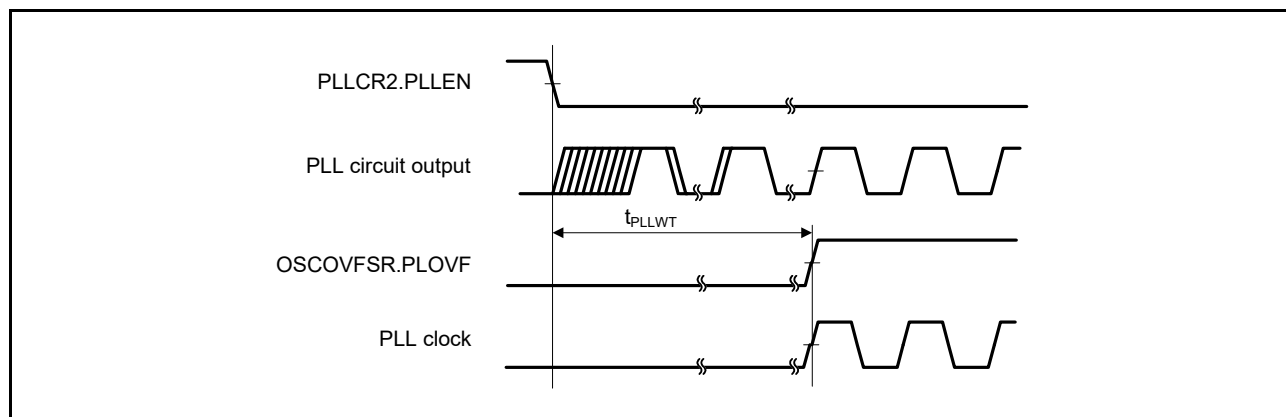
**Figure 5.5 Main Clock Oscillation Start Timing**

Table 5.19 PLL Clock Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	μ s	Figure 5.10

**Figure 5.10 PLL Clock Oscillation Start Timing****Table 5.20 Sub-Clock Timing**

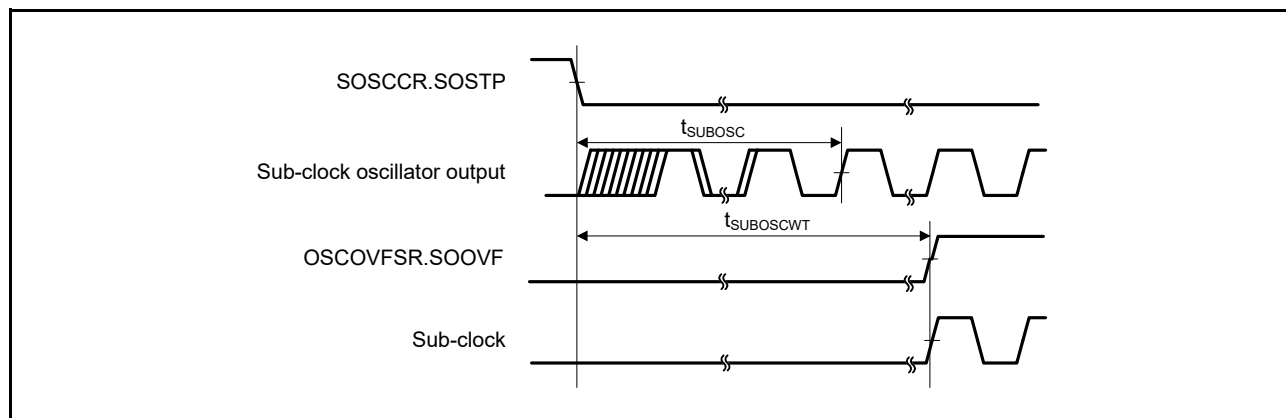
Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $V_{BATT} = 2.0$ to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 5.11
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the $SOSWTCR.SSTS[7:0]$ bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.

$$t_{SUBOSCWT} = [(SSTS[7:0] \text{ bits} \times 16384) + 10] / f_{Loco}$$

**Figure 5.11 Sub-Clock Oscillation Start Timing**

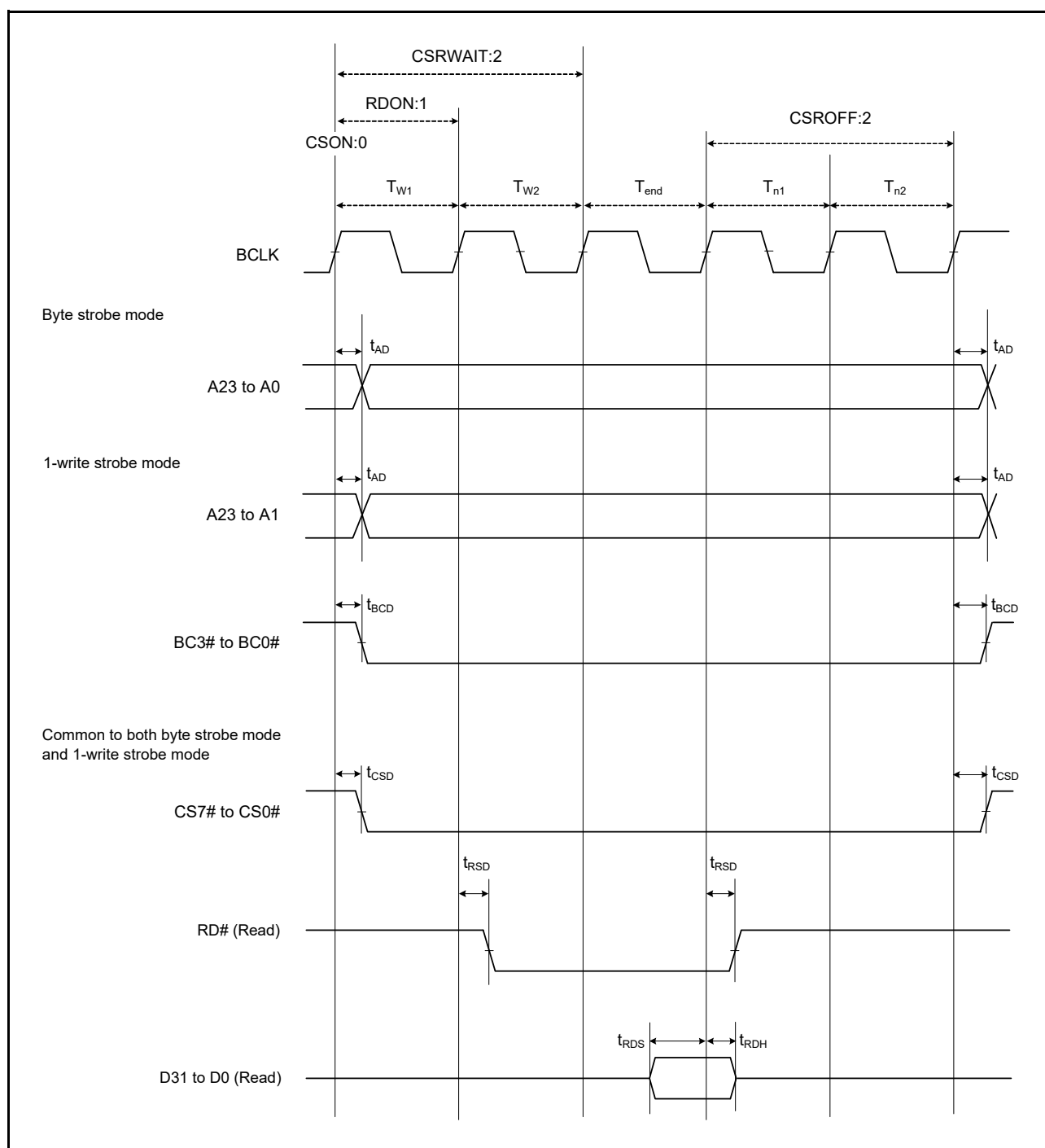


Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

Table 5.36 Simple SPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions	
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{PAcyc}	Figure 5.44	
	SCK clock cycle input (slave)		8	65536			
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}		
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}		
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns		
	Data input setup time	t_{SU}	33.3	—	ns	Figure 5.45 to Figure 5.50	
	Data input hold time	t_H	33.3	—	ns		
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}		
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}		
	Data output delay time	t_{OD}	—	33.3	ns		
	Data output hold time	t_{OH}	−10	—	ns		
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns		
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns		
	Slave access time	t_{SA}	—	5	t_{PBcyc}		Figure 5.49, Figure 5.50
	Slave output release time	t_{REL}	—	5	t_{PBcyc}		

Note 1. t_{PACVC} : PCLKA cycle, t_{PBCVC} : PCLKB cycle

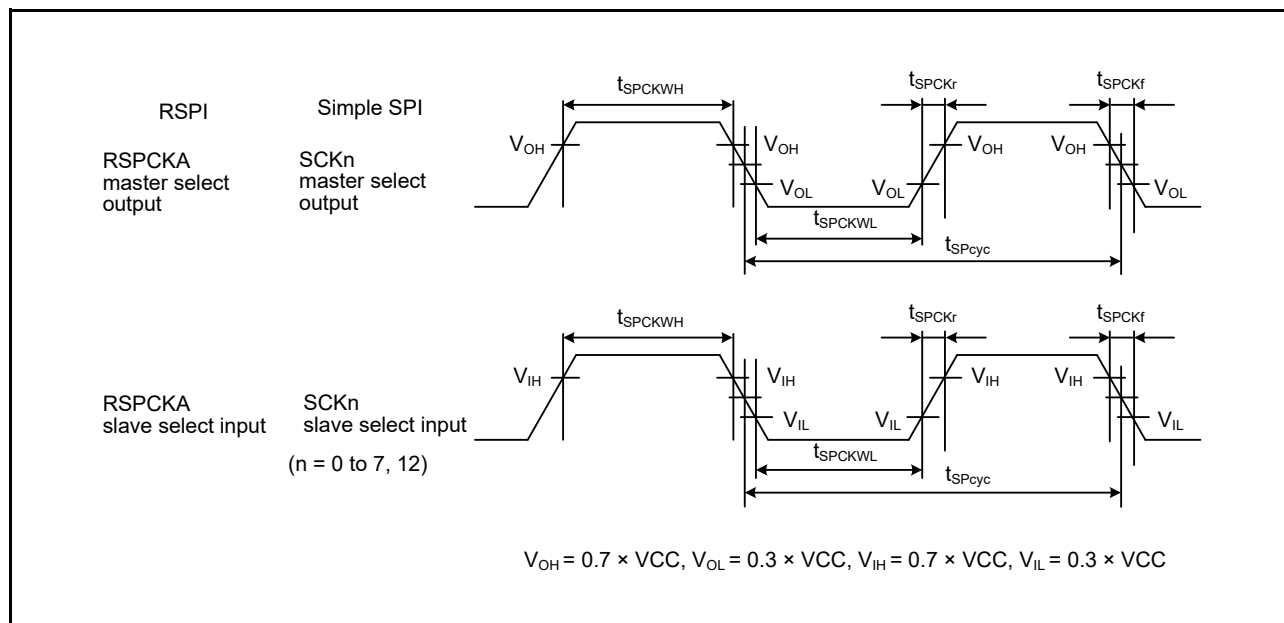


Figure 5.44 RSPI Clock Timing and Simple SPI Clock Timing

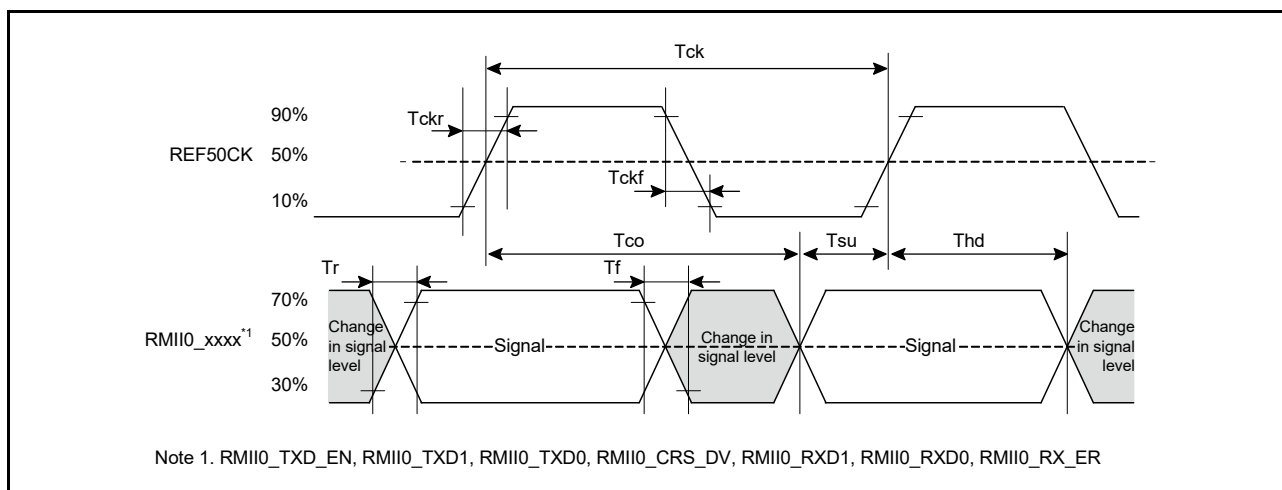


Figure 5.56 Timing with the REF50CK and RMII Signals

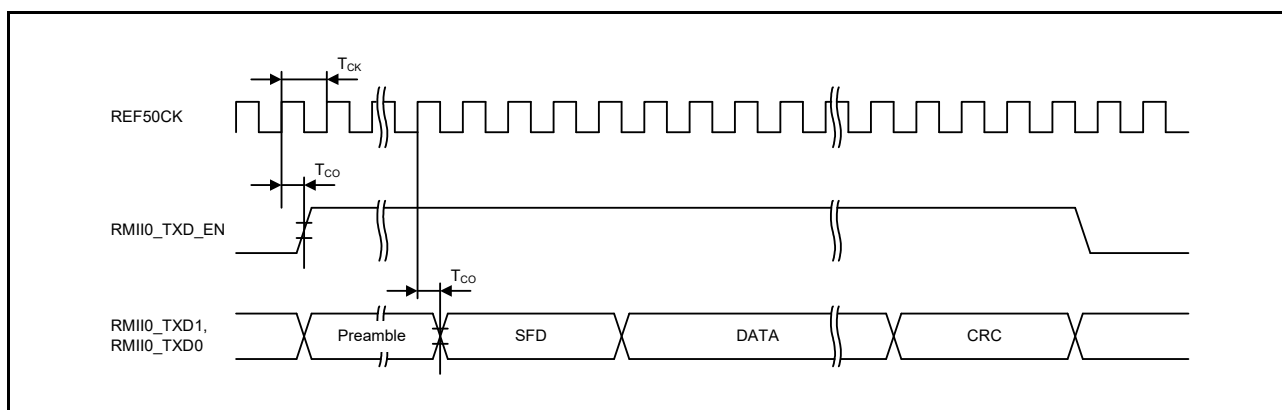


Figure 5.57 RMII Transmission Timing

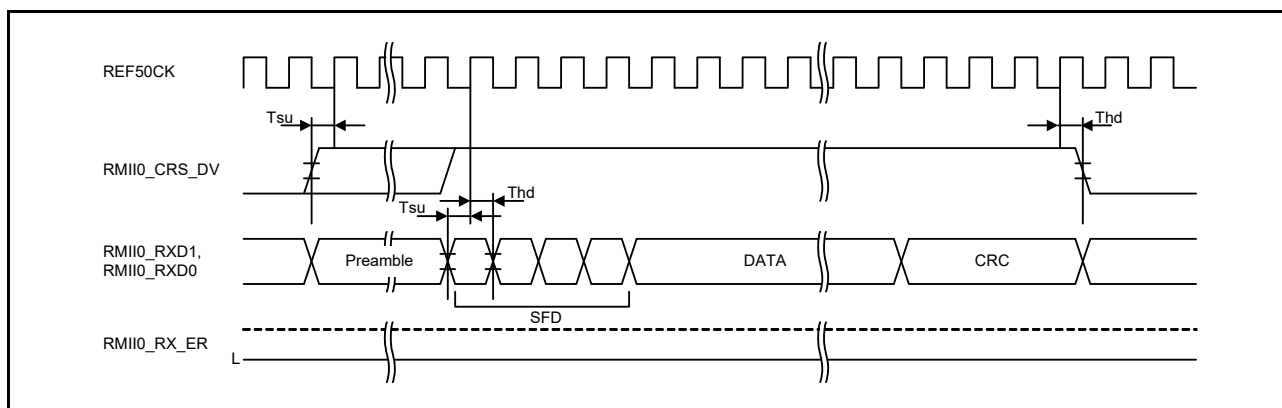


Figure 5.58 RMII Reception Timing (Normal Operation)