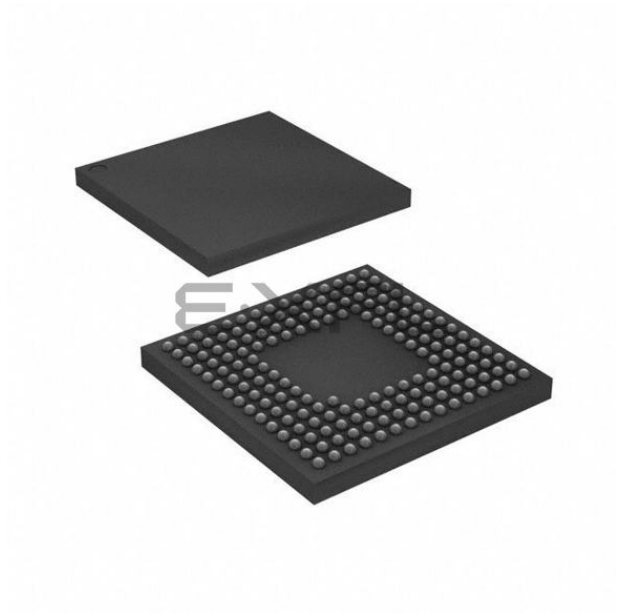
Renesas Electronics America Inc - R5F565NEDDLC#20 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	136
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565neddlc-20

Table 1.3 List of Products (3/8)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	SDHI/SDSI	Dual bank	Operating temperature (°C)
RX65N (D version)	R5F565N4EDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N4FDLK	PTLG0145KA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565NEDDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NEHDLJ	PTLG0100JA-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565NCDDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +85
	R5F565NCHDLJ	PTLG0100JA-A	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565N9ADLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N9BDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N9EDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N9FDLJ	PTLG0100JA-A	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565N7ADLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N7BDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N7EDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N7FDLJ	PTLG0100JA-A	768 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
	R5F565N4ADLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +85
	R5F565N4BDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +85
	R5F565N4EDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +85
	R5F565N4FDLJ	PTLG0100JA-A	512 K	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +85
RX65N (G version)	R5F565NEDGFC	PLQP0176KB-A *1	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NEHGFC	PLQP0176KB-A *1	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565NCDGFC	PLQP0176KB-A *1	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NCHGFC	PLQP0176KB-A *1	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565NEDGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NEHGFB	PLQP0144KA-B	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565NCDGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Not available	Available	Available	–40 to +105
	R5F565NCHGFB	PLQP0144KA-B	1.5 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +105
	R5F565N9AGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Not available	Not available	–40 to +105
	R5F565N9BGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Not available	Available	Not available	–40 to +105
	R5F565N9EGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Not available	Not available	–40 to +105
	R5F565N9FGFB	PLQP0144KA-B	1 M	256 K	Not included	120 MHz	Available	Available	Not available	–40 to +105

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/8)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
H13		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DATA5-B	IRQ6-DS	
H14		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DATA6-B		
H15	TRDATA3	PG7	D31						
J1	EXTAL	P36							
J2	VCC								
J3		P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
J4	TMS	PF3							
J12		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B		
J13	VSS								
J14		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B		
J15		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B		
K1		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0	PCKO		IRQ3-DS	
K2		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC		IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1				
K4	TCK	PF1			SCK1				
K12		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2-B	LCD_TCON2-B		
K13		P71	A18/CS1#		ET0_MDIO				
K14	VCC								
K15		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DATA0-B	IRQ12	
L1		P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
L2		P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1				

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (5/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
92	VSS								
93		P73	CS3#	PO16	ET0_WOL		LCD_EXTCLK-A		
94		PB7	A15	MTIOC3B/ TIOCB5/PO31	ET0_CRS/ RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11	SDSI_D1-B			
95		PB6	A14	MTIOC3D/ TIOCA5/PO30	ET0_ETXD1/ RMII0_TXD1/ RXD9/SMISO9/ SSCL9/ SMISO11/ SSCL11/RXD11	SDSI_D0-B			
96		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	ET0_ETXD0/ RMII0_TXD0/ SCK9/SCK11	SDSI_CLK-B	LCD_CLK-B		
97		PB4	A12	TIOCA4/PO28	ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD-B	LCD_TCON0-B		
98		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11#	ET0_RX_ER/ RMII0_RX_ER/ SCK4/SCK6	SDSI_D3-B	LCD_TCON1-B		
99		PB2	A10	TIOCC3/ TCLKC/PO26	ET0_RX_CLK/ REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2-B	LCD_TCON2-B		
100		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	ET0_ERXD0/ RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		LCD_TCON3-B	IRQ4-DS	
101		P72	A19/CS2#		ET0_MDC		LCD_DATA23-A		
102		P71	A18/CS1#		ET0_MDIO				
103	VCC								
104		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DATA0-B	IRQ12	
105	VSS								
106		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DATA1-B		
107		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DATA2-B		
108		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DATA3-B		

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (6/8)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
109		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DATA4-B	IRQ5-DS	
110		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DATA5-B	IRQ6-DS	
111	TRDATA3	PG7	D31						
112		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DATA6-B		
113	TRDATA2	PG6	D30						
114		PA1	DQM3/A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DATA7-B	IRQ11	
115	VCC								
116	TRCLK	PG5	D29						
117	VSS								
118		PA0	DQM2/ BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DATA8-B		
119	TRSYNC	PG4	D28						
120		P67	DQM1/CS7#	MTIOC7C				IRQ15	
121	TRDATA1	PG3	D27						
122		P66	DQM0/CS6#	MTIOC7D					
123	TRDATA0	PG2	D26						
124		P65	CKE/CS5#						
125		PE7	D15[A15/ D15]/D7[A7/ D7]	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105
126		PE6	D14[A14/ D14]/D6[A6/ D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DATA10-B	IRQ6	AN104
127	VCC								
128		P70	SDCLK						
129	VSS								
130		PE5	D13[A13/ D13]/D5[A5/ D5]	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DATA11-B	IRQ5	AN103
131		PE4	D12[A12/ D12]/D4[A4/ D4]	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DATA12-B		AN102
132		PE3	D11[A11/ D11]/D3[A3/ D3]	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#/SS12#	MMC_D7-B	LCD_DATA13-B		AN101
133		PE2	D10[A10/ D10]/D2[A2/ D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3-B	MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100

Table 4.1 List of I/O Registers (Address Order) (13 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 79F1h	ICU	Software Configurable Interrupt A Source Select Register 241	SLIAR241	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F2h	ICU	Software Configurable Interrupt A Source Select Register 242	SLIAR242	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F3h	ICU	Software Configurable Interrupt A Source Select Register 243	SLIAR243	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F4h	ICU	Software Configurable Interrupt A Source Select Register 244	SLIAR244	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F5h	ICU	Software Configurable Interrupt A Source Select Register 245	SLIAR245	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F6h	ICU	Software Configurable Interrupt A Source Select Register 246	SLIAR246	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F7h	ICU	Software Configurable Interrupt A Source Select Register 247	SLIAR247	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F8h	ICU	Software Configurable Interrupt A Source Select Register 248	SLIAR248	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79F9h	ICU	Software Configurable Interrupt A Source Select Register 249	SLIAR249	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FAh	ICU	Software Configurable Interrupt A Source Select Register 250	SLIAR250	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FBh	ICU	Software Configurable Interrupt A Source Select Register 251	SLIAR251	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FCh	ICU	Software Configurable Interrupt A Source Select Register 252	SLIAR252	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FDh	ICU	Software Configurable Interrupt A Source Select Register 253	SLIAR253	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FEh	ICU	Software Configurable Interrupt A Source Select Register 254	SLIAR254	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 79FFh	ICU	Software Configurable Interrupt A Source Select Register 255	SLIAR255	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUB
0008 7A00h	ICU	Software Configurable Interrupt Source Select Register Write Protect Register	SLIPRCR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 7A01h	ICU	EXDMAC Trigger Select Register	SELEXDR	8	8	2 ICLK to 1 PCLKA/B	2 ICLK	ICUB
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	WDTA
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	IWDTa
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK	IWDTa

Table 4.1 List of I/O Registers (Address Order) (27 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A08Ah	SCI4	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Bh	SCI4	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Ch	SCI4	I²C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A091h	SCI4	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A090h	SCI4	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A092h	SCI4	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0A9h	SCI5	I²C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0AAh	SCI5	I²C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0ABh	SCI5	I²C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (30 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A0EEh	SCI7	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0F0h	SCI7	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0F1h	SCI7	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0F0h	SCI7	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A0F2h	SCI7	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A106h	SMCI8	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A109h	SCI8	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A10Ah	SCI8	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A10Bh	SCI8	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A10Ch	SCI8	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh, SCIi
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh, SCIi

Table 4.1 List of I/O Registers (Address Order) (42 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C283h	SYSTEM	Deep Standby Interrupt Enable Register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C285h	SYSTEM	Deep Standby Interrupt Enable Register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C287h	SYSTEM	Deep Standby Interrupt Flag Register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C289h	SYSTEM	Deep Standby Interrupt Flag Register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Bh	SYSTEM	Deep Standby Interrupt Edge Register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Dh	SYSTEM	Deep Standby Interrupt Edge Register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-Speed On-Chip Oscillator Power Supply Control Register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C296h	FLASH	Flash P/E Protect Register	FWEPROR	8	8	2 ICLK		Flash
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA

Table 4.1 List of I/O Registers (Address Order) (48 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb

Table 4.1 List of I/O Registers (Address Order) (49 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 00F0h	USB0	PHY Cross Point Adjustment Register	PHYSLEW	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0400h	USB	Deep Standby USB Transceiver Control/Pin Monitoring Register	DPUSR0R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0404h	USB	Deep Standby USB Suspend/Resume Interrupt Register	DPUSR1R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000C 0000h	EDMAC 0	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0008h	EDMAC 0	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0010h	EDMAC 0	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0018h	EDMAC 0	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0020h	EDMAC 0	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0028h	EDMAC 0	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0030h	EDMAC 0	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0038h	EDMAC 0	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0040h	EDMAC 0	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0048h	EDMAC 0	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0050h	EDMAC 0	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0058h	EDMAC 0	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0064h	EDMAC 0	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0068h	EDMAC 0	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 006Ch	EDMAC 0	Independent Output Signal Setting Register	IOSR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0070h	EDMAC 0	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a

Table 5.4 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Input pull-up MOS current	Other than P35	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μA	V_{in} = VCC
Input capacitance	All input pins (except for ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	Ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM		—	—	16		

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.
Note 7. Reference value

Table 5.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item				Symbol	D version		G version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current*1	High-speed operating mode	Max.*2		I_{CC}*3	—	60	—	73	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz
		Normal	Peripheral function clock signal supplied*4		26	—	26	—		
			Peripheral function clock signal stopped*4		13	—	13	—		
		Core Mark	Peripheral function clock signal stopped*4		17	—	17	—		
		Sleep mode: The clock signal to peripheral modules is supplied*4			20	38	20	52		
		All-module-clock-stop mode (reference value)			9	26	9	39		
		Increased by BGO operation *7	Reading from the code flash memory while the data flash memory is being programmed		6	—	6	—		
			Reading from the code flash memory while the code flash memory is being programmed		7	—	7	—		
		Increased by Trusted Secure IP operation			—	12	—	12		
	Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4				1.6	—	1.6	—		All clocks 1 MHz
	Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4				1.6	—	1.6	—		All clocks 32.768 kHz
	Software standby mode				1.6	13	1.6	22.4		
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)			15.5	70	15.5	98	μA	
		Power not supplied to standby RAM and USB resume detecting unit (USB0 only)	Power-on reset circuit and low-power consumption function disabled*5		11.5	42	11.5	54		
			Power-on reset circuit and low-power consumption function enabled*6		4.9	32	4.9	47		
		Increased by RTC operation	When a low C_L crystal is in use		1	—	1	—		
			When a standard C_L crystal is in use		2	—	2	—		
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		0.9	—	0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					1.6	—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		1.7	—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					3.3	—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on returning from deep software standby mode		Inrush current*8	I_{RUSH}	—	130	—	130	mA	
			Energy of inrush current*8	E_{RUSH}	—	1.0	—	1.0	μC	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)
[D version]
I_{CC} Max. = 0.38 × f + 14 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.18 × f + 4 (ICLK 1 MHz max) (normal operation in high-speed operating mode)
I_{CC} Typ. = 0.4 × f + 1.2 (low-speed operating mode 1)
I_{CC} Max. = 0.2 × f + 14 (sleep mode)
[G version]

5.3 AC Characteristics

Table 5.10 Operating Frequency (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	120	MHz
	Peripheral module clock (PCLKA)			—	—	120	
	Peripheral module clock (PCLKB)			—	—	60	
	Peripheral module clock (PCLKC)			—	—	60	
	Peripheral module clock (PCLKD)			—	—	60	
	Flash-IF clock (FCLK)			—*1	—	60	
	External bus clock (BCLK)	Other than 100-pin package		—	—	120	
		100-pin package		—	—	60	
	BCLK pin output	Other than 100-pin package		—	—	60	
		100-pin package		—	—	30	
	SDRAM clock (SDCLK)	Other than 100-pin package		—	—	60	
	SDCLK pin output	Other than 100-pin package		—	—	60	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 5.11 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	1	MHz
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	Peripheral module clock (PCLKC)*1			—	—	1	
	Peripheral module clock (PCLKD)*1			—	—	1	
	Flash-IF clock (FCLK)			—	—	1	
	External bus clock (BCLK)	Other than 100-pin package		—	—	1	
		100-pin package		—	—	1	
	BCLK pin output	Other than 100-pin package		—	—	1	
		100-pin package		—	—	1	
	SDRAM clock (SDCLK)	Other than 100-pin package		—	—	1	
	SDCLK pin output	Other than 100-pin package		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

Table 5.22 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 5.13
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	23	—	24	t_{Lcyc}	

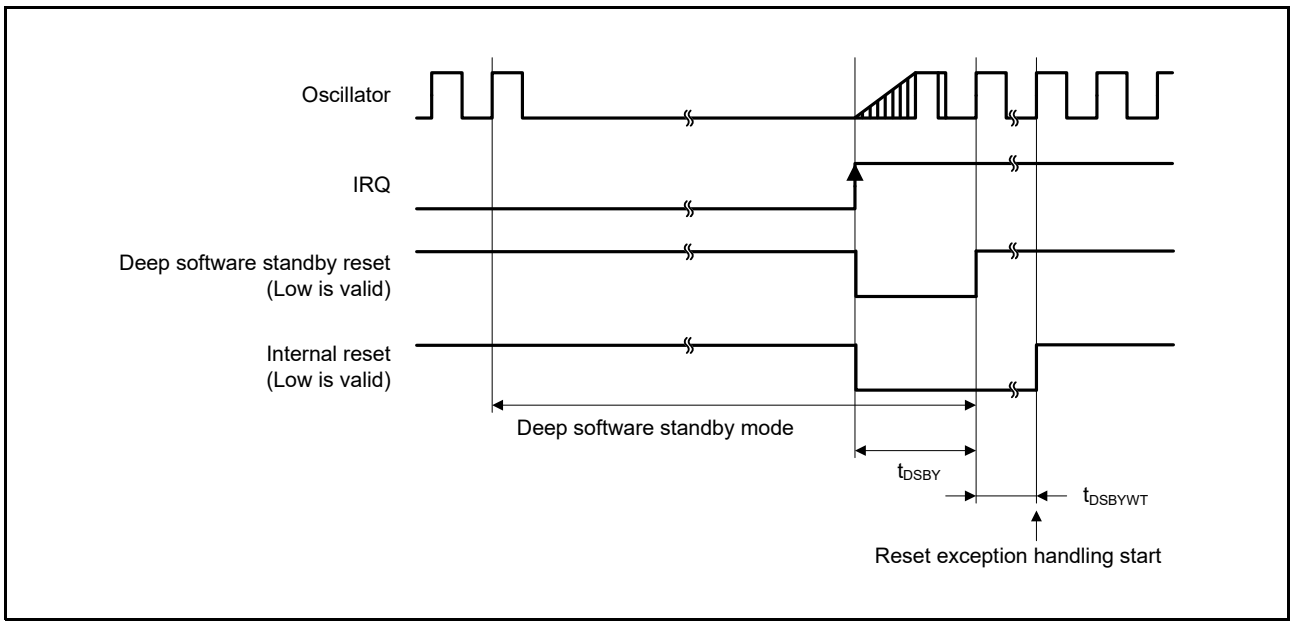

Figure 5.13 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.23 Control Signal Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 5.14
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 5.14
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 5.15
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 5.15

Note 1. t_{PBcyc}: PCLKB cycle

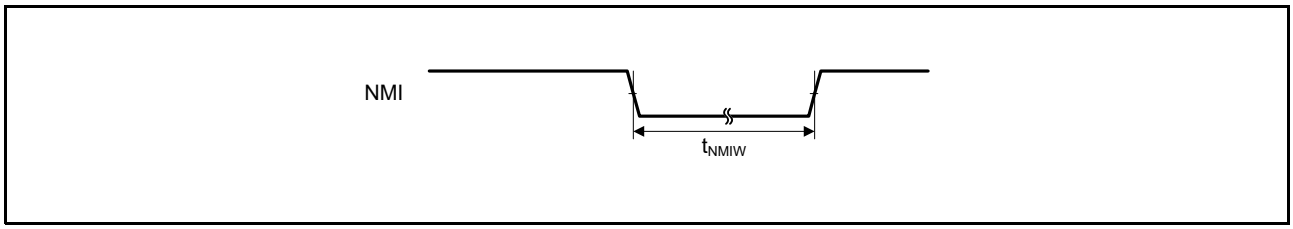

Figure 5.14 NMI Interrupt Input Timing

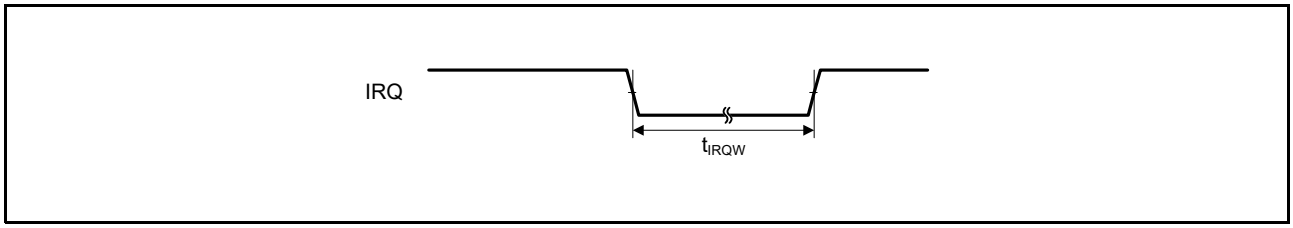

Figure 5.15 IRQ Interrupt Input Timing

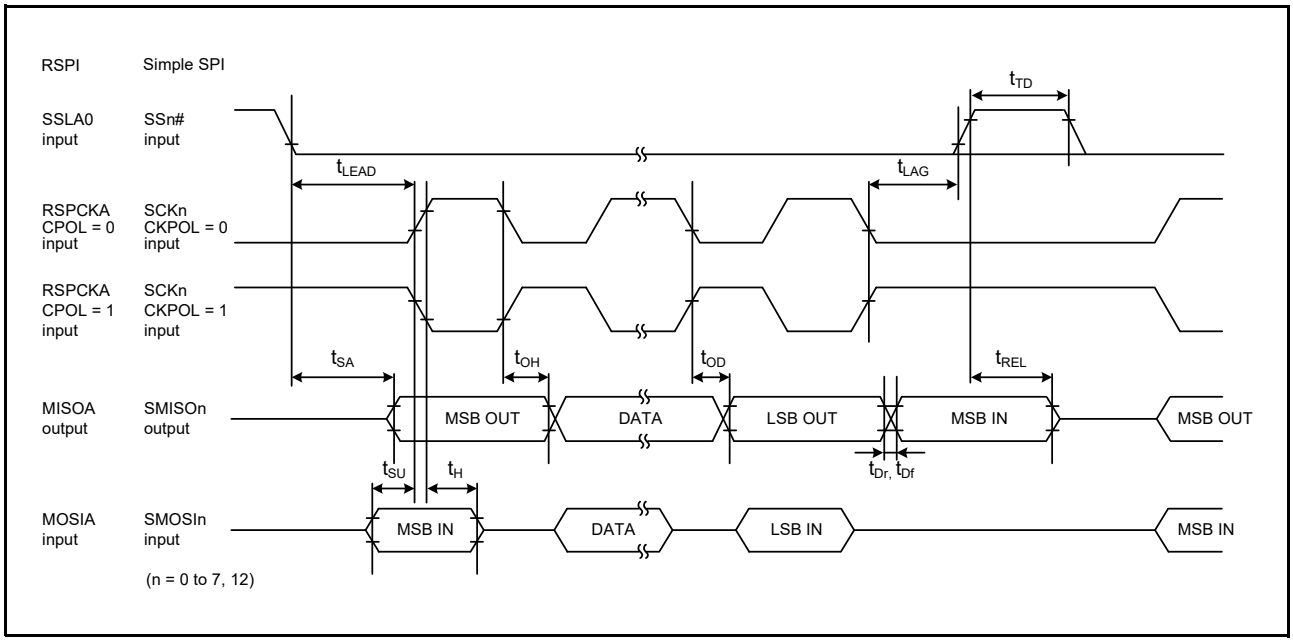

Figure 5.49 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

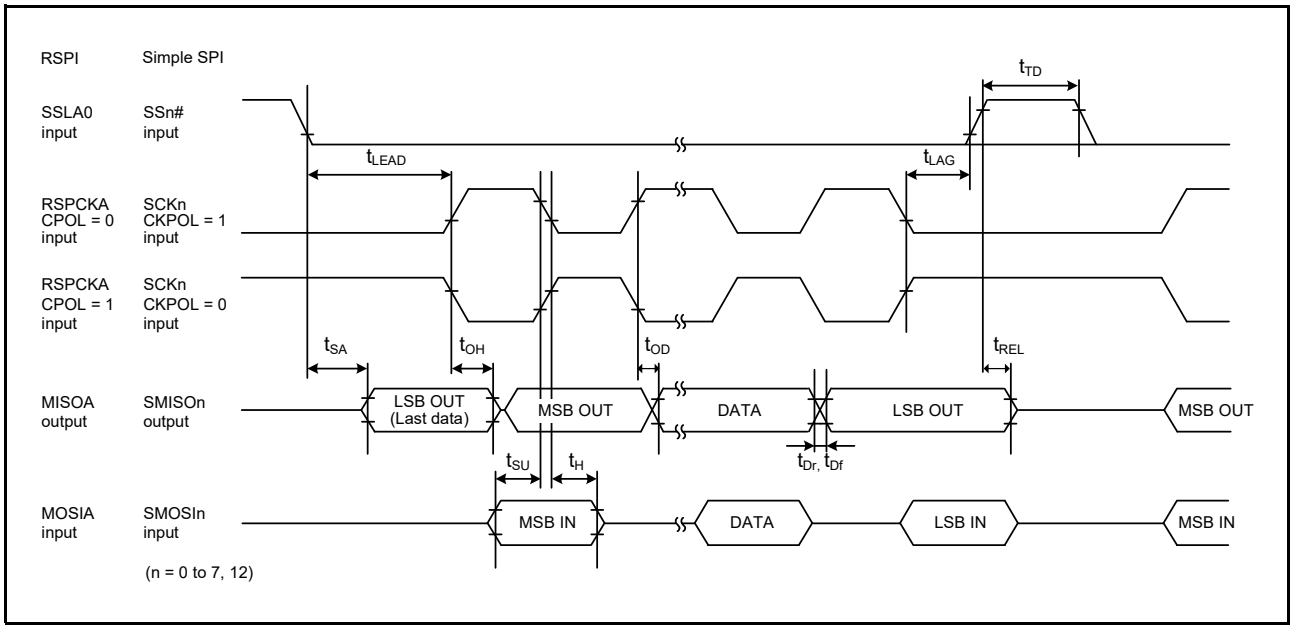

Figure 5.50 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

Table 5.37 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions*2
QSPI	QSPCLK clock cycle	t_{QScyc}	2	4080	t_{PBcyc}	Figure 5.51
	Data input setup time*3	t_{Su}	6.5	—	ns	Figure 5.52, Figure 5.53
	Data input hold time	t_{IH}	5	—	ns	
	SS setup time	t_{LEAD}	1.5	8.5	t_{QScyc}	
	SS hold time	t_{LAG}	1	8	t_{QScyc}	
	Data output delay time	t_{OD}	—	10.0	ns	
	Data output hold time	t_{OH}	–5	—	ns	
	Successive transmission delay time	t_{TD}	1	8	t_{QScyc}	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the QSPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. For version G products (+85 < Ta ≤ +105°C), the high-drive ability control register of the QSPCLK pin measures this data input setup time with the high-speed interface high-drive output selected.

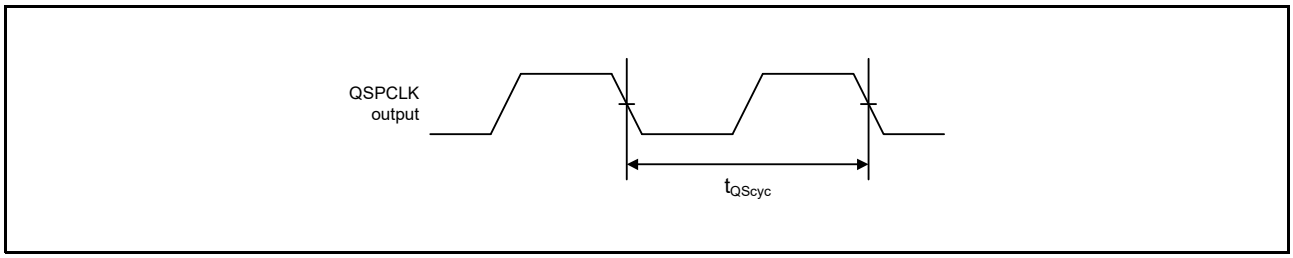

Figure 5.51 QSPI Clock Timing

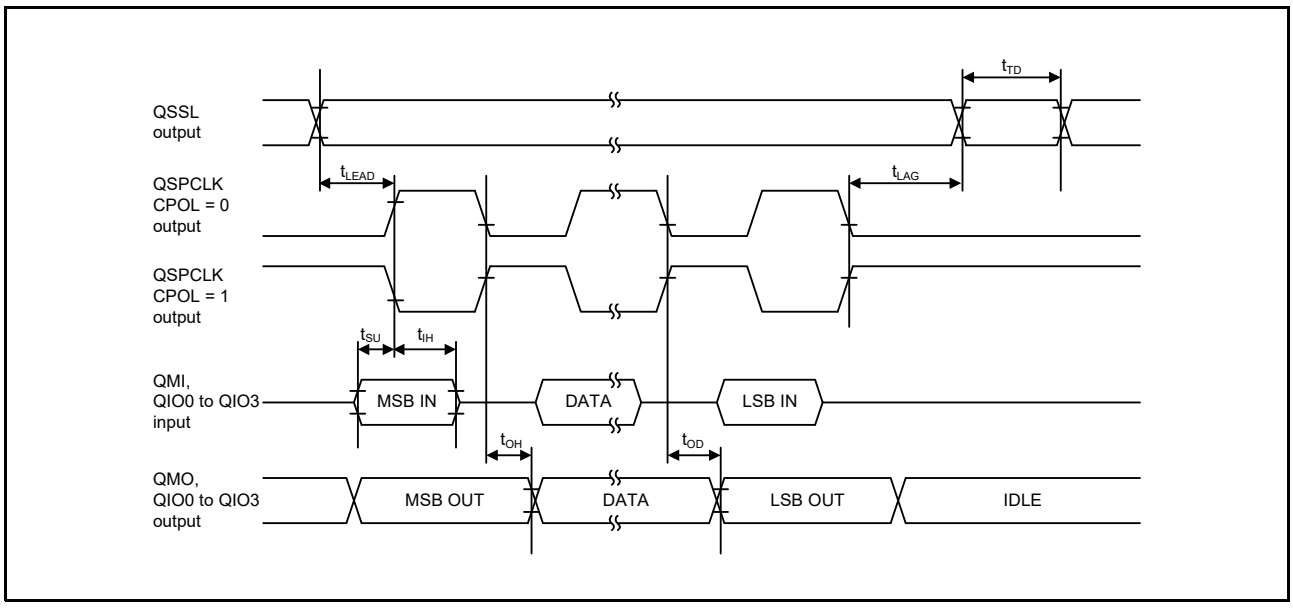

Figure 5.52 Transmit/Receive Timing (CPHA = 0)

Table 5.55 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.18	1.9	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.9	11	—	1.7	10	ms
	128 bytes	t_{DP128}	—	4.7	27	—	2.9	16	—	2.6	15	ms
	256 bytes	t_{DP256}	—	8.9	50	—	5.4	31	—	4.9	28	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	33	—	—	30	µs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	100000 *2	—	—	Times
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	132	—	—	120	µs
First suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	216	—	—	132	—	—	120	µs
	128 bytes	—	—	—	216	—	—	132	—	—	120	µs
	256 bytes	—	—	—	216	—	—	132	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Suspend delay time during erasing (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

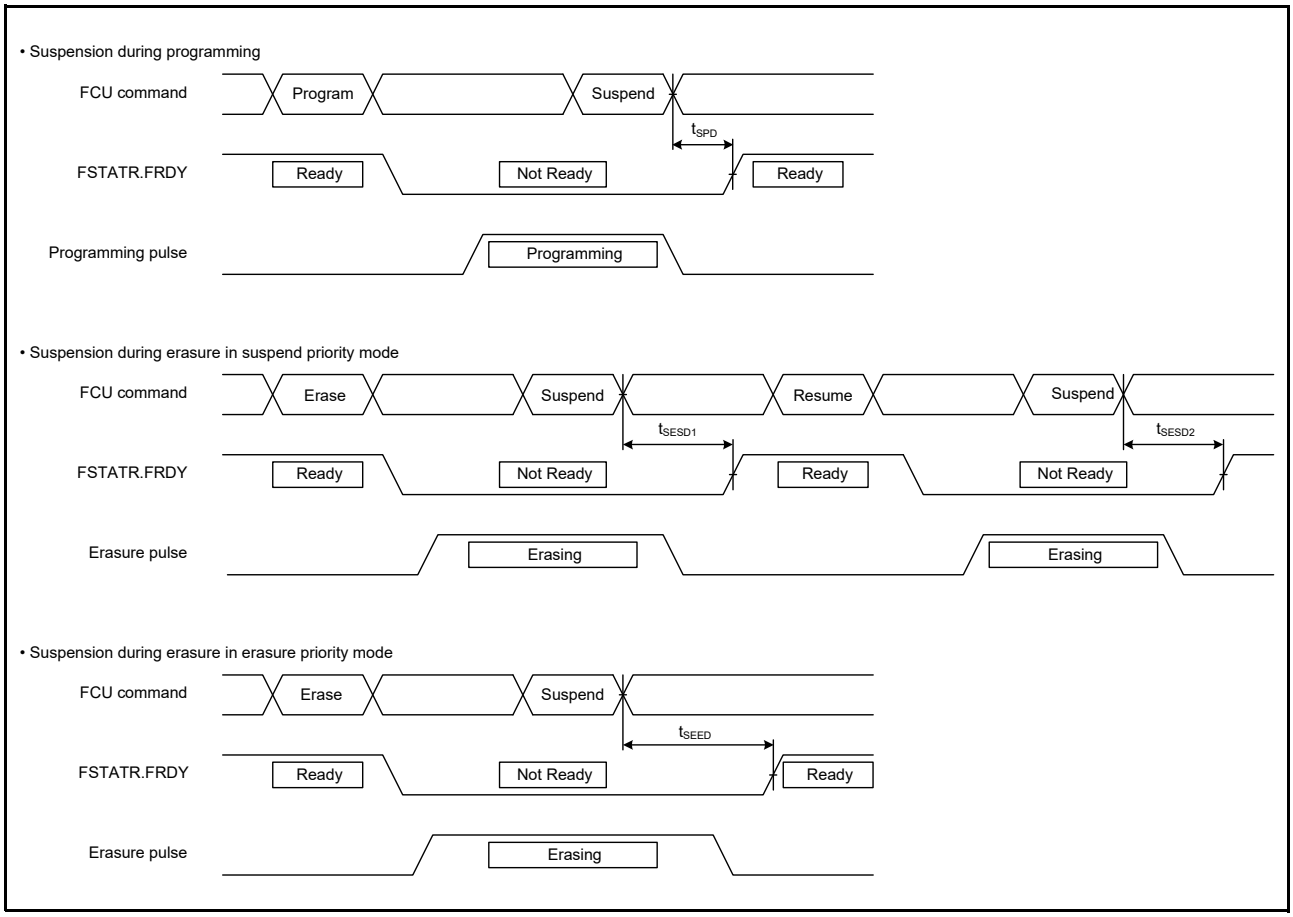

Figure 5.82 Flash Memory Programming/Erasure Suspension Timing

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.