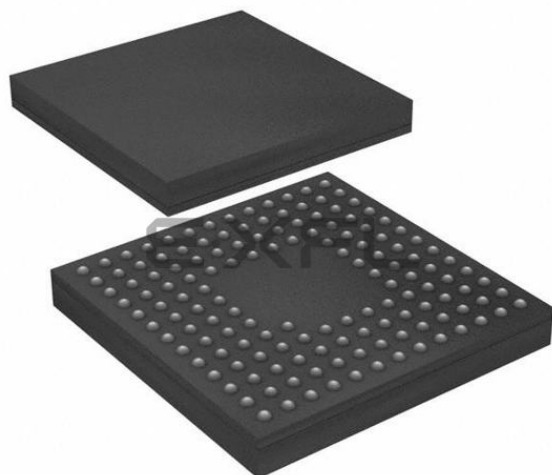




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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, QSPI, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f565neddlk-20

Table 1.1 Outline of Specifications (6/9)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIg, SCIlh, SCLi)	13 channels (SCIg: 10 channels + SCIlh: 1 channel + SCLi: 2 channels) - SCIg, SCIlh, SCLi Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Start-bit detection: Level or edge detection is selectable. Simple I²C Simple SPI 9-bit transfer mode Bit rate modulation Double-speed mode - SCIg, SCIlh Average transfer rate clock can be input from TMR timers for SCIl5, SCIl6, and SCIl12 Event linking by the ELC (only on channel 5) - SCIlh Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format - SCLi Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit
	I ² C bus interface (RIICa)	3 channels (only channel 0 can be used in fast-mode plus) Communication formats I²C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) - Event linking by the ELC
	CAN module (CAN)	2 channels - Compliance with the ISO11898-1 specification (standard frame and extended frame) 32 mailboxes per channel
	Serial peripheral interface (RSPIC)	3 channels RSPIC transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPIC clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave - Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transit/receive data can be swapped in byte units - Buffered structure Double buffers for both transmission and reception - RSPCK can be stopped with the receive buffer full for master reception. - Event linking by the ELC
	Quad serial peripheral interface (QSPI)	1 channel - Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) - Programmable bit length and selectable active sense and phase of the clock signal - Sequential execution of transfer - LSB or MSB first is selectable

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/8)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
51		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCUR A		LCD_CL K-A	IRQ4	
52		P13	WR2#/BC2#	MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		LCD_TC ON0-A	IRQ3	ADTRG1 #
53		P12	WR3#/ BC3#	MTIC5U/ TMC1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]		LCD_TC ON1-A	IRQ2	
54	VCC_USB								
55					USB0_DM				
56					USB0_DP				
57	VSS_USB								
58		PJ2			TXD8/SMOSI8/ SSDA8/SSLC3-B		LCD_TC ON2-A		
59		PJ1		MTIOC6A	RXD8/SMISO8/ SSCL8/SSLC2-B		LCD_TC ON3-A		
60		PJ0		MTIOC6B	SCK8/SSLC1-B		LCD_DA TA0-A		
61		P85		MTIOC6C/ TIOCC0			LCD_DA TA1-A		
62		P84		MTIOC6D			LCD_DA TA2-A		
63		P57			RXD7/SMISO7/ SSCL7/SSLC0-B		LCD_DA TA3-A		
64		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7/RSPCKC- B		LCD_DA TA4-A		
65		P55	D0[A0/D0]/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC- B/CRX1		LCD_DA TA5-A	IRQ10	
66		P54	D1[A1/D1]/ EDACK0	MTIOC4B/ TMC1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1		LCD_DA TA6-A		
67		P11		MTIC5V/TMC13	SCK2		LCD_DA TA7-A	IRQ1	
68		P10	ALE	MTIC5W/ TMRI3				IRQ0	
69		P53*1	BCLK						
70		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A				
71		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A				
72		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A				
73	VSS								

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
E4	EMLE								
E5		P44						IRQ12-DS	AN004
E10		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DA TA8-B*1		
E11		P66	DQM0/CS6#	MTIOC7D					
E12		P65	CKE/CS5#						
E13		P67	DQM1/CS7#	MTIOC7C				IRQ15	
F1	XCIN								
F2	XCOUT								
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
F4	VBATT								
F10		PA3	A3	MTIOC0D/ MTCLKD/ TIOC0D/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DA TA5-B*1	IRQ6-DS	
F11	VSS								
F12		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DA TA7-B*1	IRQ11	
F13		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DA TA6-B*1		
G1	XTAL	P37							
G2	RES#								
G3	MD/FINED								
G4	BSCANP								
G10		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DA TA3-B*1		
G11		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMC13/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DA TA2-B*1		
G12	VCC								
G13		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DA TA4-B*1	IRQ5-DS	
H1	EXTAL	P36							
H2	VCC								
H3	VSS								
H4	UPSEL	P35						NMI	
H10		P72	A19/CS2#		ET0_MDC				
H11		P71	A18/CS1#		ET0_MDIO				

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (5/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
87		PB0	A8	MTIC5W/ TIOCA3/PO24	ET0_ERXD1/ RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		LCD_DA TA0-B*1	IRQ12	
88		PA7	A7	TIOCB2/PO23	ET0_WOL/ MISOA-B		LCD_DA TA1-B*1		
89		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	ET0_EXOUT/ CTS5#/RTS5#/ SS5#/MOSIA-B		LCD_DA TA2-B*1		
90		PA5	A5	MTIOC6B/ TIOCB1/PO21	ET0_LINKSTA/ RSPCKA-B		LCD_DA TA3-B*1		
91	VCC								
92		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	ET0_MDC/TXD5/ SMOSI5/SSDA5/ SSLA0-B		LCD_DA TA4-B*1	IRQ5-DS	
93	VSS								
94		PA3	A3	MTIOC0D/ MTCLKD/ TIOC0D/ TCLKB/PO19	ET0_MDIO/ RXD5/SMISO5/ SSCL5		LCD_DA TA5-B*1	IRQ6-DS	
95		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B		LCD_DA TA6-B*1		
96		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	ET0_WOL/ SCK5/SSLA2-B		LCD_DA TA7-B*1	IRQ11	
97		PA0	BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF	ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B		LCD_DA TA8-B*1		
98		P67	DQM1/CS7#	MTIOC7C				IRQ15	
99		P66	DQM0/CS6#	MTIOC7D					
100		P65	CKE/CS5#						
101		PE7	D15[A15/ D15]/D7[A7/ D7]*1	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ MMC_RES#-B	LCD_DA TA9-B*1	IRQ7	AN105
102		PE6	D14[A14/ D14]/D6[A6/ D6]*1	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ MMC_CD-B	LCD_DA TA10-B*1	IRQ6	AN104
103	VCC								
104		P70	SDCLK						
105	VSS								
106		PE5	D13[A13/ D13]/D5[A5/ D5]*1	MTIOC4C/ MTIOC2B	ET0_RX_CLK/ REF50CK0/ RSPCKB-B		LCD_DA TA11-B*1	IRQ5	AN103
107		PE4	D12[A12/ D12]/D4[A4/ D4]*1	MTIOC4D/ MTIOC1A/ PO28	ET0_ERXD2/ SSLB0-B		LCD_DA TA12-B*1		AN102
108		PE3	D11[A11/ D11]/D3[A3/ D3]*1	MTIOC4B/ PO26/TOC3/ POE8#	ET0_ERXD3/ CTS12#/ RTS12#/SS12#	MMC_D7-B	LCD_DA TA13-B*1		AN101
109		PE2	D10[A10/ D10]/D2[A2/ D2]*1	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/SSLB3- B	MMC_D6-B	LCD_DA TA14-B*1	IRQ7-DS	AN100

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (1/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
1	AVCC1								
2	EMLE								
3	AVSS1								
4		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ SS6#/CTS0#/ RTS0#/SS0#				
5	VCL								
6	VBATT								
7	MD/FINED								
8	XCIN								
9	XCOUT								
10	RES#								
11	XTAL	P37							
12	VSS								
13	EXTAL	P36							
14	VCC								
15	UPSEL	P35						NMI	
16	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	ET0_LINKSTA/ SCK6/SCK0			IRQ4	
17		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0			IRQ3-DS	
18		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0/ USB0_VBUSEN			IRQ2-DS	
19	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A			IRQ1-DS	
20	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A			IRQ0-DS	
21	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A				
22	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#/ MOSIB-A				
23		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3				ADTRG0 #
24		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN				
25		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#				

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSDI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
79		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	QMI-B/QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DA TA17-B*1	IRQ7	AN107
80		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	QMO-B/QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DA TA18-B*1	IRQ6	AN106
81		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DA TA19-B*1	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DA TA20-B*1	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	RSPCKC-A	QIO3-B/SDHI_D3- B/MMC_D3-B	LCD_DA TA21-B*1	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/TIC2	MISOC-A/CRX0	QIO2-B/SDHI_D2- B/MMC_D2-B	LCD_DA TA22-B*1	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ POE0#	MOSIC-A/CTX0		LCD_DA TA23-B*1	IRQ1	AN109
86		PD0	D0[A0/D0]	POE4#			LCD_EX TCLK-B *1	IRQ0	AN108
87		P47						IRQ15- DS	AN007
88		P46						IRQ14- DS	AN006
89		P45						IRQ13- DS	AN005
90		P44						IRQ12- DS	AN004
91		P43						IRQ11- DS	AN003
92		P42						IRQ10- DS	AN002
93		P41						IRQ9-DS	AN001
94	VREFL0								
95		P40						IRQ8-DS	AN000
96	VREFH0								
97	AVCC0								
98		P07						IRQ15	ADTRG0 #
99	AVSS0								
100		P05						IRQ13	DA1

Note 1. These pins are only enabled for products with 2 or 1.5 Mbytes of code flash memory.

Note 2. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (4 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 20DFh	DMAC3	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2100h	DMAC4	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2104h	DMAC4	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2108h	DMAC4	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 211Fh	DMAC4	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 215Fh	DMAC5	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 219Fh	DMAC6	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 21DCh	DMAC7	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 21DDh	DMAC7	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 21DEh	DMAC7	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 21DFh	DMAC7	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2200h	DMAC	DMAC Module Start Register	DMAST	8	8	2	ICLK	DMACaA
0008 2204h	DMAC	DMAC74 Interrupt Status Monitor Register	DMIST	8	8	2	ICLK	DMACaA
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2	ICLK	DTCb
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2	ICLK	DTCb
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2	ICLK	DTCb

Table 4.1 List of I/O Registers (Address Order) (5 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK		DTCb
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK		DTCb
0008 2410h	DTC	DTC Index Table Base Register	DTCIBR	32	32	2 ICLK		DTCb
0008 2414h	DTC	DTC Operation Register	DTCOR	8	8	2 ICLK		DTCb
0008 2416h	DTC	DTC Sequence Transfer Enable Register	DTCSEQE	16	16	2 ICLK		DTCb
0008 2418h	DTC	DTC Address Displacement Register	DTCDISP	32	32	2 ICLK		DTCb
0008 2800h	EXDMA C0	EXDMA Source Address Register	EDMSAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2804h	EXDMA C0	EXDMA Destination Address Register	EDMDAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2808h	EXDMA C0	EXDMA Transfer Count Register	EDMCRA	32	32	1, 2 BCLK		EXDMA Ca
0008 280Ch	EXDMA C0	EXDMA Block Transfer Count Register	EDMCRB	16	16	1, 2 BCLK		EXDMA Ca
0008 2810h	EXDMA C0	EXDMA Transfer Mode Register	EDMTMD	16	16	1, 2 BCLK		EXDMA Ca
0008 2812h	EXDMA C0	EXDMA Output Setting Register	EDMOMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2813h	EXDMA C0	EXDMA Interrupt Setting Register	EDMINT	8	8	1, 2 BCLK		EXDMA Ca
0008 2814h	EXDMA C0	EXDMA Address Mode Register	EDMAMD	32	32	1, 2 BCLK		EXDMA Ca
0008 2818h	EXDMA C0	EXDMA Offset Register	EDMOFR	32	32	1, 2 BCLK		EXDMA Ca
0008 281Ch	EXDMA C0	EXDMA Transfer Enable Register	EDMCNT	8	8	1, 2 BCLK		EXDMA Ca
0008 281Dh	EXDMA C0	EXDMA Software Start Register	EDMREQ	8	8	1, 2 BCLK		EXDMA Ca
0008 281Eh	EXDMA C0	EXDMA Status Register	EDMSTS	8	8	1, 2 BCLK		EXDMA Ca
0008 2820h	EXDMA C0	EXDMA External Request Sense Mode Register	EDMRMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2821h	EXDMA C0	EXDMA External Request Flag Register	EDMERF	8	8	1, 2 BCLK		EXDMA Ca
0008 2822h	EXDMA C0	EXDMA Peripheral Request Flag Register	EDMPRF	8	8	1, 2 BCLK		EXDMA Ca
0008 2840h	EXDMA C1	EXDMA Source Address Register	EDMSAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2844h	EXDMA C1	EXDMA Destination Address Register	EDMDAR	32	32	1, 2 BCLK		EXDMA Ca
0008 2848h	EXDMA C1	EXDMA Transfer Count Register	EDMCRA	32	32	1, 2 BCLK		EXDMA Ca
0008 284Ch	EXDMA C1	EXDMA Block Transfer Count Register	EDMCRB	16	16	1, 2 BCLK		EXDMA Ca
0008 2850h	EXDMA C1	EXDMA Transfer Mode Register	EDMTMD	16	16	1, 2 BCLK		EXDMA Ca
0008 2852h	EXDMA C1	EXDMA Output Setting Register	EDMOMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2853h	EXDMA C1	EXDMA Interrupt Setting Register	EDMINT	8	8	1, 2 BCLK		EXDMA Ca
0008 2854h	EXDMA C1	EXDMA Address Mode Register	EDMAMD	32	32	1, 2 BCLK		EXDMA Ca
0008 285Ch	EXDMA C1	EXDMA Transfer Enable Register	EDMCNT	8	8	1, 2 BCLK		EXDMA Ca
0008 285Dh	EXDMA C1	EXDMA Software Start Register	EDMREQ	8	8	1, 2 BCLK		EXDMA Ca
0008 285Eh	EXDMA C1	EXDMA Status Register	EDMSTS	8	8	1, 2 BCLK		EXDMA Ca
0008 2860h	EXDMA C1	EXDMA External Request Sense Mode Register	EDMRMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2861h	EXDMA C1	EXDMA External Request Flag Register	EDMERF	8	8	1, 2 BCLK		EXDMA Ca

Table 4.1 List of I/O Registers (Address Order) (43 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Registers 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C428h	RTC	RTC Control Register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ah	RTC	Frequency Register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ch	RTC	Frequency Register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd

Table 4.1 List of I/O Registers (Address Order) (45 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 0820h to 0009 083Fh	CAN0	Message Control Registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0840h	CAN0	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 0842h	CAN0	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 0844h	CAN0	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0848h	CAN0	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0849h	CAN0	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 084Ah	CAN0	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 084Bh	CAN0	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 084Ch	CAN0	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 084Dh	CAN0	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 084Eh	CAN0	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 084Fh	CAN0	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0850h	CAN0	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0851h	CAN0	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0852h	CAN0	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0853h	CAN0	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0854h	CAN0	Time Stamp Register	TSR	16	16	2, 3 PCLKB	2 ICLK	CAN
0009 0856h	CAN0	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 0858h	CAN0	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1200h to 0009 13FFh	CAN1	Mailbox Registers 0 to 31	MB0 to 31	128	8, 16, 32*6	2, 3 PCLKB	2 ICLK	CAN
0009 1400h to 0009 141Fh	CAN1	Mask Registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 1420h	CAN1	FIFO Received ID Compare Register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 1424h	CAN1	FIFO Received ID Compare Register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 1428h	CAN1	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 142Ch	CAN1	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 1820h to 0009 183Fh	CAN1	Message Control Registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1840h	CAN1	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 1842h	CAN1	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 1844h	CAN1	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 1848h	CAN1	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1849h	CAN1	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 184Ah	CAN1	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 184Bh	CAN1	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 184Ch	CAN1	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 184Dh	CAN1	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 184Eh	CAN1	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 184Fh	CAN1	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1850h	CAN1	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1851h	CAN1	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1854h	CAN1	Time Stamp Register	TSR	16	16	2, 3 PCLKB	2 ICLK	CAN
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 4200h	CMTW0	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW

Table 4.1 List of I/O Registers (Address Order) (49 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00F0h	USB0	PHY Cross Point Adjustment Register	PHYSLEW	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0400h	USB	Deep Standby USB Transceiver Control/Pin Monitoring Register	DPUSR0R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0404h	USB	Deep Standby USB Suspend/Resume Interrupt Register	DPUSR1R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000C 0000h	EDMAC 0	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0008h	EDMAC 0	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0010h	EDMAC 0	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0018h	EDMAC 0	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0020h	EDMAC 0	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0028h	EDMAC 0	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0030h	EDMAC 0	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0038h	EDMAC 0	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0040h	EDMAC 0	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0048h	EDMAC 0	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0050h	EDMAC 0	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0058h	EDMAC 0	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0064h	EDMAC 0	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0068h	EDMAC 0	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 006Ch	EDMAC 0	Independent Output Signal Setting Register	IOSR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a
000C 0070h	EDMAC 0	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	1 to 3 ICLK	EDMAC a

Table 4.1 List of I/O Registers (Address Order) (51 / 61)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 01F8h	ETHER C0	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	1 to 7 ICLK	ETHER C
000C 1200h	MTU3	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Ch	MTU3	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1231h	MTU	Timer Interrupt Skipping Counter 1A	TITCNT1A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 123Ch	MTU	Timer Interrupt Skipping Counter 2A	TITCNT2A	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4, 5 PCLKA	1, 2 ICLK	MTU3a
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	4, 5 PCLKA	1, 2 ICLK	MTU3a

Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Note 7. Reference value

Table 5.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,

T_a = T_{opr}

Item			Symbol	D version		G version		Unit	Test Conditions			
				Typ.	Max.	Typ.	Max.					
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	60	—	73	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz		
		Normal	Peripheral function clock signal supplied*4		26	—	26	—				
			Peripheral function clock signal stopped*4		13	—	13	—				
		Core Mark	Peripheral function clock signal stopped*4		17	—	17	—				
			Sleep mode: The clock signal to peripheral modules is supplied*4		20	38	20	52				
		All-module-clock-stop mode (reference value)			9	26	9	39				
		Increased by BGO operation*7	Reading from the code flash memory while the data flash memory is being programmed		6	—	6	—				
			Reading from the code flash memory while the code flash memory is being programmed		7	—	7	—				
		Increased by Trusted Secure IP operation			—	12	—	12				
		Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4			1.6	—	1.6	—				
		Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4			1.6	—	1.6	—				
		Software standby mode			1.6	13	1.6	22.4				
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)		15.5	70	15.5	98	μA				
		Power not supplied to standby RAM and USB resume detecting unit (USB0 only)	Power-on reset circuit and low-power consumption function disabled*5	11.5	42	11.5	54					
			Power-on reset circuit and low-power consumption function enabled*6	4.9	32	4.9	47					
		Increased by RTC operation	When a low C _L crystal is in use	1	—	1	—					
			When a standard C _L crystal is in use	2	—	2	—					
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use	0.9	—	0.9	—					
				1.6	—	1.6	—					
			When a crystal oscillator for standard clock loads is in use	1.7	—	1.7	—					
				3.3	—	3.3	—					
		Inrush current on returning from deep software standby mode	Inrush current*8	I _{RUSH}	—	130	—			130	mA	
			Energy of inrush current*8	E _{RUSH}	—	1.0	—			1.0		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripheral modules is stopped in this state.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)

[D version]

I_{CC} Max. = 0.38 × f + 14 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.18 × f + 4 (ICLK 1 MHz max) (normal operation in high-speed operating mode)

I_{CC} Typ. = 0.4 × f + 1.2 (low-speed operating mode 1)

I_{CC} Max. = 0.2 × f + 14 (sleep mode)

[G version]

5.3.2 Clock Timing

Table 5.14 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = 0$ V,
 $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	Figure 5.3
	100-pin package		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Other than 100-pin package	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	

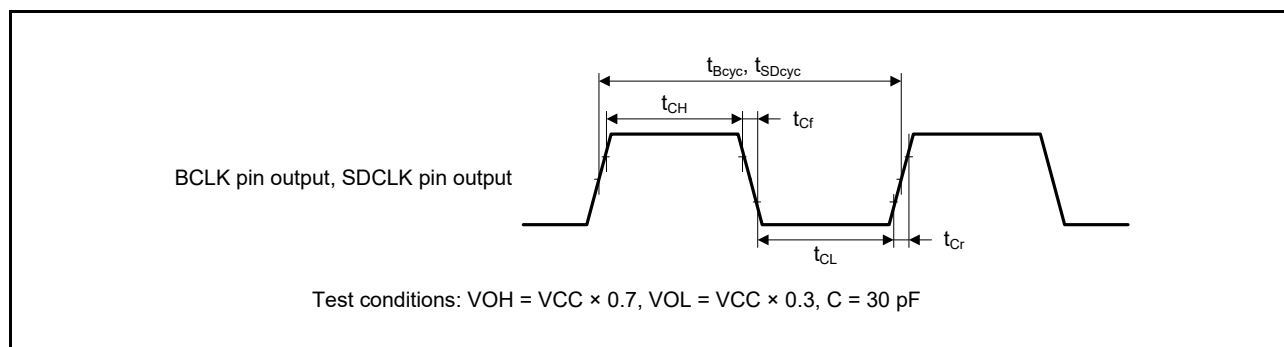
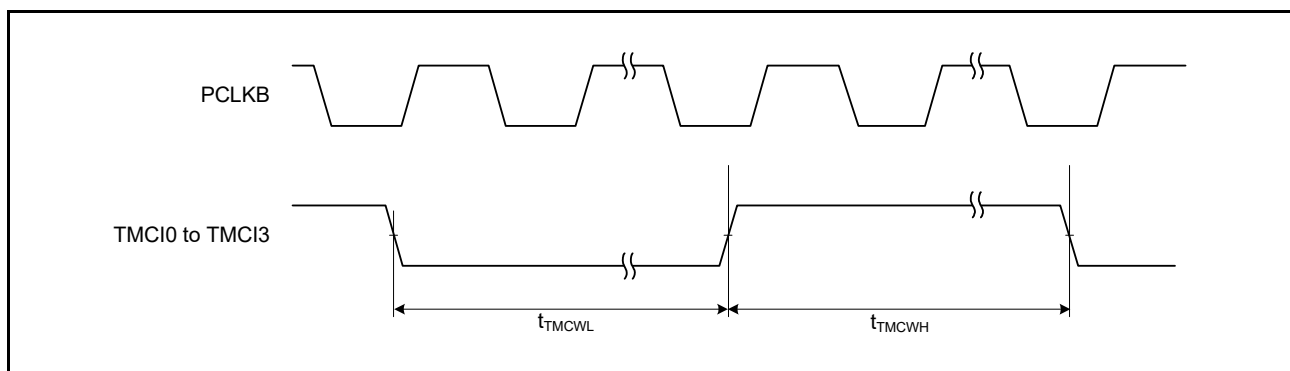
**Figure 5.3 BCLK Pin and SDCLK Pin Output Timing**

Table 5.28 TMR Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH} , t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 5.36
		Both-edge setting		2.5	—		

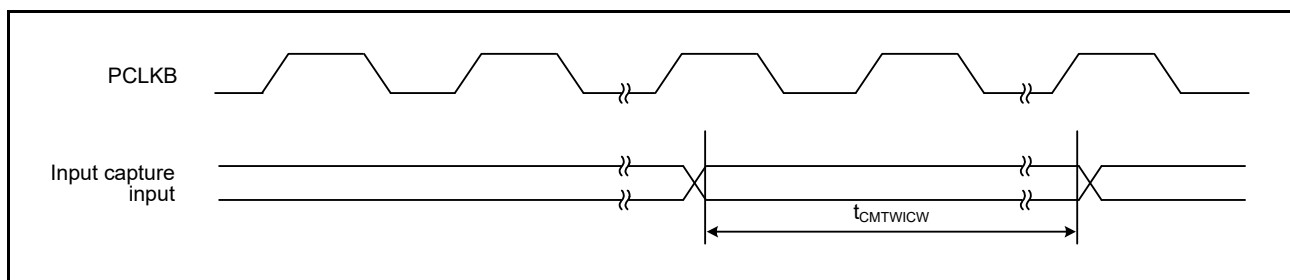
Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.36 TMR Clock Input Timing****Table 5.29 CMTW Timing**

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, 2.7 V $\leq V_{REFH0} \leq AVCC0$,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$,
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PBcyc}	Figure 5.37
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.37 CMTW Input Capture Input Timing**

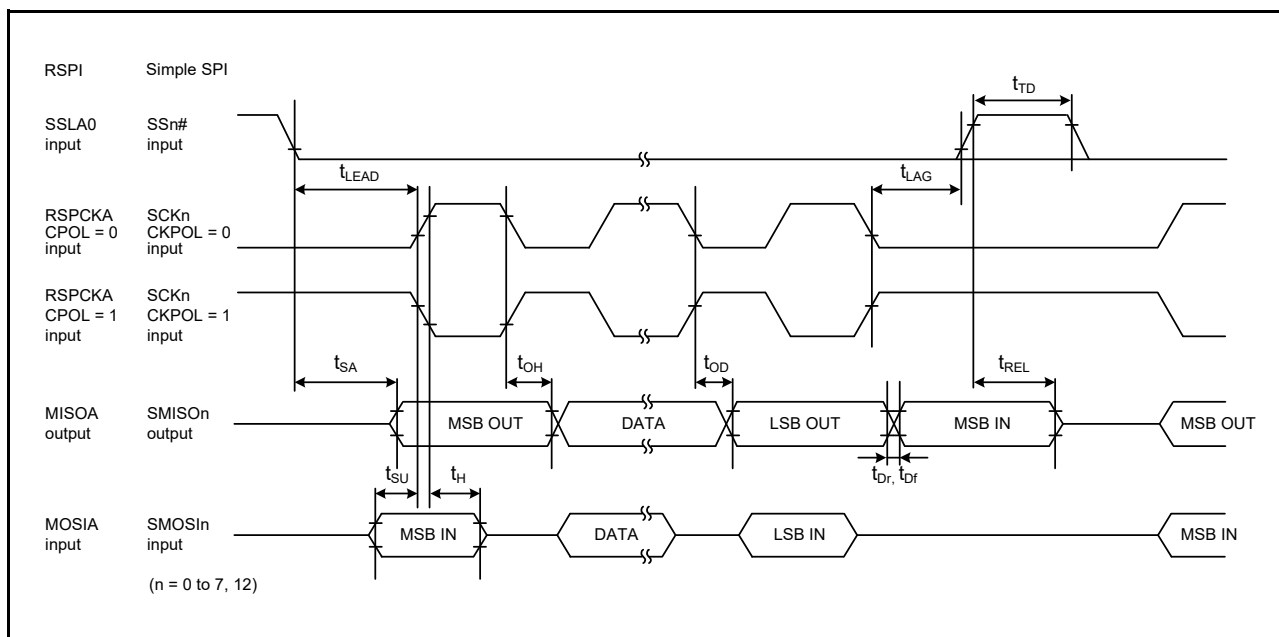


Figure 5.49 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

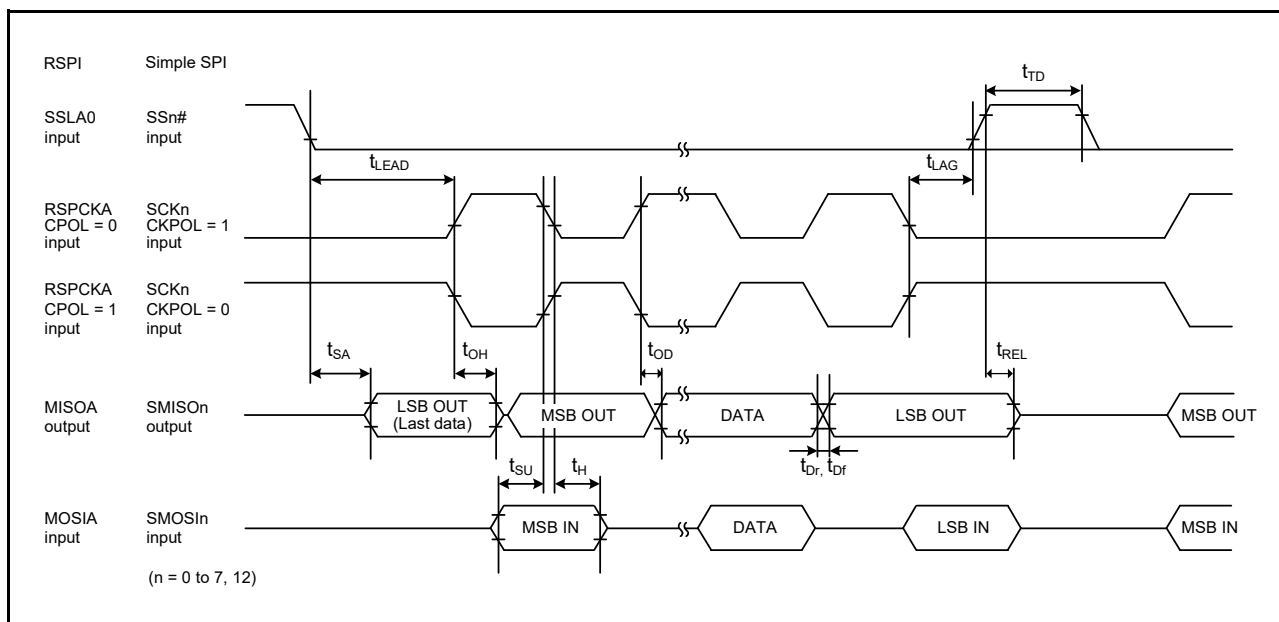


Figure 5.50 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

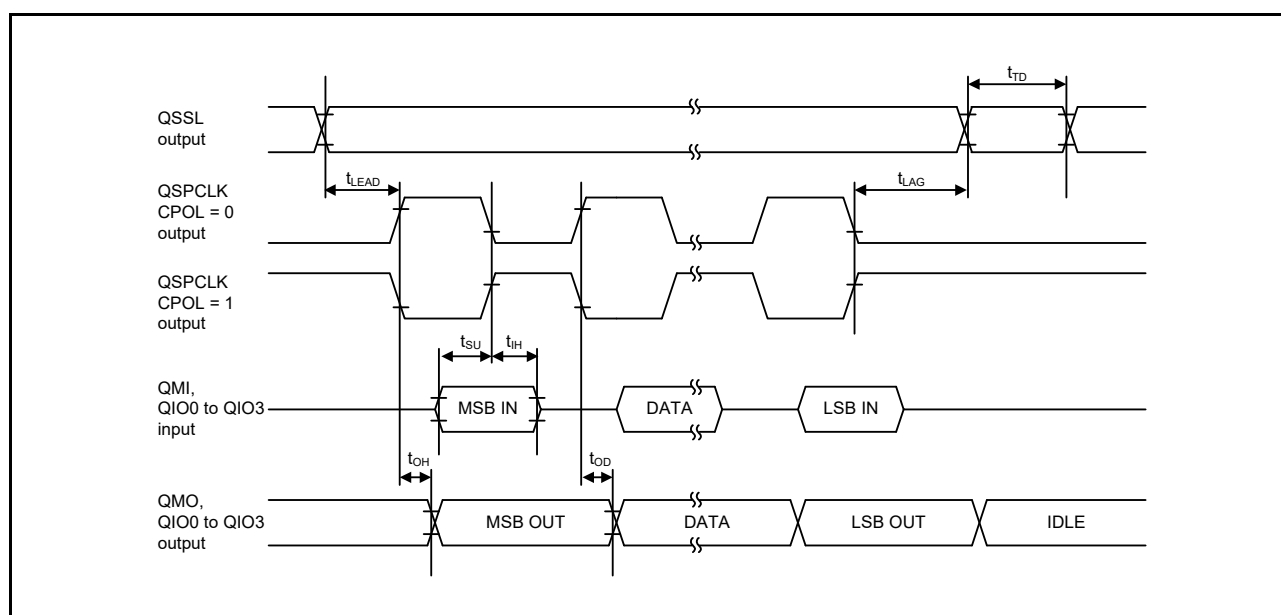


Figure 5.53 Transmit/Receive Timing (CPHA = 1)

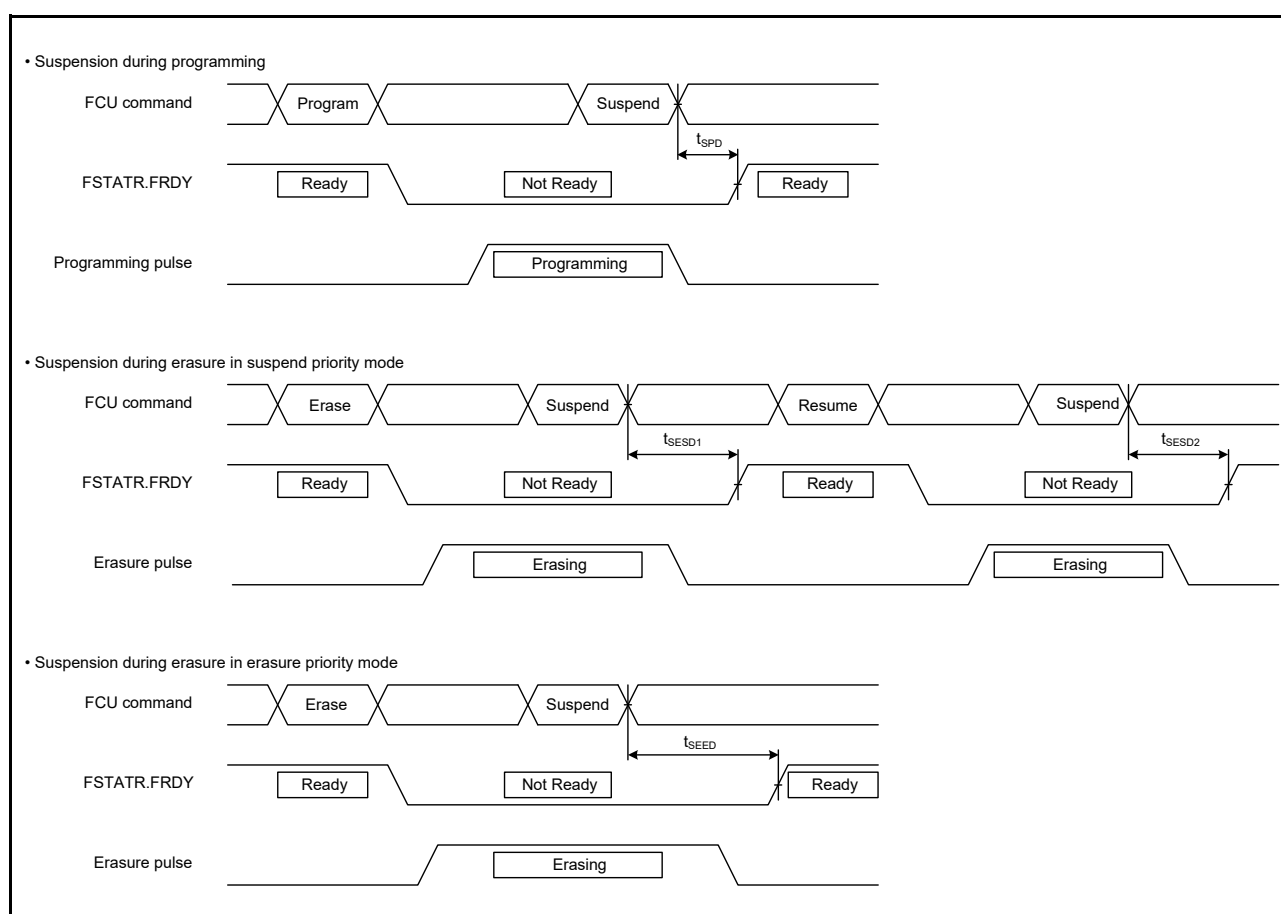


Figure 5.82 Flash Memory Programming/Erasure Suspension Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

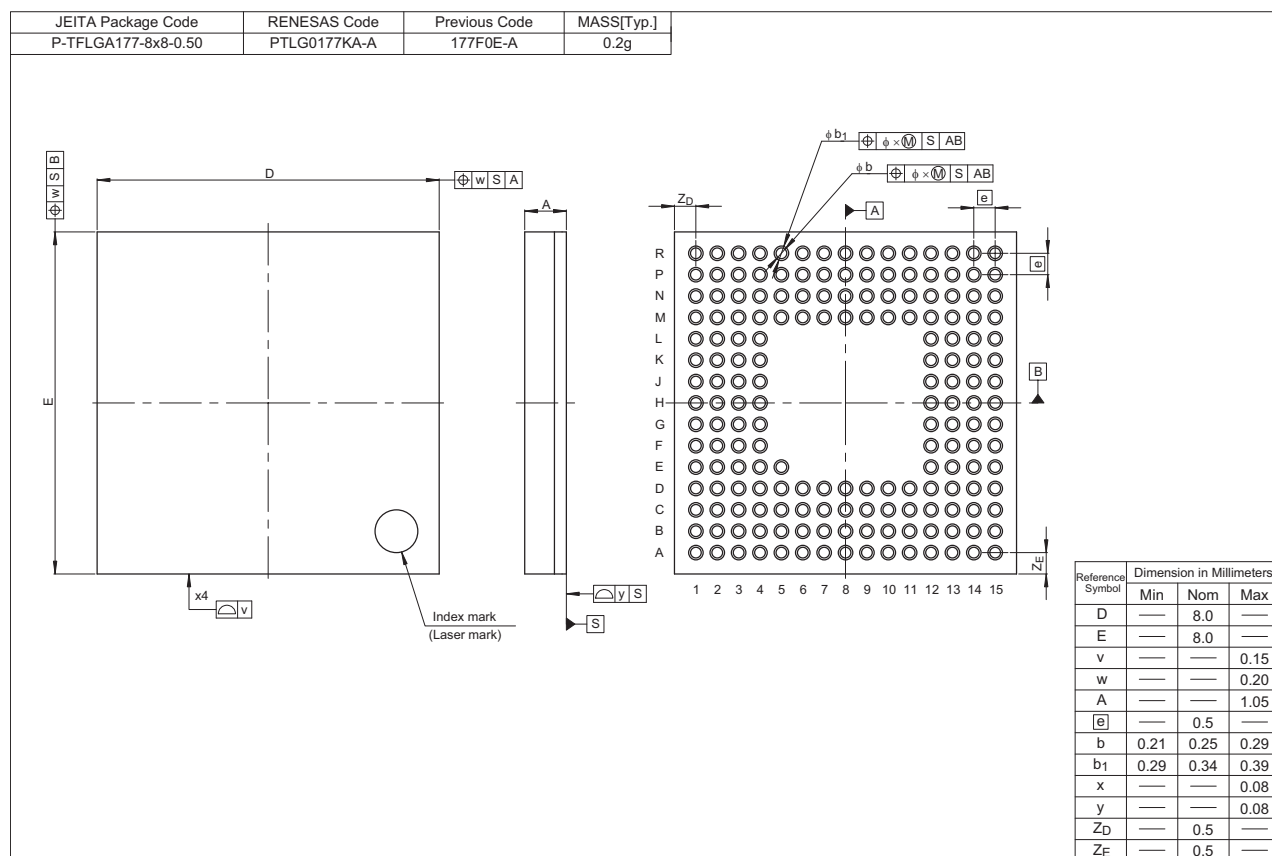


Figure A 177-Pin TFLGA (PTLG0177KA-A)