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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	42K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2238n40f80lrabkxuma1

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



16/32-Bit

Architecture

XC2232N, XC2234N, XC2236N, XC2238N

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance XC2000 Family / Value Line

Data Sheet V1.5 2013-02

Microcontrollers



Summary of Features

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance XC223xN (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC223xN are summarized here.

- · High-performance CPU with five-stage pipeline and MPU
 - 12.5 ns instruction cycle @ 80 MHz CPU clock (single-cycle execution)
 - One-cycle 32-bit addition and subtraction with 40-bit result
 - One-cycle multiplication (16 × 16 bit)
 - Background division (32 / 16 bit) in 21 cycles
 - One-cycle multiply-and-accumulate (MAC) instructions
 - Enhanced Boolean bit manipulation facilities
 - Zero-cycle jump execution
 - Additional instructions to support HLL and operating systems
 - Register-based design with multiple variable register banks
 - Fast context switching support with two additional local register banks
 - 16 Mbytes total linear address space for code and data
 - 1,024 Bytes on-chip special function register area (C166 Family compatible)
 Integrated Memory Protection Unit (MPU)
- · Interrupt system with 16 priority levels providing 96 interrupt nodes
 - Selectable external inputs for interrupt generation and wake-up
 - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
 - 8 Kbytes on-chip stand-by RAM (SBRAM)
 - 2 Kbytes on-chip dual-port RAM (DPRAM)
 - Up to 16 Kbytes on-chip data SRAM (DSRAM)
 - Up to 16 Kbytes on-chip program/data SRAM (PSRAM)
 - Up to 320 Kbytes on-chip program memory (Flash memory)
 - Memory content protection through Error Correction Code (ECC)



Summary of Features

1.3 Definition of Feature Variants

The XC223xN types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3	Continuous Flash	Memory	Ranges
---------	------------------	--------	--------

Total Flash Size	1st Range ¹⁾	2nd Range	3rd Range
320 Kbytes	C0'0000 _H C0'EFFF _H	C1'0000 _H C4'FFFF _H	n.a.
192 Kbytes	C0'0000 _H C0'EFFF _H	C1'0000 _H C1'FFFF _H	C4'0000 _H C4'FFFF _H
128 Kbytes	C0'0000 _H C0'EFFF _H	C4'0000 _H C4'FFFF _H	n.a.
64 Kbytes	C0'0000 _H C0'EFFF _H	n.a.	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

Table 4	Elach Momon	Modulo Allocation	(in Khytee	١
I able 4	Flash wellory	would Anocation	(III KDytes	,

	-		
Total Flash Size	Flash 0 ¹⁾	Flash 1	
320	256	64	
192	128	64	
128	64	64	
64	64	-	

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XC223xN types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5	Interface Char	nel Association
---------	----------------	-----------------

Total Number	Available Channels / Message Objects	
7 ADC0 channels	CH0, CH2, CH4, CH8, CH10, CH13, CH15	
2 ADC1 channels	CH0, CH4	
1 CAN node	CAN0 64 message objects	
2 CAN nodes	CAN0, CAN1 64 message objects	



General Device Information

2 General Device Information

The XC223xN series (16/32-Bit Single-Chip Microcontroller

with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature singlechip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.



Figure 2 XC223xN Logic Symbol



XC2232N, XC2234N, XC2236N, XC2238N XC2000 Family / Value Line

General Device Information

Table	Table 6Pin Definitions and Functions (cont'd)				
Pin	Symbol	Ctrl.	Туре	Function	
40	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output	
	U0C0_SCLK OUT	01	St/B	USIC0 Channel 0 Shift Clock Output	
	CCU60_CC6 2	O2	St/B	CCU60 Channel 2 Output	
	CCU60_CC6 2INA	I	St/B	CCU60 Channel 2 Input	
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input	
42	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output	
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output	
	U0C0_SELO 3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output	
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.	
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input	
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input	
43	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output	
	CCU60_COU T60	O2	St/B	CCU60 Channel 0 Output	
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input	
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input	
44	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output	
	U0C0_SELO 3	01	St/B	USIC0 Channel 0 Select/Control 3 Output	
	CCU60_COU T61	O2	St/B	CCU60 Channel 1 Output	
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input	
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input	
	ESR1_9	I	St/B	ESR1 Trigger Input 9	



3 Functional Description

The architecture of the XC223xN combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC223xN.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC223xN.



Figure 4 Block Diagram



3.3 Memory Protection Unit (MPU)

The XC223xN's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.4 Memory Checker Module (MCHK)

The XC223xN's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.



to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

3.6 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XC223xN provides a broad range of debug and emulation features. User software running on the XC223xN can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing of data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XC2000 Family emulation device. With this device the DAP can operate on clock rates of up to 20 MHz.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.



XC2232N, XC2234N, XC2236N, XC2238N XC2000 Family / Value Line

Functional Description



Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.



The RTC module can be used for different purposes:

- · System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time



3.19 Instruction Set Summary

Table 11 lists the instructions of the XC223xN.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Mnemonic	Description	Bytes		
ADD(B)	Add word (byte) operands			
ADDC(B)	Add word (byte) operands with Carry	2/4		
SUB(B)	Subtract word (byte) operands	2/4		
SUBC(B)	Subtract word (byte) operands with Carry	2/4		
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- \times 16-bit)	2		
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2		
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2		
CPL(B)	Complement direct word (byte) GPR	2		
NEG(B)	Negate direct word (byte) GPR	2		
AND(B)	Bitwise AND, (word/byte operands)	2/4		
OR(B)	Bitwise OR, (word/byte operands)	2/4		
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2/4		
BCLR/BSET	Clear/Set direct bit	2		
BMOV(N)	Move (negated) direct bit to direct bit	4		
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4		
BCMP	Compare direct bit to direct bit	4		
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4		
CMP(B)	Compare word (byte) operands	2/4		
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4		
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4		
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2		
SHL/SHR	Shift left/right direct word GPR	2		

Table 11 Instruction Set Summary



Table 13Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Overload current coupling factor for digital I/O pins	K _{OVD} CC	_	1.0 x 10 ⁻²	3.0 x 10 ⁻²	-	<i>I</i> _{OV} < 0 mA; not subject to production test
		_	1.0 x 10 ⁻⁴	5.0 x 10 ⁻³	-	<i>I</i> _{OV} > 0 mA; not subject to production test
Absolute sum of overload currents	$\Sigma I_{OV} $ SR	-	-	50	mA	not subject to production test
Digital core supply voltage for domain M ⁸⁾	V _{DDIM} CC	-	1.5	-		
Digital core supply voltage for domain 1 ⁸⁾	V _{DDI1} CC	-	1.5	-		
Digital supply voltage for IO pads and voltage regulators	$V_{\rm DDP}{ m SR}$	3.0	-	5.5	V	
Digital ground voltage	$V_{\rm SS}{\rm SR}$	-	0	-	V	

1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

- 2) Use one Capacitor for each pin.
- This is the reference load. For bigger capacitive loads, use the derating factors listed in the pad properties section.
- 4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).
- 5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.
- 6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: V_{OV} > V_{IHmax} (I_{OV} > 0) or V_{OV} < V_{ILmin} ((I_{OV} < 0). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).



4.3.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{\rm OV}$.

Note: Operating Conditions apply.

Table 16 is valid under the following conditions: $V_{\text{DDP}} \le 5.5 \text{ V}$; V_{DDP} typ. 5 V; $V_{\text{DDP}} \ge 4.5 \text{ V}$

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	C _{IO} CC	_	-	10	pF	not subject to production test
Input Hysteresis ²⁾	HYS CC	0.11 x V _{DDP}	-	-	V	R _S = 0 Ohm
Absolute input leakage current on pins of analog ports ³⁾	I _{OZ1} CC	-	10	200	nA	$V_{\rm IN}$ > $V_{\rm SS}$; $V_{\rm IN}$ < $V_{\rm DDP}$
Absolute input leakage current for all other pins. To be double	I _{OZ2} CC	-	0.2	5	μA	$T_{J} \leq 110 \text{ °C};$ $V_{IN} > V_{SS};$ $V_{IN} < V_{DDP}$
bond pins. ³⁾¹⁾⁴⁾		_	0.2	15	μA	$T_{\rm J} \leq$ 150 °C; $V_{\rm IN} > V_{\rm SS}$; $V_{\rm IN} < V_{\rm DDP}$
Pull Level Force Current ⁵⁾	I _{PLF} SR	250	_	_	μA	
Pull Level Keep Current ⁶⁾	I _{PLK} SR	_	_	30	μA	$ \begin{array}{l} V_{\rm IN} \geq V_{\rm IHmin}(pull \\ up_enabled); \\ V_{\rm IN} \leq V_{\rm ILmax}(pull \\ down_enabled) \end{array} $
Input high voltage (all except XTAL1)	V _{IH} SR	0.7 x V _{DDP}	-	V _{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	$V_{\rm IL}$ SR	-0.3	-	0.3 x V _{DDP}	V	

 Table 16
 DC Characteristics for Upper Voltage Range



	••			·	,	
Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Output High voltage ⁷⁾	V _{OH} CC	V _{DDP} - 1.0	-	_	V	$I_{\rm OH} \ge I_{\rm OHmax}$
		V _{DDP} - 0.4	-	-	V	$I_{\text{OH}} \ge I_{\text{OHnom}}^{8}$
Output Low Voltage ⁷⁾	V _{OL} CC	-	-	0.4	V	$I_{\rm OL} \le I_{\rm OLnom}^{8}$
		-	-	1.0	V	$I_{\rm OL} \leq I_{\rm OLmax}$

Table 16 DC Characteristics for Upper Voltage Range (cont'd)

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

 Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{\rm IN} < V_{\rm SS}$) or supply ripple ($V_{\rm IN} > V_{\rm DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{\rm INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{\rm CV}$.
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (*T*_J = junction temperature [°C]): *I*_{OZ} = 0.05 x e^(1.5 + 0.028 x T,J>) [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = *V*_{DDP} *V*_{PIN} [V]): *I*_{OZ} = *I*_{OZtempmax} (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.
- Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.
- 6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.
- 7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL} -> V_{SS} , V_{OH} -> V_{DDP}). However, only the levels for nominal output currents are verified.



4.3.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{\rm OV}$.

Note: Operating Conditions apply.

Table 17 is valid under the following conditions: $V_{\text{DDP}} \ge 3.0 \text{ V}$; V_{DDP} typ. 3.3 V; $V_{\text{DDP}} \le 4.5 \text{ V}$

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	C _{IO} CC	_	-	10	pF	not subject to production test
Input Hysteresis ²⁾	HYS CC	0.07 x V _{DDP}	-	-	V	R _s = 0 Ohm
Absolute input leakage current on pins of analog ports ³⁾	I _{OZ1} CC	-	10	200	nA	$V_{\rm IN}$ > $V_{\rm SS}$; $V_{\rm IN}$ < $V_{\rm DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins. ³⁾¹⁾⁴⁾	I _{OZ2} CC	-	0.2	2.5	μA	$\begin{array}{l} T_{\rm J} \leq 110 ~^{\circ}{\rm C}; \\ V_{\rm IN} > V_{\rm SS} ~; \\ V_{\rm IN} < V_{\rm DDP} \end{array}$
		_	0.2	8	μA	$T_{J} \leq 150 \text{ °C};$ $V_{IN} > V_{SS};$ $V_{IN} < V_{DDP}$
Pull Level Force Current ⁵⁾	$ I_{PLF} $ SR	150	_	_	μA	$V_{\rm IN} \ge V_{\rm IHmin}(pull down) ; V_{\rm IN} \le V_{\rm ILmax}(pull up)$
Pull Level Keep Current ⁶⁾	I _{PLK} SR	_	_	10	μA	$V_{\rm IN} \ge V_{\rm IHmin}(pull up); V_{\rm IN} \le V_{\rm ILmax}(pull down)$
Input high voltage (all except XTAL1)	$V_{IH} SR$	0.7 x V _{DDP}	-	V _{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	-	0.3 x V _{DDP}	V	

Table 17 DC Characteristics for Lower Voltage Range



4.7.2 Definition of Internal Timing

The internal operation of the XC223xN is controlled by the internal system clock f_{SYS} .

Because the system clock signal $f_{\rm SYS}$ can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate $f_{\rm SYS}$. This must be considered when calculating the timing for the XC223xN.



Figure 19 Generation Mechanisms for the System Clock

Note: The example of PLL operation shown in **Figure 19** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).



The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.

The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 20**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS} . The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

 D_{Tmax} [ns] = ±(220 / (K2 × f_{SYS}) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of $\mathbf{T} \times TCS$ the accumulated jitter D_T is determined by:

 D_{T} [ns] = $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

 f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

 $D_{max} = \pm (220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

 $\mathsf{D}_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$

= 5.97 × [0.768 × 2 / 26.39 + 0.232]

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

 $D_{max} = \pm (220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

 $\begin{array}{l} \mathsf{D}_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) \, / \, (0.83 \times 33 - 1) + 0.058 \times 2] \\ = 7.63 \times [0.884 \times 2 \, / \, 26.39 + 0.116] \end{array}$



4.7.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 30 is valid under the following conditions: C_L = 20 pF; *SSC*= master ; voltage_range= upper

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	1	Test Condition
Slave select output SELO active to first SCLKOUT transmit edge	t ₁ CC	t _{SYS} - 8 ¹⁾	-	-	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t ₂ CC	t _{SYS} - 6 ¹⁾	-	-	ns	
Data output DOUT valid time	t ₃ CC	-6	-	9	ns	
Receive data input setup time to SCLKOUT receive edge	t ₄ SR	31	-	-	ns	
Data input DX0 hold time from SCLKOUT receive edge	t ₅ SR	-4	-	-	ns	

Table 30 USIC SSC Master Mode Timing for Upper Voltage Range

1) $t_{SYS} = 1 / f_{SYS}$

Table 31 is valid under the following conditions: C_L = 20 pF; *SSC*= master ; voltage_range= lower



XC2232N, XC2234N, XC2236N, XC2238N XC2000 Family / Value Line

Package and Reliability

Package Outlines



Figure 28 PG-LQFP-64-6 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": http://www.infineon.com/packages



Package and Reliability

5.2 Thermal Considerations

When operating the XC223xN in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta,IA}$

The internal power consumption is defined as

 $P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as $P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}}-V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- · Reduce the system frequency
- · Reduce the number of output pins
- Reduce the load on active output drivers