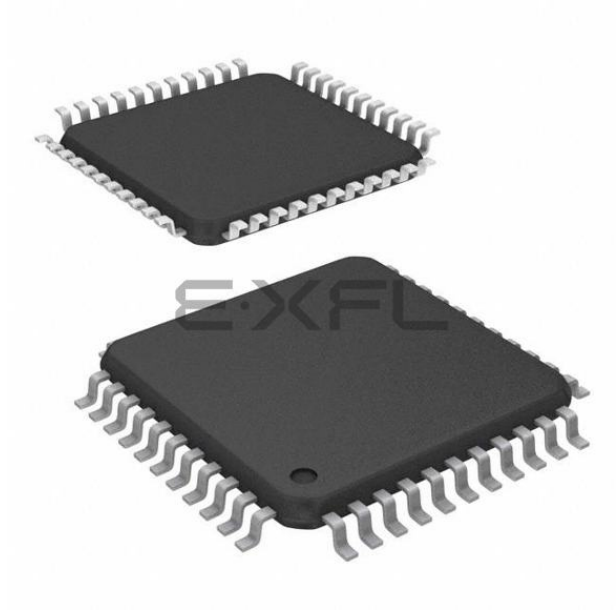

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v662fbc-557

5. Pinning information

5.1 Pinning

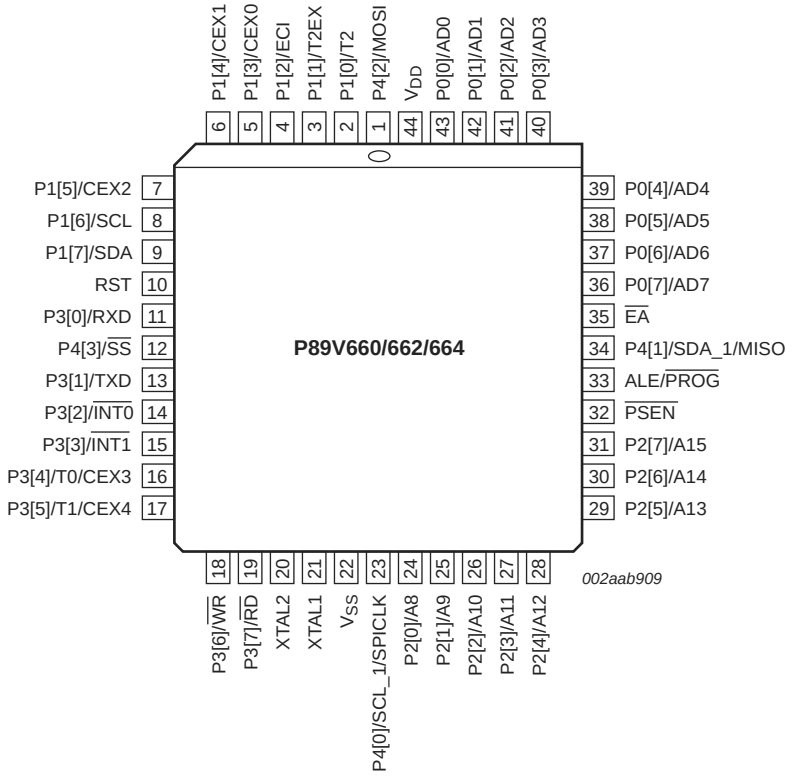

Fig 2. PLCC44 pin configuration

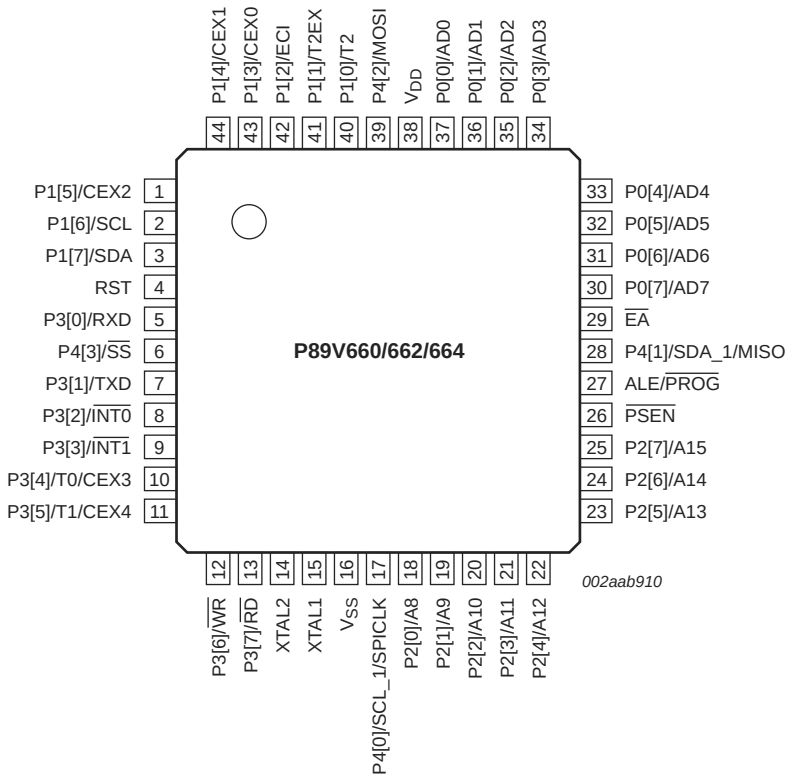

Fig 3. TQFP44 pin configuration

Table 3. Pin description *…continued*

Symbol	Pin		Type	Description
	TQFP44	PLCC44		
ALE/$\overline{\text{PROG}}$	27	33	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input ($\overline{\text{PROG}}$) for flash programming. Normally the ALE[2] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[3] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to '1', ALE is disabled.
XTAL1	15	21	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	14	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	38	44	I	**Power supply**
V_{SS}	16	22	I	**Ground**

[1] Port 1, 2, 3, and 4 enter the bidirectional state (except the I²C pins) with a weak pull-up after reset. In this state, the pins can be used as inputs or outputs. See the *80C51 Family Hardware Description* for details of the port structure.

A reset does not assert the strong pull-up for two clock cycles for these ports which normally occurs when the port transitions from a LOW to a HIGH state. You must first write a zero, then a logic one to enable the strong pull-up for two clock cycles.

[2] ALE loading issue: When ALE pin experiences higher loading (>30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3 kΩ to 50 kΩ to V_{DD}, e.g., for ALE pin.

[3] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

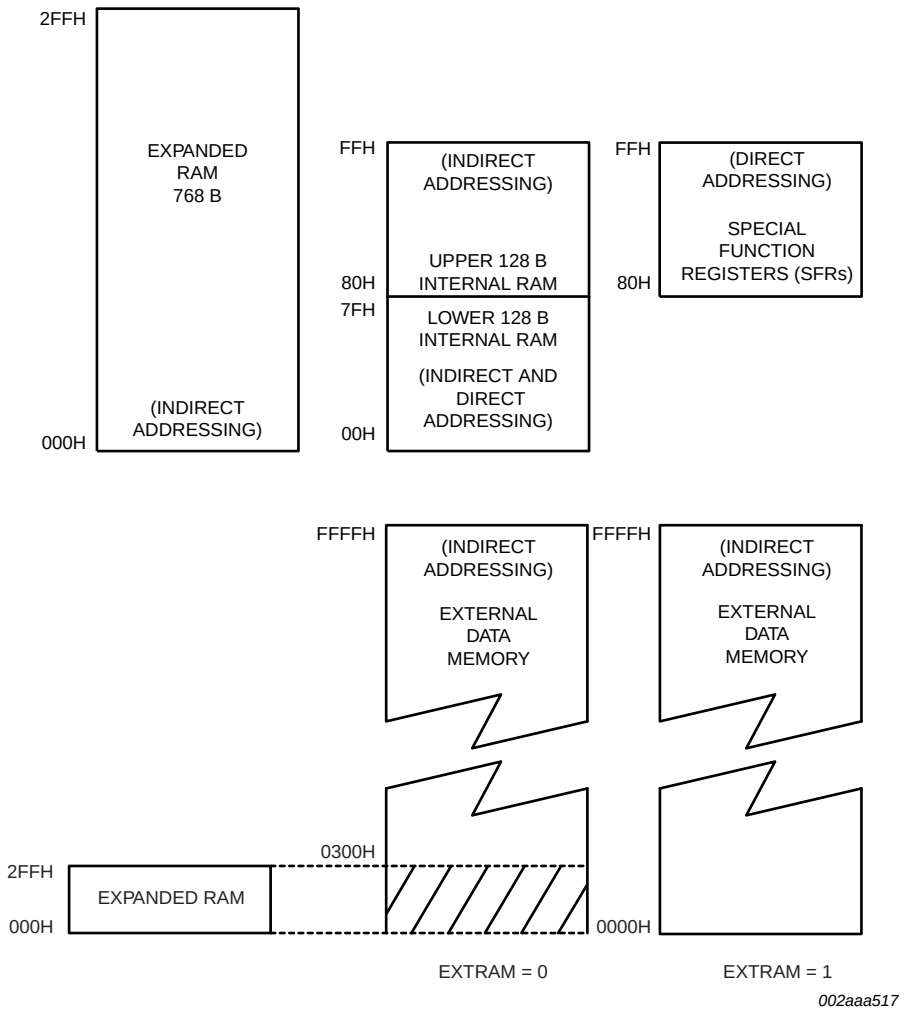

Fig 4. Internal and external data memory structure

6.2.2 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1 (see Figure 5).

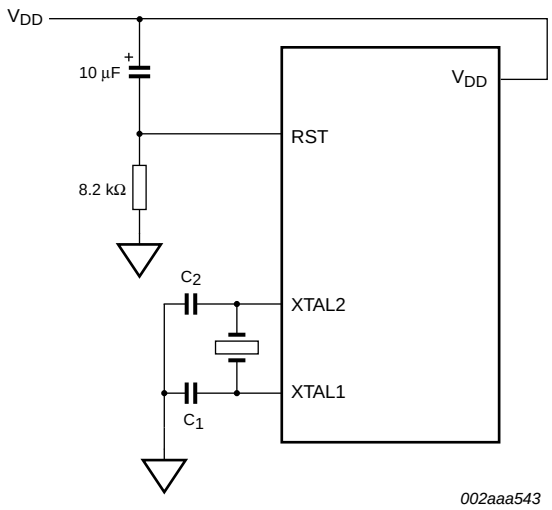

Fig 6. Power-on reset circuit

6.3 Flash memory

6.3.1 Flash organization

The P89V660/662/664 program memory consists of a 16/32/64 kB block for user code. The flash can be read or written in bytes and can be erased in 128 pages. A chip erase function will erase the entire user code memory and its associated security bits. There are three methods of erasing or programming the flash memory that may be used. First, the flash may be programmed or erased in the end-user application by calling LOW-state routines through a common IAP entry point. Second, the on-chip ISP bootloader may be invoked. This ISP bootloader will, in turn, call LOW-state routines through the same common entry point that can be used by the end-user application. Third, the flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device.

6.3.2 Features

- Flash internal program memory with 128-byte page erase.
- Internal Boot block, containing LOW-state IAP routines available to user code.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Default loader providing ISP via the serial port, located in upper end of program memory.
- Programming and erase over the full operating voltage range.
- Read/Programming/Erase using ISP/IAP.
- Programming with industry-standard commercial programmers.
- 10000 typical erase/program cycles for each byte.
- 100 year minimum data retention.

based on the oscillator frequency. The ISP feature requires that an initial character (an uppercase U) be sent to the P89V660/662/664 to establish the baud rate. The ISP firmware provides auto-echo of received characters. Once baud rate initialization has been performed, the ISP firmware will only accept Intel Hex-type records. Intel Hex records consist of ASCII characters used to represent hexadecimal values and are summarized below:

:NNAAAARRDD..DDCC<crlf>

In the Intel Hex record, the ‘NN’ represents the number of data bytes in the record. The P89V660/662/664 will accept up to 32 data bytes. The ‘AAAA’ string represents the address of the first byte in the record. If there are zero bytes in the record, this field is often set to 0000. The ‘RR’ string indicates the record type. A record type of ‘00’ is a data record. A record type of ‘01’ indicates the end-of-file mark. In this application, additional record types will be added to indicate either commands or data for the ISP facility.

The maximum number of data bytes in a record is limited to 32 (decimal). ISP commands are summarized in Table 11. As a record is received by the P89V660/662/664, the information in the record is stored internally and a checksum calculation is performed. The operation indicated by the record type is not performed until the entire record has been received. Should an error occur in the checksum, the P89V660/662/664 will send an ‘X’ out the serial port indicating a checksum error. If the checksum calculation is found to match the checksum in the record, then the command will be executed. In most cases, successful reception of the record will be indicated by transmitting a ‘.’ character out the serial port.

Table 11. ISP hex record formats

Record type	Command/data function
00	Program User Code Memory :nnaaaa00dd..ddcc Where: nn = number of bytes to program aaaa = address dd..dd = data bytes cc = checksum Example: :0900000001020304050607080 9CA
01	End of File (EOF), no operation :xxxxxx01cc Where: xxxxxx = required field but value is a ‘don’t care’ cc = checksum Example: :00000001FF
02	not used

Table 12. IAP function calls *…continued*

IAP function	IAP call parameters
Erase Status bit and Boot vector	**Input parameters:** R1 = 04H or 84H (WDT feed) DPL = don't care DPH = don't care **Return parameter(s):** ACC = 00 = pass ACC = !00 = fail
Program Security bits	**Input parameters:** R1 = 05H or 85H (WDT feed) DPL = 00H = security bit 1 DPL = 01H = security bit 2 DPL = 02H = security bit 3 **Return parameter(s):** ACC = 00 = pass ACC = !00 = fail
Program Status bit, Boot vector, 6x/12x bit	**Input parameters:** R1 = 06H or 86H (WDT feed) DPL = 00H = program Status bit DPL = 01H = program Boot vector DPL = 02H = 6x/12x bit ACC = Boot vector value to program **Return parameter(s):** ACC = 00 = pass ACC = !00 = fail
Read Security bits, Status bit, Boot vector	**Input parameters:** ACC = 07H or 87H (WDT feed) DPL = 00H = security bits DPL = 01H = Status bit DPL = 02H = Boot vector **Return parameter(s):** ACC = 00 SoftICE S/N-match 0 SB 0 DBL_CLK
Erase page	**Input parameters:** R1 = 08H or 88H (WDT feed) DPH = page address high byte DPL = page address low byte **Return parameter(s):** ACC = 00 = pass ACC = !00 = fail

6.4 I2C-bus interface

The I2C-bus uses two wires, Serial Clock (SCL) and Serial Data (SDA) to transfer information between devices connected to the bus, and has the following features:

- Bidirectional data transfer between masters and slaves

6.4.1 I2C-bus data register

S1DAT register contains the data to be transmitted or the data received. The CPU can read and write to this 8-bit register while it is not in the process of shifting a byte. Thus this register should only be accessed when the SI bit is set. Data in S1DAT remains stable as long as the SI bit is set. Data in S1DAT is always shifted from right to left: the first bit to be transmitted is the MSB (bit 7), and after a byte has been received, the first bit of received data is located at the MSB of S1DAT.

6.4.2 I2C-bus slave address register

The S1ADR register is readable and writable, and is only used when the I2C-bus interface is set to slave mode. In master mode, this register has no effect. The LSB of S1ADR is general call bit. When this bit is set, the general call address (00H) is recognized.

Table 13. I2C-bus slave address register (S1ADR - address DBH) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	S1ADR.6	S1ADR.5	S1ADR.4	S1ADR.3	S1ADR.2	S1ADR.1	S1ADR.0	S1GC
Reset	0	0	0	0	0	0	0	0

Table 14. I2C-bus slave address register (S1ADR - address DBH) bit description

Bit	Symbol	Description
7:1	S1ADR7:1	7 bit own slave address. When in master mode, the contents of this register has no effect.
0	S1GC	General call bit. When set, the general call address (00H) is recognized, otherwise it is ignored.

6.4.3 I2C-bus control register

The CPU can read and write this register. There are two bits are affected by hardware: the SI bit and the STO bit. The SI bit is set by hardware and the STO bit is cleared by hardware.

CR2:0 determines the SCL source and frequency when the I2C-bus is in master mode. In slave mode these bits are ignored and the bus will automatically synchronize with any clock frequency up to 100 kHz from the master I2C-bus device. Timer 1 should be programmed by the user in 8 bit auto-reload mode (Mode 2) when used as the SCL source. See Table 17.

The STA bit is START flag. Setting this bit causes the I2C-bus interface to enter master mode and attempt transmitting a START condition or transmitting a repeated START condition when it is already in master mode.

The STO bit is STOP flag. Setting this bit causes the I2C-bus interface to transmit a STOP condition in master mode, or recovering from an error condition in slave mode.

If the STA and STO are both set, then a STOP condition is transmitted to the I2C-bus if it is in master mode, and transmits a START condition afterwards. If it is in slave mode, an internal STOP condition will be generated, but it is not transmitted to the bus.

6.6.2 Auto-reload mode (up or down-counter)

In the 16-bit auto-reload mode, Timer 2 can be configured as either a timer or counter (via C/$\overline{T}$2 in T2CON), then programmed to count up or down. The counting direction is determined by bit DCEN (Down-counter Enable) which is located in the T2MOD register (see Table 34 and Table 35). When reset is applied, DCEN = 0 and Timer 2 will default to counting up. If the DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 19 shows Timer 2 counting up automatically (DCEN = 0).

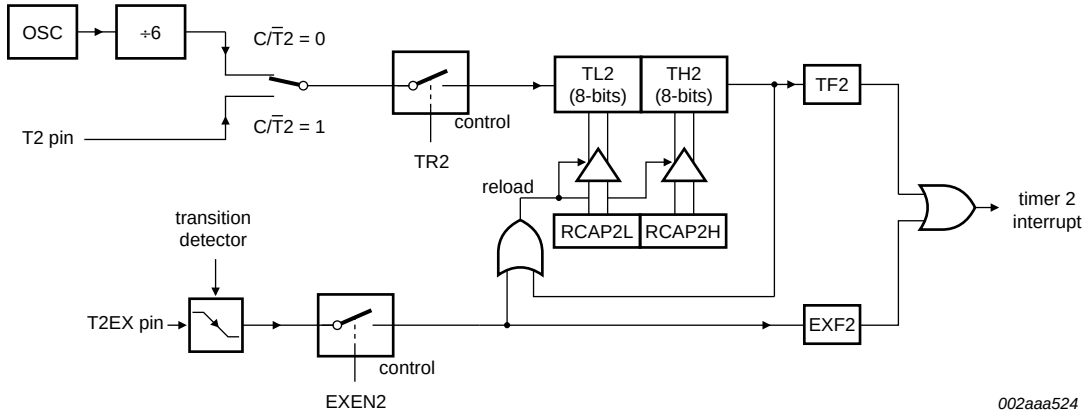

Fig 19. Timer 2 in Auto-reload mode (DCEN = 0)

In this mode, there are two options selected by bit EXEN2 in T2CON register. If EXEN2 = 0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

Auto reload frequency when Timer 2 is counting up can be determined from this formula:

$$\frac{SupplyFrequency}{65536 - (RCAP2H, RCAP2L)} \quad (1)$$

Where SupplyFrequency is either f_{osc} (C/$\overline{T2}$ = 0) or frequency of signal on T2 pin (C/$\overline{T2}$ = 1).

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 is ‘1’.

Microcontroller’s hardware will need three consecutive machine cycles in order to recognize falling edge on T2EX and set EXF2 = 1: in the first machine cycle pin T2EX has to be sampled as ‘1’; in the second machine cycle it has to be sampled as ‘0’, and in the third machine cycle EXF2 will be set to ‘1’.

SPICLK pin is the clock output and input for the master and slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin on the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPIF flag is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the SPI interrupt enable bit, ES3, are both set.

An external master drives the Slave Select input pin, $\overline{SS}$ LOW to select the SPI module as a slave. If $\overline{SS}$ has not been driven LOW, then the slave SPI unit is not active and the MOSI pin can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock. Figure 24 and Figure 25 show the four possible combinations of these two bits.

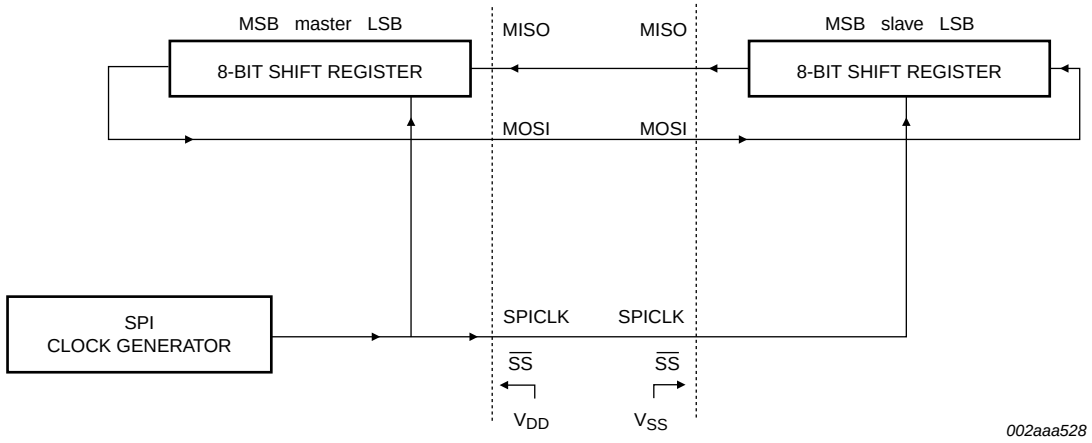

Fig 23. SPI master-slave interconnection

Table 40. SPCR - SPI control register (address D5H) bit allocation
Bit addressable; Reset source(s): any reset; Reset value: 0000 0000B

Bit	7	6	5	4	3	2	1	0
Symbol	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Table 41. SPCR - SPI control register (address D5H) bit description

Bit	Symbol	Description
7	SPIE	If both SPIE and ES3 are set to one, SPI interrupts are enabled.
6	SPEN	SPI enable bit. When set enables SPI.
5	DORD	Data transmission order. 0 = MSB first; 1 = LSB first in data transmission.
4	MSTR	Master/slave select. 1 = master mode, 0 = slave mode.
3	CPOL	Clock polarity. 1 = SPICLK is high when idle (active LOW), 0 = SPICLK is low when idle (active HIGH).

Table 50. CCAPMn - PCA modules compare/capture register (address CCAPM0 0C2H, CCAPM1 0C3H, CCAPM2 0C4H, CCAPM3 0C5H, CCAPM4 0C6H) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Table 51. CCAPMn - PCA modules compare/capture register (address CCAPM0 0C2H, CCAPM1 0C3H, CCAPM2 0C4H, CCAPM3 0C5H, CCAPM4 0C6H) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
5	CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
4	CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
3	MATn	Match. When MATn = 1 a match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
2	TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module’s compare/capture register causes the CEXn pin to toggle.
1	PWMn	Pulse Width Modulation mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
0	ECCFn	Enable CCF Interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

Table 52. PCA module modes (CCAPMn register)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module function
0	0	0	0	0	0	0	no operation
x	1	0	0	0	0	x	16-bit capture by a positive-edge trigger on CEXn
x	0	1	0	0	0	x	16-bit capture by a negative-edge trigger on CEXn
x	1	1	0	0	0	x	16-bit capture by any transition on CEXn
1	0	0	1	0	0	x	16-bit software timer
1	0	0	1	1	0	x	16-bit high-speed output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	x	0	x	watchdog timer

6.10.1 PCA capture mode

To use one of the PCA modules in the capture mode (Figure 28) either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module’s capture registers (CCAPnL and CCAPnH).

value in the module's CCAPnL SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPnL is reloaded with the value in CCAPnH. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

6.10.5 PCA watchdog timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a Watchdog. However, this module can still be used for other modes if the Watchdog is not needed. Figure 31 shows a diagram of how the Watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

user's software then must periodically change (CCAP4H,CCAP4L) to keep a match from occurring with the PCA timer (CH,CL). This code is given in the WATCHDOG routine shown above.

In order to hold off the reset, the user has three options:

1. Periodically change the compare value so it will never match the PCA timer.
2. Periodically change the PCA timer value so it will never match the compare values.
3. Disable the Watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

```
;CALL the following WATCHDOG subroutine periodically.
   CLR    EA           ;Hold off interrupts
   MOV    CCAP4L,#00   ;Next compare value is within 255 counts of
                        current PCA timer value
   MOV    CCAP4H,CH
   SETB   EA           ;Re-enable interrupts
   RET
```

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the Watchdog will keep getting reset. Thus, the purpose of the Watchdog would be defeated. Instead, call this subroutine from the main program within 2^{16} count of the PCA timer.

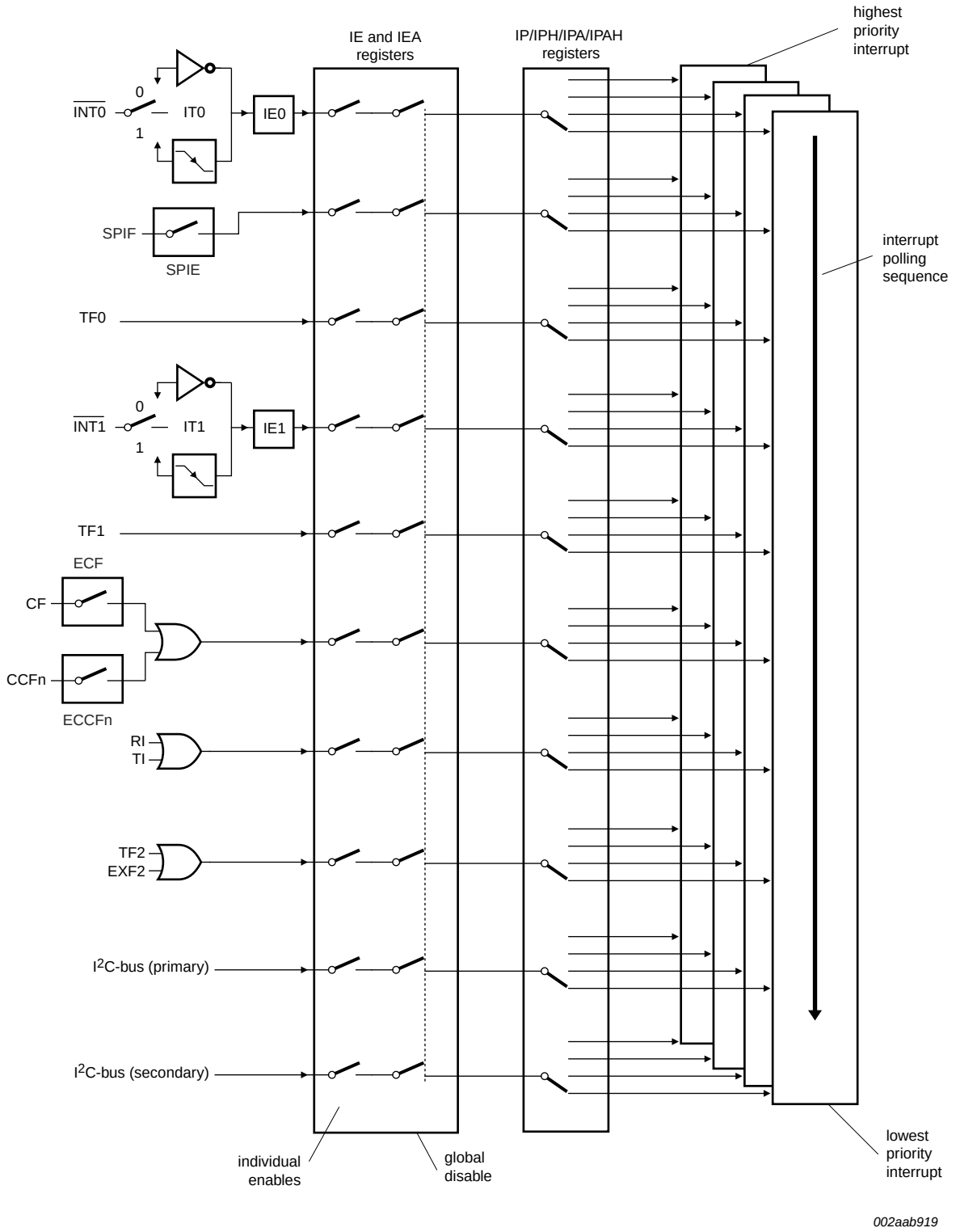

Fig 32. Interrupt structure

6.13.1 Idle mode

Idle mode is entered setting the IDL bit in the PCON register. In Idle mode, the program counter is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits Idle mode through either a system interrupt or a hardware reset. Exiting Idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits Idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the Idle mode. A hardware reset starts the device similar to a power-on reset.

6.13.2 Power-down mode

The Power-down mode is entered by setting the PD bit in the PCON register. In the Power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during Power-down, the minimum V_{DD} level is 2.0 V.

The device exits Power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits Power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal restored to logic V_{IH}, the interrupt service routine program execution resumes beginning at the instruction immediately following the instruction which invoked Power-down mode. A hardware reset starts the device similar to power-on reset.

To exit properly out of Power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

Table 67. Power-saving modes

Mode	Initiated by	State of MCU	Exited by
Idle mode	Software (Set IDL bit in PCON) MOV PCON, #01H	CLK is running. Interrupts, serial port and timers/counters are active. Program Counter is stopped. ALE and $\overline{\text{PSEN}}$ signals at a HIGH-state during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked Idle mode. A hardware reset restarts the device similar to a power-on reset.
Power-down mode	Software (Set PD bit in PCON) MOV PCON, #02H	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and $\overline{\text{PSEN}}$ signals at a LOW-state during power-down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits Power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Power-down mode. A hardware reset restarts the device similar to a power-on reset.

7. Limiting values

Table 69. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_I	input voltage	on $\overline{EA}$ pin to V_{SS}	–0.5	14	V
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	15	mA
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 70. Static characteristics

T_{amb} = –40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1]	10000	-	-	cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1]	100	-	-	years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1]	100 + I_{DD}	-	-	mA
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		–0.5	-	$0.2V_{DD}$ – 0.1	V
V_{IL}	LOW-level input voltage	SCL, SDA		–0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA, XTAL1, RST		$0.2V_{DD}$ + 0.9	-	V_{DD} + 0.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA		$0.7V_{DD}$	-	V_{DD} + 0.5	V
		XTAL1, RST		$0.7V_{DD}$	-	6.0	V
V_{OL}	LOW-level output voltage	V_{DD} = 4.5 V, except, $\overline{PSEN}$, ALE, SCL, SDA	[2][3][4]				
		I_{OL} = 1.6 mA		-	-	0.4	V
		V_{DD} = 4.5 V, ALE, $\overline{PSEN}$					
		I_{OL} = 3.2 mA		-	-	0.45	V
		V_{DD} = 4.5 V, SCL, SDA					
		I_{OL} = 3.0 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	V_{DD} = 4.5 V, ports 1, 2, 3, 4	[5]				
		I_{OH} = –30 μA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V, Port 0 in External Bus mode, ALE, $\overline{PSEN}$					
		I_{OH} = –3.2 mA		V_{DD} – 0.7	-	-	V
I_{IL}	LOW-level input current	V_I = 0.4 V, ports 1, 2, 3, 4		–1	-	–75	μA

9.1 Explanation of symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A — Address

C — Clock

D — Input data

H — Logic level HIGH

I — Instruction (program memory contents)

L — Logic level LOW or ALE

P — $\overline{\text{PSEN}}$

Q — Output data

R — $\overline{\text{RD}}$ signal

T — Time

V — Valid

W — $\overline{\text{WR}}$ signal

X — No longer a valid logic level

Z — High impedance (Float)

Example:

t_{AVLL} = Address valid to ALE LOW time

t_{LLPL} = ALE LOW to $\overline{\text{PSEN}}$ LOW time

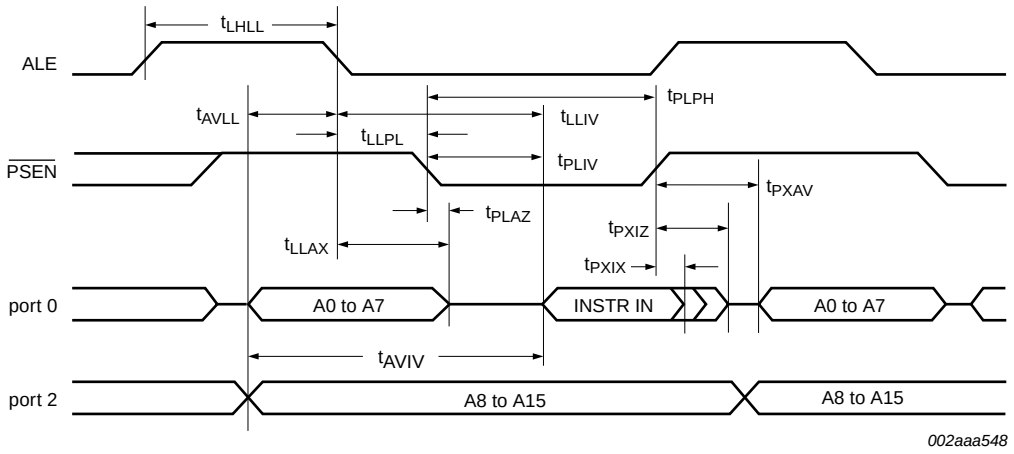

Fig 36. External program memory read cycle

Table 72. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

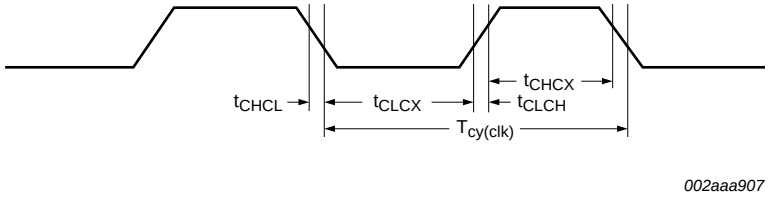

Fig 39. External clock drive waveform

Table 73. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 50$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns

11. Abbreviations

Table 76. Acronym list

Acronym	Description
ALE	Address Latch Enabled
CPU	Central Processing Unit
DUT	Device Under Test
EPROM	Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
MCU	Microcontroller Unit
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 77. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89V660_662_664 v.3.1	20111017	Product data sheet	-	P89V660_662_664 v.3
Modifications:	• Table 3 “Pin description”: Added Table note 1. • Updated Equation 2 and Equation 3. • Removed type numbers P89V660FA and P89V660FBC from Table 1 and Table 2 due to EOL.			
P89V660_662_664 v.3	20081110	Product data sheet	-	P89V660_662_664 v.2
Modifications:	• Section 2.2 “Additional features”: corrected 6-clock/12-clock mode information.			
P89V660_662_664 v.2	20080129	Product data sheet	-	P89V660_662_664 v.1
P89V660_662_664 v.1	20070502	Product data sheet	-	-

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