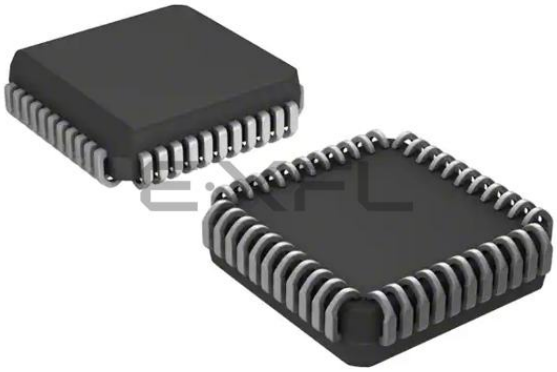

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v664fa-512

- Idle mode

2.3 Comparison to the P89C660/662/664 devices

- **SPI interface**. The P89V660/662/664 devices include an SPI interface that was not present on the P89C660/662/664 devices.
- **Dual I2C-bus interfaces**. The P89V660/662/664 devices have two I²C-bus interfaces. The P89C660/662/664 devices have one.
- **More I/O pins**. The P89V660/662/664 devices have an additional four-bit I/O port, Port 4.
- The **6x/12x mode** on theP89V660/662/664 devices is **programmable** and erasable **using ISP** and IAP as well as parallel programmer mode. The P89C660/662/664 devices could only be switched using parallel programmer mode.
- **Smaller block sizes**. The smallest block size on the P89C660/662/664 devices was 8 kB. The P89V660/662/664 devices have a page size of 128 B. These small pages can be erased and reprogrammed using IAP function calls making use of the code memory for non-volatile data storage practical. Each page erase is 30 ms or less. The IAP and ISP code in P89V660/662/664 devices support these 128-byte page operations. In addition, the IAP and ISP code uses multiple page erase operations to emulate the erasing of the larger block sizes (8 kB and 16 kB to maintain firmware compatibility).
- **Status bit versus Status byte**. The P89V660/662/664 devices used a Status byte to control the automatic entry into ISP mode following a reset. On the P89V660/662/664 devices this has changed to a single Status bit. Since the ISP entry was based on the zero/non-zero value of the Status byte this is an almost identical operation on the P89V660/662/664 devices.
- **Faster block erase**. The erase time for the entire user code memory of the P89V660/662/664 devices is 150 ms.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89V662FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89V662FBC	TQFP44	plastic thin quad flat package; 44 leads; body 10 × 10 × 1.0 mm	SOT376-1
P89V664FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89V664FBC	TQFP44	plastic thin quad flat package; 44 leads; body 10 × 10 × 1.0 mm	SOT376-1

5. Pinning information

5.1 Pinning

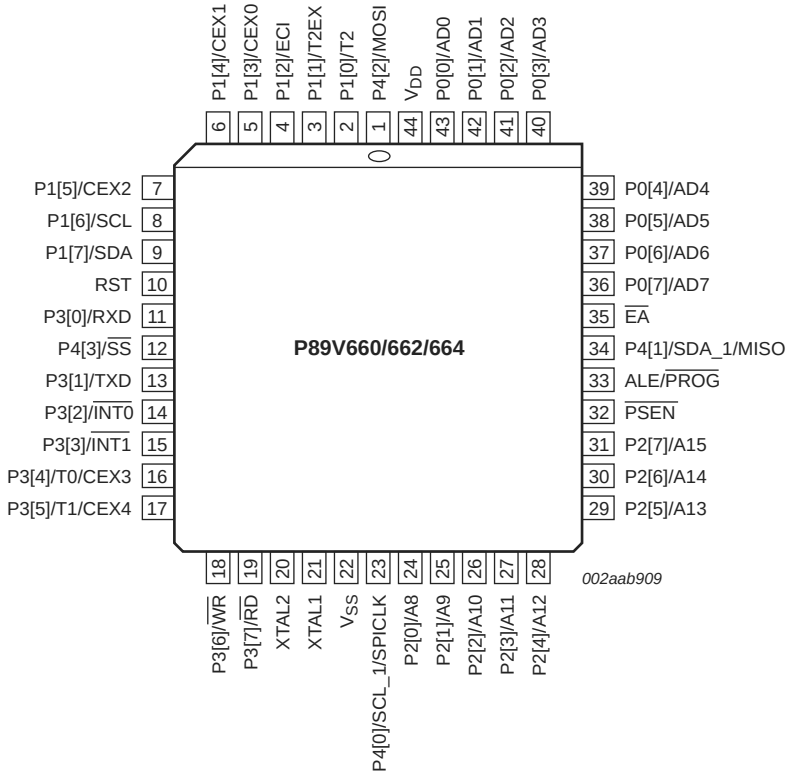


Fig 2. PLCC44 pin configuration

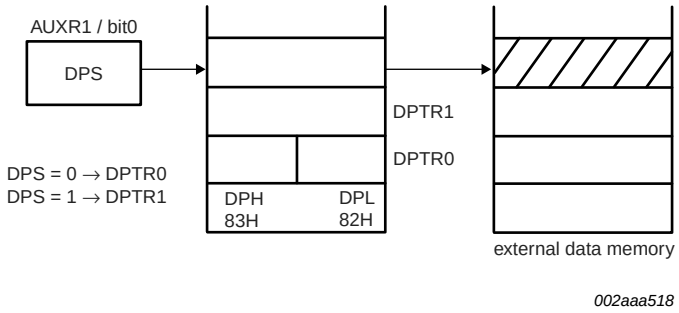


Fig 5. Dual data pointer organization

Table 8. AUXR1 - Auxiliary register 1 (address A2H) bit allocation
Not bit addressable; Reset value 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	GF2	0	-	DPS

Table 9. AUXR1 - Auxiliary register 1 (address A2H) bit description

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Should be set to ‘0’ by user programs.
3	GF2	General purpose user-defined flag.
2	0	This bit contains a hard-wired ‘0’. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to ‘0’ by user programs.
0	DPS	Data pointer select. Chooses one of two Data Pointers for use by the program. See text for details.

6.2.3 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins high. Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held high long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 6.

During initial power the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

Following a reset condition, under normal conditions, the MCU will start executing code from address 0000H in the user’s code memory. However if either the $\overline{\text{PSEN}}$ pin was low when reset was exited, or the Status Bit was set = 1, the MCU will start executing code from the boot address. The boot address is formed using the value of the boot vector as the high byte of the address and 00H as the low byte.

based on the oscillator frequency. The ISP feature requires that an initial character (an uppercase U) be sent to the P89V660/662/664 to establish the baud rate. The ISP firmware provides auto-echo of received characters. Once baud rate initialization has been performed, the ISP firmware will only accept Intel Hex-type records. Intel Hex records consist of ASCII characters used to represent hexadecimal values and are summarized below:

:NNAAAARRDD..DDCC<crlf>

In the Intel Hex record, the ‘NN’ represents the number of data bytes in the record. The P89V660/662/664 will accept up to 32 data bytes. The ‘AAAA’ string represents the address of the first byte in the record. If there are zero bytes in the record, this field is often set to 0000. The ‘RR’ string indicates the record type. A record type of ‘00’ is a data record. A record type of ‘01’ indicates the end-of-file mark. In this application, additional record types will be added to indicate either commands or data for the ISP facility.

The maximum number of data bytes in a record is limited to 32 (decimal). ISP commands are summarized in Table 11. As a record is received by the P89V660/662/664, the information in the record is stored internally and a checksum calculation is performed. The operation indicated by the record type is not performed until the entire record has been received. Should an error occur in the checksum, the P89V660/662/664 will send an ‘X’ out the serial port indicating a checksum error. If the checksum calculation is found to match the checksum in the record, then the command will be executed. In most cases, successful reception of the record will be indicated by transmitting a ‘.’ character out the serial port.

Table 11. ISP hex record formats

Record type	Command/data function
00	Program User Code Memory :nnaaaa00dd..ddcc Where: nn = number of bytes to program aaaa = address dd..dd = data bytes cc = checksum Example: :0900000001020304050607080 9CA
01	End of File (EOF), no operation :xxxxxx01cc Where: xxxxxx = required field but value is a ‘don’t care’ cc = checksum Example: :00000001FF
02	not used

6.4.1 I2C-bus data register

S1DAT register contains the data to be transmitted or the data received. The CPU can read and write to this 8-bit register while it is not in the process of shifting a byte. Thus this register should only be accessed when the SI bit is set. Data in S1DAT remains stable as long as the SI bit is set. Data in S1DAT is always shifted from right to left: the first bit to be transmitted is the MSB (bit 7), and after a byte has been received, the first bit of received data is located at the MSB of S1DAT.

6.4.2 I2C-bus slave address register

The S1ADR register is readable and writable, and is only used when the I2C-bus interface is set to slave mode. In master mode, this register has no effect. The LSB of S1ADR is general call bit. When this bit is set, the general call address (00H) is recognized.

Table 13. I2C-bus slave address register (S1ADR - address DBH) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	S1ADR.6	S1ADR.5	S1ADR.4	S1ADR.3	S1ADR.2	S1ADR.1	S1ADR.0	S1GC
Reset	0	0	0	0	0	0	0	0

Table 14. I2C-bus slave address register (S1ADR - address DBH) bit description

Bit	Symbol	Description
7:1	S1ADR7:1	7 bit own slave address. When in master mode, the contents of this register has no effect.
0	S1GC	General call bit. When set, the general call address (00H) is recognized, otherwise it is ignored.

6.4.3 I2C-bus control register

The CPU can read and write this register. There are two bits are affected by hardware: the SI bit and the STO bit. The SI bit is set by hardware and the STO bit is cleared by hardware.

CR2:0 determines the SCL source and frequency when the I2C-bus is in master mode. In slave mode these bits are ignored and the bus will automatically synchronize with any clock frequency up to 100 kHz from the master I2C-bus device. Timer 1 should be programmed by the user in 8 bit auto-reload mode (Mode 2) when used as the SCL source. See Table 17.

The STA bit is START flag. Setting this bit causes the I2C-bus interface to enter master mode and attempt transmitting a START condition or transmitting a repeated START condition when it is already in master mode.

The STO bit is STOP flag. Setting this bit causes the I2C-bus interface to transmit a STOP condition in master mode, or recovering from an error condition in slave mode.

If the STA and STO are both set, then a STOP condition is transmitted to the I2C-bus if it is in master mode, and transmits a START condition afterwards. If it is in slave mode, an internal STOP condition will be generated, but it is not transmitted to the bus.

Table 17. I²C-bus clock rates *...continued*

CR2:0	Bit frequency at f_{osc}					
	6-clock mode		12-clock mode		f_{osc} divided by	
	6 MHz	12 MHZ	6 MHz	12 MHz	6X	12X
101	100	200	50	100	60	120
110	200	400	100	200	30	60
111	0.49 < 62.5	0.98 < 50.0	0.24 < 62.5	0.49 < 62.5	48 x (Timer 1 reload)	96 x (Timer 1 reload)

6.4.4 I²C-bus status register

This is a read-only register. It contains the status code of the I²C-bus interface. The least three bits are always 0. There are 26 possible status codes. When the code is F8H, there is no relevant information available and SI bit is not set. All other 25 status codes correspond to defined I²C-bus states. When any of these states entered, the SI bit will be set. Refer to Table 22 to Table 25 for details.

Table 18. I²C-bus status register (S1STA - address D9H) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SC.4	SC.3	SC.2	SC.1	SC.0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 19. I²C-bus status register (S1STA - address D9H) bit description

Bit	Symbol	Description
7:3	SC[4:0]	I²C-bus Status code.
2:0	-	Reserved, are always set to 0.

6.4.5 I²C-bus operation modes

6.4.5.1 Master transmitter mode

In this mode data is transmitted from master to slave. Before the Master Transmitter mode can be entered, S1CON must be initialized as follows:

Table 20. I²C-bus control register (S1CON - address D8H)

Bit	7	6	5	4	3	2	1	0
Symbol	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
Value	bit rate	1	0	0	0	x	bit rate	bit rate

CR2:0 define the bit rate (See Table 17). ENS1 must be set to 1 to enable the I²C-bus function. If the AA bit is 0, it will not acknowledge its own slave address or the general call address in the event of another device becoming master of the bus and it can not enter slave mode. STA, STO, and SI bits must be cleared to 0.

The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case, the data direction bit (R/W) will be logic 0 indicating a write. Data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

Table 25. Slave transmitter mode *…continued*

Status code (S1STA)	Status of the I²C-bus hardware	Application software response					Next action taken by I²C-bus hardware
		to/from S1DAT	to S1CON				
			STA	STO	SI	AA	
C0H	Data byte in S1DAT has been transmitted; NOT ACK has been received.	No S1DAT action or	0	0	0	0	Switched to not addressed SLA mode; no recognition of own SLA or General call address.
		no S1DAT action or	0	0	0	1	Switched to not addressed SLA mode; Own slave address will be recognized; General call address will be recognized if S1ADR.0 = 1.
		no S1DAT action or	1	0	0	0	Switched to not addressed SLA mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		no S1DAT action	1	0	0	1	Switched to not addressed SLA mode; Own slave address will be recognized; General call address will be recognized if S1ADR.0 = 1. A START condition will be transmitted when the bus becomes free.
C8H	Last data byte in S1DAT has been transmitted (AA = 0); ACK has been received.	No S1DAT action or	0	0	0	0	Switched to not addressed SLA mode; no recognition of own SLA or General call address.
		no S1DAT action or	0	0	0	1	Switched to not addressed SLA mode; Own slave address will be recognized; General call address will be recognized if S1ADR.0 = 1.
		no S1DAT action or	1	0	0	0	Switched to not addressed SLA mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		no S1DAT action	1	0	0	1	Switched to not addressed SLA mode; Own slave address will be recognized; General call address will be recognized if S1ADR.0 = 1. A START condition will be transmitted when the bus becomes free.

6.5 Timers/counters 0 and 1

The two 16-bit Timer/Counter registers: Timer 0 and Timer 1 can be configured to operate either as timers or event counters (see Table 26 and Table 27).

In the ‘Timer’ function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of six oscillator periods, the count rate is $\frac{1}{6}$ of the oscillator frequency.

Table 38. SCON - Serial port control register (address 98H) bit description *…continued*

Bit	Symbol	Description
3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is undefined.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or approximately halfway through the stop bit time in all other modes. (See SM2 for exceptions). Must be cleared by software.

Table 39. SCON - Serial port control register (address 98H) SM0/SM1 mode definition

SM0, SM1	UART mode	Baud rate
0 0	0: shift register	CPU clock / 6
0 1	1: 8-bit UART	variable
1 0	2: 9-bit UART	CPU clock / 32 or CPU clock / 16
1 1	3: 9-bit UART	variable

6.7.5 Framing error

Framing error (FE) is reported in the SCON.7 bit if SMOD0 (PCON.6) = 1. If SMOD0 = 0, SCON.7 is the SM0 bit for the UART, it is recommended that SM0 is set up before SMOD0 is set to ‘1’.

6.7.6 More about UART mode 1

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset to align its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated.

6.7.7 More about UART modes 2 and 3

Reception is performed in the same manner as in mode 1.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Example 1, slave 0:

SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0 (6)

Example 2, slave 1:

SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X (7)

Example 2, slave 2:

SADDR = 1100 0000
SADEN = 1111 1100
Given = 1100 00XX (8)

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all 'don't cares' as well as a Broadcast address of all 'don't cares'. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

6.8 Serial Peripheral Interface (SPI)

6.8.1 SPI features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write collision flag protection (WCOL)
- Wake-up from Idle mode (slave mode only)

6.8.2 SPI description

The serial peripheral interface allows high-speed synchronous data transfer between the P89V660/662/664 and peripheral devices or between several P89V660/662/664 devices. Figure 23 shows the correspondence between master and slave SPI devices. The

Table 41. SPCR - SPI control register (address D5H) bit description *…continued*

Bit	Symbol	Description
2	CPHA	Clock Phase control bit. 1 = shift triggered on the trailing edge of the clock; 0 = shift triggered on the leading edge of the clock.
1	SPR1	SPI Clock Rate Select bit 1. Along with SPR0 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave. See Table 42.
0	SPR0	SPI Clock Rate Select bit 0. Along with SPR1 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave. See Table 42.

Table 42. SPCR - SPI control register (address D5H) clock rate selection

SPR1	SPR0	SPICLK = f_{osc} divided by	
		6-clock mode	12-clock mode
0	0	2	4
0	1	8	16
1	0	32	64
1	1	64	128

Table 43. SPSR - SPI status register (address AAH) bit allocation
Bit addressable; Reset source(s): any reset; Reset value: 0000 0000B

Bit	7	6	5	4	3	2	1	0
Symbol	SPIF	WCOL	-	-	-	-	-	-

Table 44. SPSR - SPI status register (address AAH) bit description

Bit	Symbol	Description
7	SPIF	SPI interrupt flag. Upon completion of data transfer, this bit is set to ‘1’. If SPIE = 1 and ES3 = 1, an interrupt is then generated. This bit is cleared by software.
6	WCOL	Write Collision Flag. Set if the SPI data register is written to during data transfer. This bit is cleared by software.
5 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

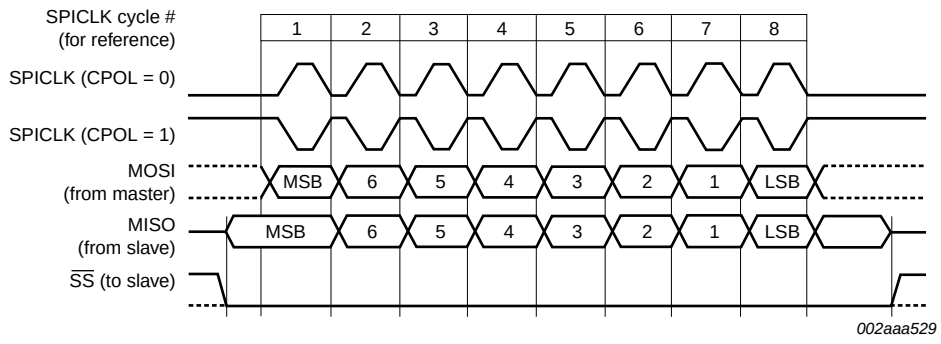


Fig 24. SPI transfer format with CPHA = 0

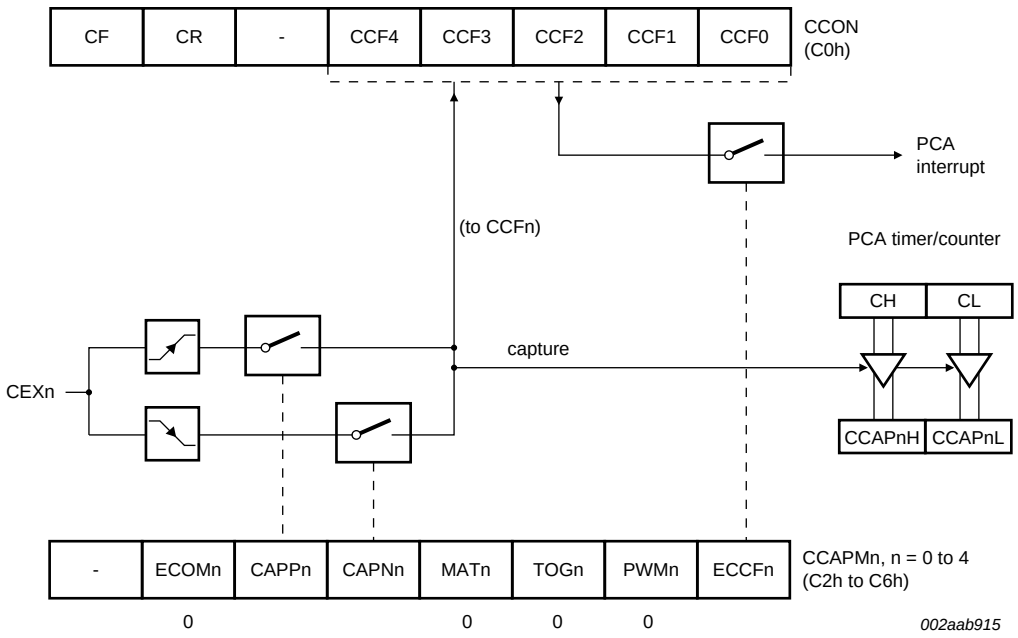


Fig 28. PCA capture mode

If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated.

6.10.2 16-bit software timer mode

The PCA modules can be used as software timers (Figure 29) by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

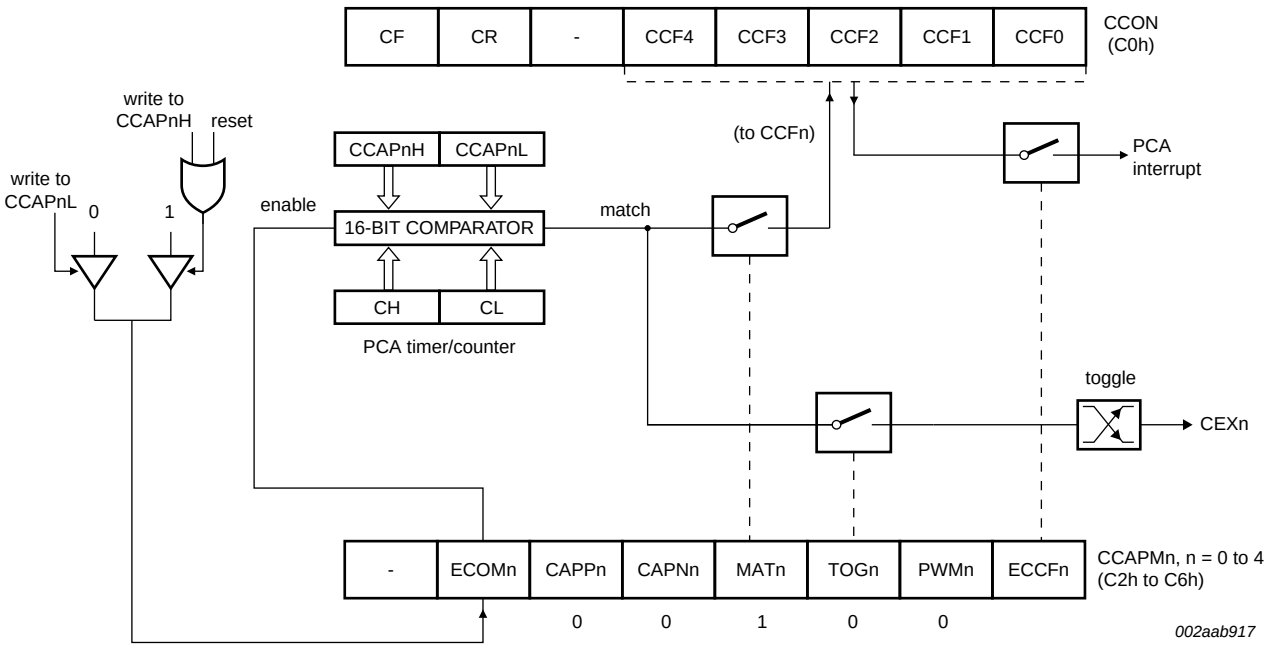


Fig 30. PCA high-speed output mode

6.10.4 Pulse width modulator mode

All of the PCA modules can be used as PWM outputs (Figure 31). Output frequency depends on the source for the PCA timer.

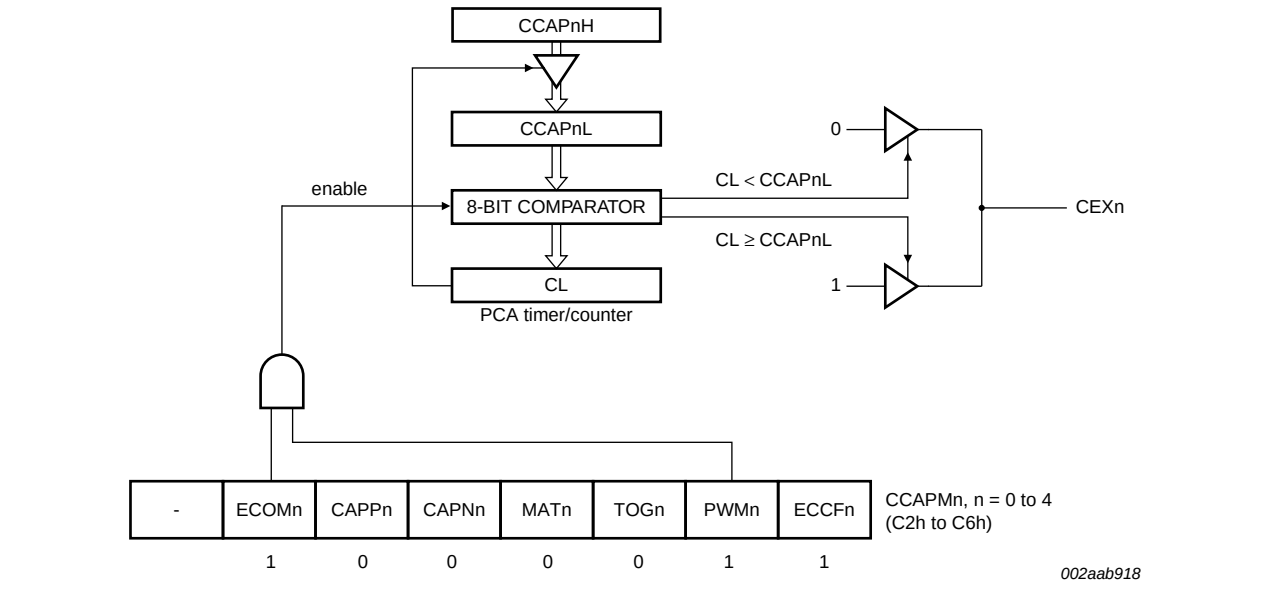


Fig 31. PCA PWM mode

All of the modules will have the same frequency of output because they all share one and only PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPnL. When the value of the PCA CL SFR is less than the

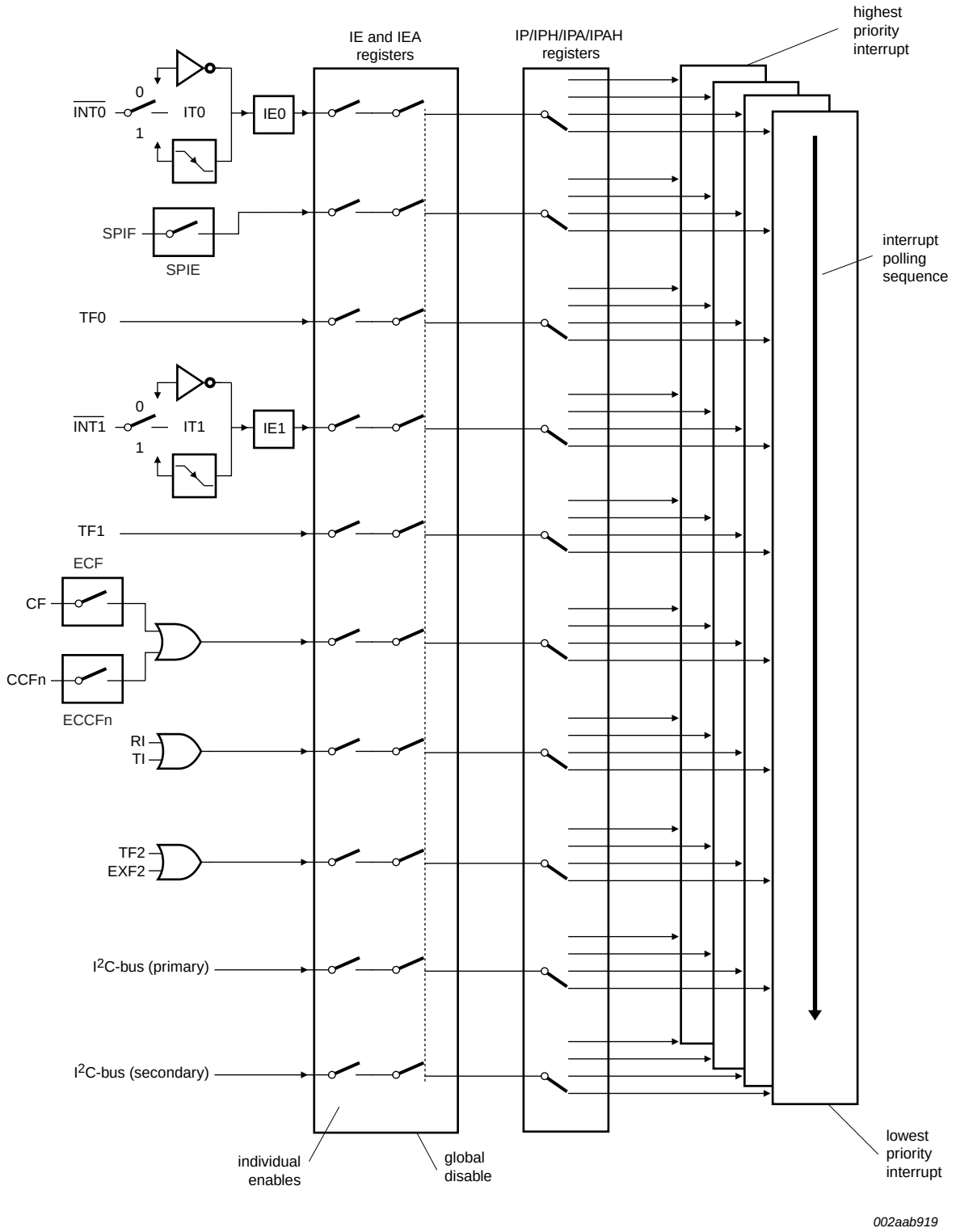


Fig 32. Interrupt structure

7. Limiting values

Table 69. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_I	input voltage	on $\overline{EA}$ pin to V_{SS}	–0.5	14	V
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	15	mA
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 70. Static characteristics

T_{amb} = –40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1]	10000	-	-	cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1]	100	-	-	years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1]	100 + I_{DD}	-	-	mA
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		–0.5	-	$0.2V_{DD}$ – 0.1	V
V_{IL}	LOW-level input voltage	SCL, SDA		–0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA, XTAL1, RST		$0.2V_{DD}$ + 0.9	-	V_{DD} + 0.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA		$0.7V_{DD}$	-	V_{DD} + 0.5	V
		XTAL1, RST		$0.7V_{DD}$	-	6.0	V
V_{OL}	LOW-level output voltage	V_{DD} = 4.5 V, except, $\overline{PSEN}$, ALE, SCL, SDA	[2][3][4]				
		I_{OL} = 1.6 mA		-	-	0.4	V
		V_{DD} = 4.5 V, ALE, $\overline{PSEN}$					
		I_{OL} = 3.2 mA		-	-	0.45	V
		V_{DD} = 4.5 V, SCL, SDA					
		I_{OL} = 3.0 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	V_{DD} = 4.5 V, ports 1, 2, 3, 4	[5]				
		I_{OH} = –30 μA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V, Port 0 in External Bus mode, ALE, $\overline{PSEN}$					
		I_{OH} = –3.2 mA		V_{DD} – 0.7	-	-	V
I_{IL}	LOW-level input current	V_I = 0.4 V, ports 1, 2, 3, 4		–1	-	–75	μA

9.1 Explanation of symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A — Address

C — Clock

D — Input data

H — Logic level HIGH

I — Instruction (program memory contents)

L — Logic level LOW or ALE

P — $\overline{\text{PSEN}}$

Q — Output data

R — $\overline{\text{RD}}$ signal

T — Time

V — Valid

W — $\overline{\text{WR}}$ signal

X — No longer a valid logic level

Z — High impedance (Float)

Example:

t_{AVLL} = Address valid to ALE LOW time

t_{LLPL} = ALE LOW to $\overline{\text{PSEN}}$ LOW time

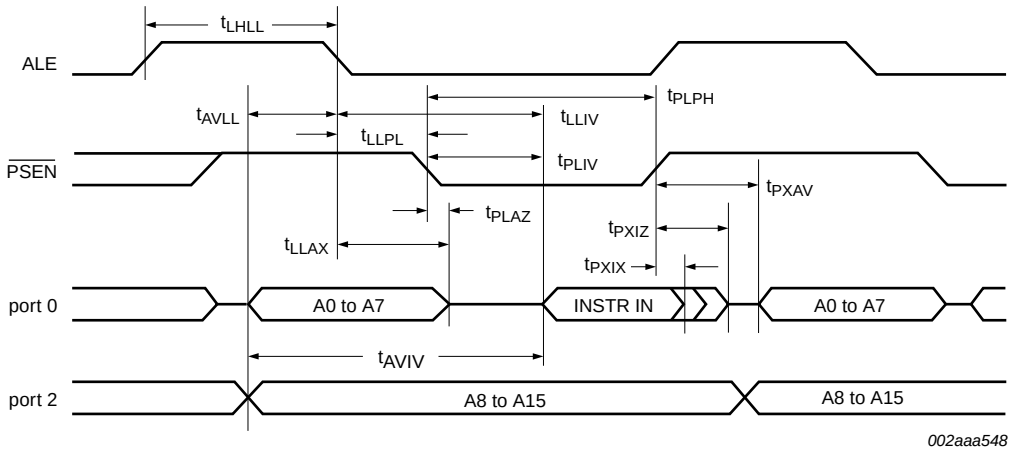


Fig 36. External program memory read cycle

Table 72. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

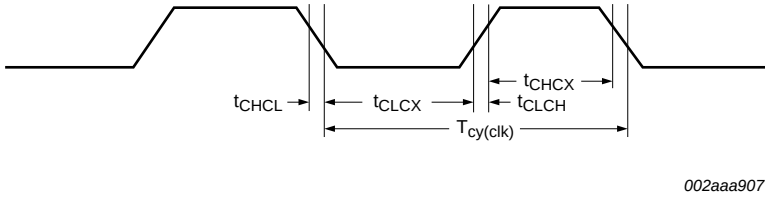


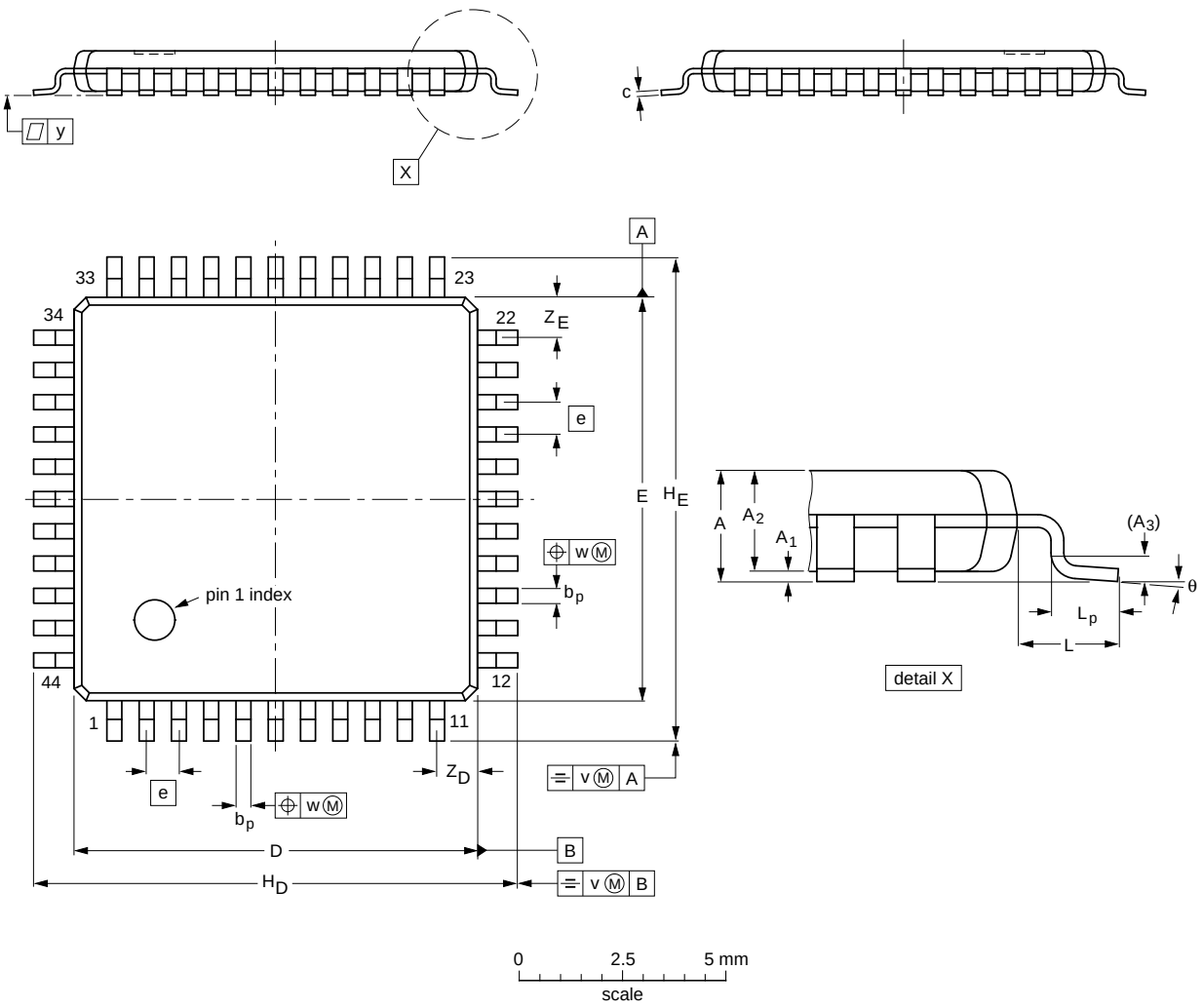
Fig 39. External clock drive waveform

Table 73. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 50$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns

10. Package outline

TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm **SOT376-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.45 0.30	0.18 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

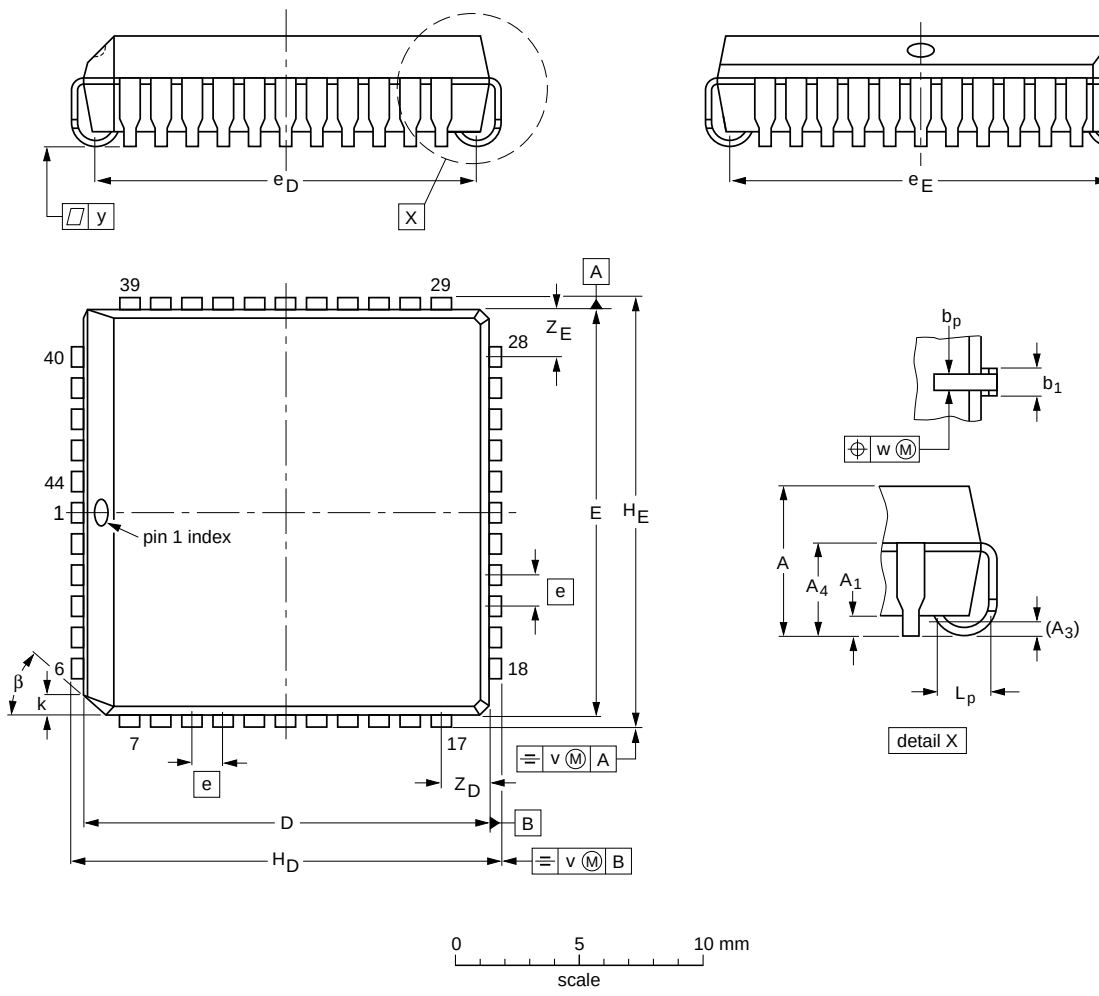
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT376-1	137E08	MS-026				~~00-01-19~~ 02-03-14

Fig 50. Package outline SOT376-1 (TQFP44)

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 51. Package outline SOT187-2 (PLCC44)

11. Abbreviations

Table 76. Acronym list

Acronym	Description
ALE	Address Latch Enabled
CPU	Central Processing Unit
DUT	Device Under Test
EPROM	Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
MCU	Microcontroller Unit
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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