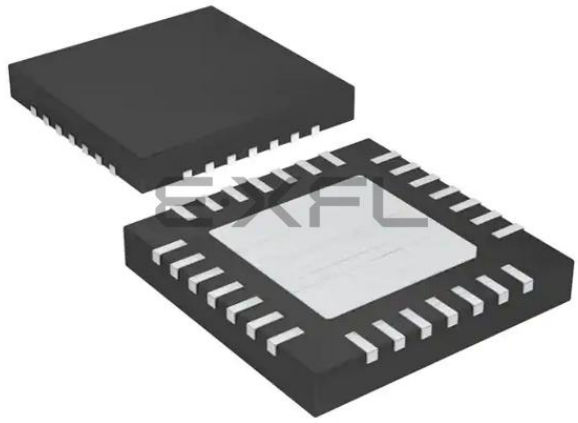
Silicon Labs - EFM8UB10F16G-C-QFN28R Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-WFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub10f16g-c-qfn28r

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to ±2% over supply and temperature corners.
- 48 MHz internal oscillator (HFOSC1), accurate to ±1.5% over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 12, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD [1]	V_{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO [3]	V_{IO}		1.71	—	V_{DD}	V
Operating Supply Voltage on VREGIN	V_{REGIN}		3.0	—	5.25	V
System Clock Frequency	f_{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation.
2. All voltages with respect to GND.
3. On devices without a VIO pin, $V_{IO} = V_{DD}$.
4. GPIO levels are undefined whenever VIO is less than 1 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on [4]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	820	1200	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	405	580	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	370	—	µA
		100 ksps, V_{DD} = 3.0 V	—	185	—	µA
		10 ksps, V_{DD} = 3.0 V	—	20	—	µA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	485	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	25	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	505	—	µA
		50 ksps, V_{DD} = 3.0 V	—	255	—	µA
		10 ksps, V_{DD} = 3.0 V	—	50	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	415	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	80	—	µA
Internal ADC0 Reference, Always-on [5]	I_{VREFFS}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	170	210	µA
Temperature Sensor	I_{TSENSE}		—	70	120	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	µA
		CPMD = 10	—	3	—	µA
		CPMD = 01	—	8.5	—	µA
		CPMD = 00	—	22.5	—	µA
Comparator Reference	I_{CPREF}		—	1.2	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5V Regulator	I_{VREG}	Normal Mode (SUSEN = 0, BIASENB = 0)	—	245	340	µA
		Suspend Mode (SUSEN = 1, BIASENB = 0)	—	60	100	µA
		Bias Disabled (BIASENB = 1)	—	2.5	10	µA
		Disabled (BIASENB = 1, REG1ENB = 1)	—	2.5	—	nA
USB (USB0) Full-Speed	I_{USB}	Low Energy Mode, 64 byte 1ms IN Interrupt transfers	—	850	—	µA
		Low Energy Mode, 64 byte 1ms OUT Interrupt transfers	—	250	—	µA
		Low Energy Mode, Idle (SOF only)	—	50	—	µA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.2	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.2 V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} >1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	40	—	ppm/°C
High Frequency Oscillator 1 (48 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	T_A = 25 °C	—	0.02	—	%/V
Temperature Sensitivity	TS_{HFOSC1}	V_{DD} = 3.0 V	—	45	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	-79	—	dB
		10 Bit Mode	—	-70	—	dB

Note:
1. Absolute input pin voltage is limited by the V_{DD} supply.

4.1.9 Voltage Reference

Table 4.9. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, V_{DD} > 2.6 V	2.35	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; VREF = 3.0 V	—	8	—	µA

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential, V_{CM} = 1.65 V	—	110	—	ns
		-100 mV Differential, V_{CM} = 1.65 V	—	160	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential, V_{CM} = 1.65 V	—	1.2	—	µs
		-100 mV Differential, V_{CM} = 1.65 V	—	4.5	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V_{IN}	Direct comparator input	-0.25	—	V_{IO}+0.25	V
		Reference DAC input	1.2		V_{IO}	V
Reference DAC Resolution	N_{bits}			6		bits
Reference DAC Input Impedance	R_{CPREF}		—	2.75	—	MΩ
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°

4.1.14 USB Transceiver

Table 4.14. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmitter						
Output High Voltage	V_{OH}	V_{DD} ≥3.0V	2.8	—	—	V
Output Low Voltage	V_{OL}	V_{DD} ≥3.0V	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	28	36	44	Ω
		Driving Low	28	36	44	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
		Low Speed (D- Pull-up)				
Output Rise Time	T_R	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Output Fall Time	T_F	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Receiver						
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

4.2 Thermal Conditions

Table 4.15. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN-20 Packages	—	60	—	°C/W
		QFN-28 Packages	—	26	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

5. Typical Connection Diagrams

5.1 Power

The figure below shows a typical connection diagram for the power pins of the EFM8UB1 devices when the internal regulator used and USB is connected (bus-powered). VBUS is not used as a sense pin in this scenario, so that pin can be used as a standard GPIO.

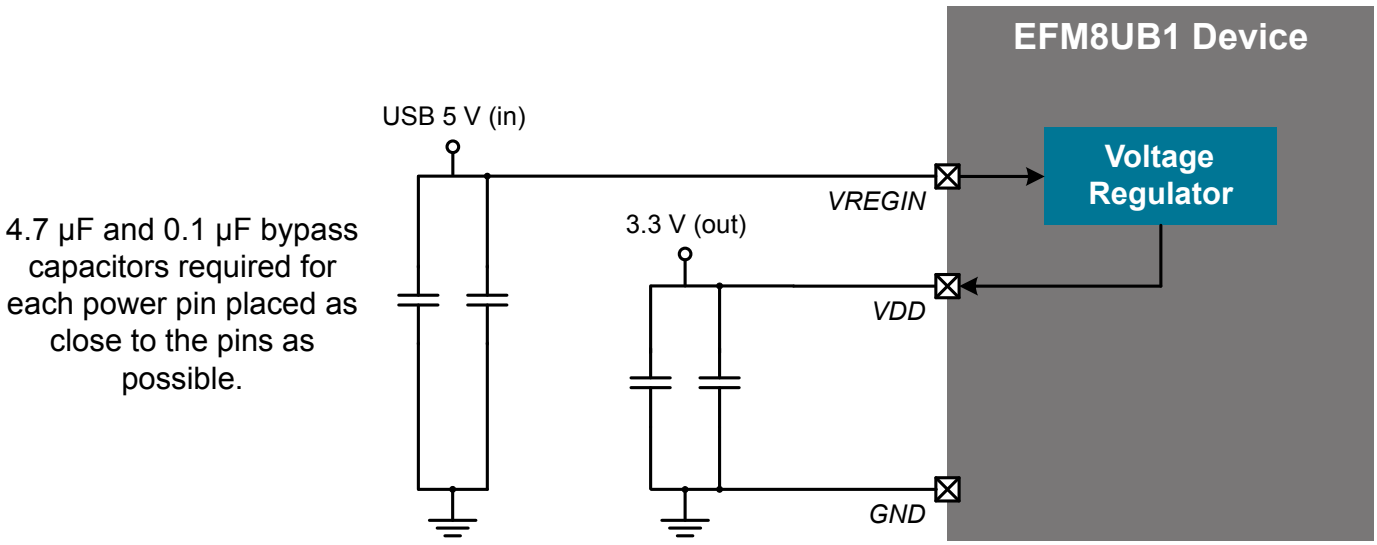

Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB1 devices when the internal regulator used and USB is connected (self-powered). The VBUS signal is used to detect when USB is connected to a host device.

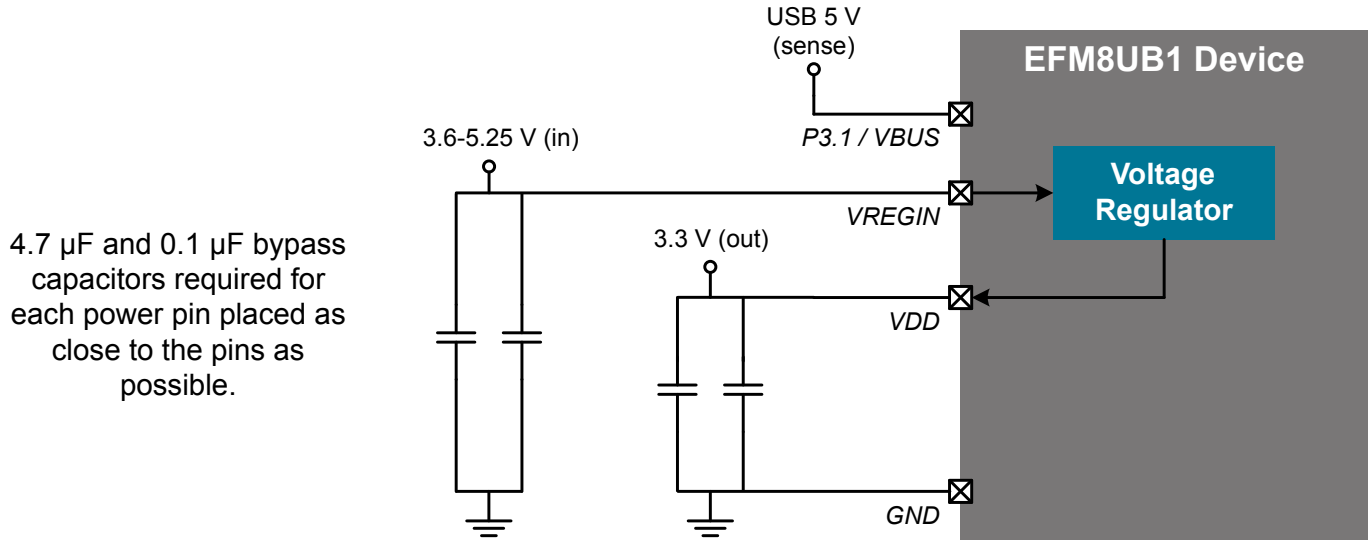

Figure 5.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB1 devices when the internal 5 V-to-3.3 V regulator is not used.

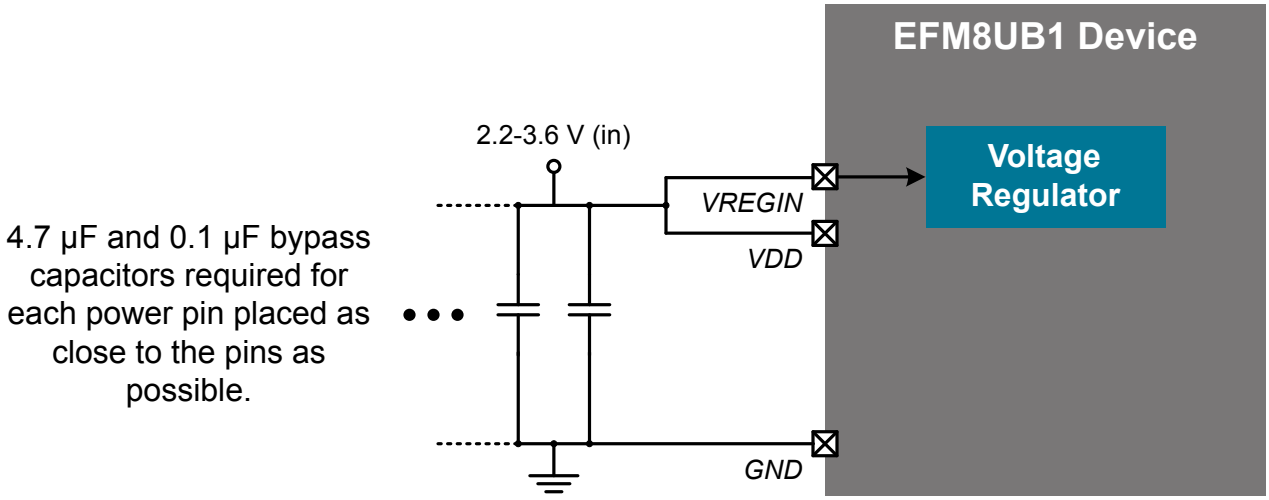

Figure 5.3. Connection Diagram with Voltage Regulator Not Used

5.3 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

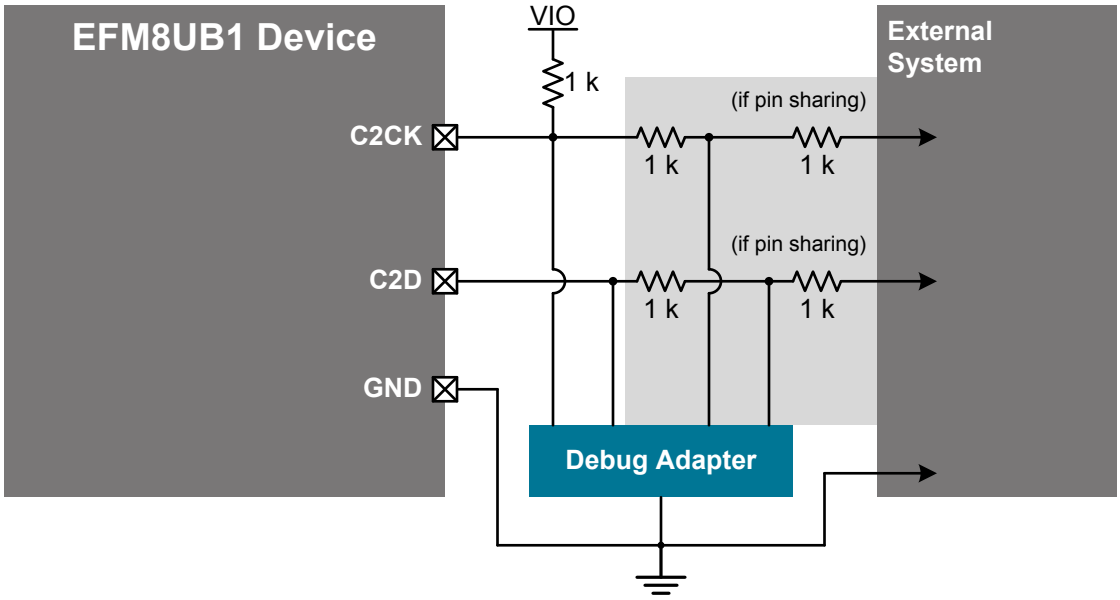

Figure 5.6. Debug Connection Diagram

5.4 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
3	GND	Ground			
4	D+	USB Data Positive			ADC0.28
5	D-	USB Data Negative			ADC0.29
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	P3.1	Multifunction I/O		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
11	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.23 CMP1P.12 CMP1N.12
12	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.22 CMP1P.11 CMP1N.11
13	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.21 CMP1P.10 CMP1N.10
14	P2.0	Multifunction I/O	Yes	P2MAT.0	ADC0.20 CMP1P.9 CMP1N.9
15	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CMP1P.7 CMP1N.7
16	P1.6	Multifunction I/O	Yes	P1MAT.6 I2C0_SCL	ADC0.14 CMP1P.6 CMP1N.6
17	P1.5	Multifunction I/O	Yes	P1MAT.5 I2C0_SDA	ADC0.13 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
4	GND	Ground			
5	D+	USB Data Positive			ADC0.28
6	D-	USB Data Negative			ADC0.29
7	VIO	I/O Power Input			
8	VDD	Supply Power Input / 5V Regulator Output			
9	VREGIN	5V Regulator Input			
10	P3.1	Multifunction I/O		VBUS	
11	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
12	P2.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		
13	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.9 CMP1N.9
14	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.7 CMP1N.7
15	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.6 CMP1N.6
16	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.5 CMP1N.5
17	P1.2	Multifunction I/O	Yes	P1MAT.2 I2C0_SCL	ADC0.10 CMP1P.4 CMP1N.4
18	P1.1	Multifunction I/O	Yes	P1MAT.1 I2C0_SDA	ADC0.9 CMP1P.3 CMP1N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.2 CMP1N.2
20	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP1P.1 CMP1N.1 CMP0P.7 CMP0N.7
21	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP1P.0 CMP1N.0 CMP0P.6 CMP0N.6
22	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5
23	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4
24	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	GND	Ground			
4	D+	USB Data Positive			ADC0.28
5	D-	USB Data Negative			ADC0.29
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	P3.1	Multifunction I/O		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P2.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		
11	P1.2	Multifunction I/O	Yes	P1MAT.2 I2C0_SCL	ADC0.10 CMP1P.4 CMP1N.4
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1 I2C0_SDA	ADC0.9 CMP1P.3 CMP1N.3
14	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.2 CMP1N.2
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP1P.1 CMP1N.1 CMP0P.7 CMP0N.7
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP1P.0 CMP1N.0 CMP0P.6 CMP0N.6
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5

7. QFN28 Package Specifications

7.1 QFN28 Package Dimensions

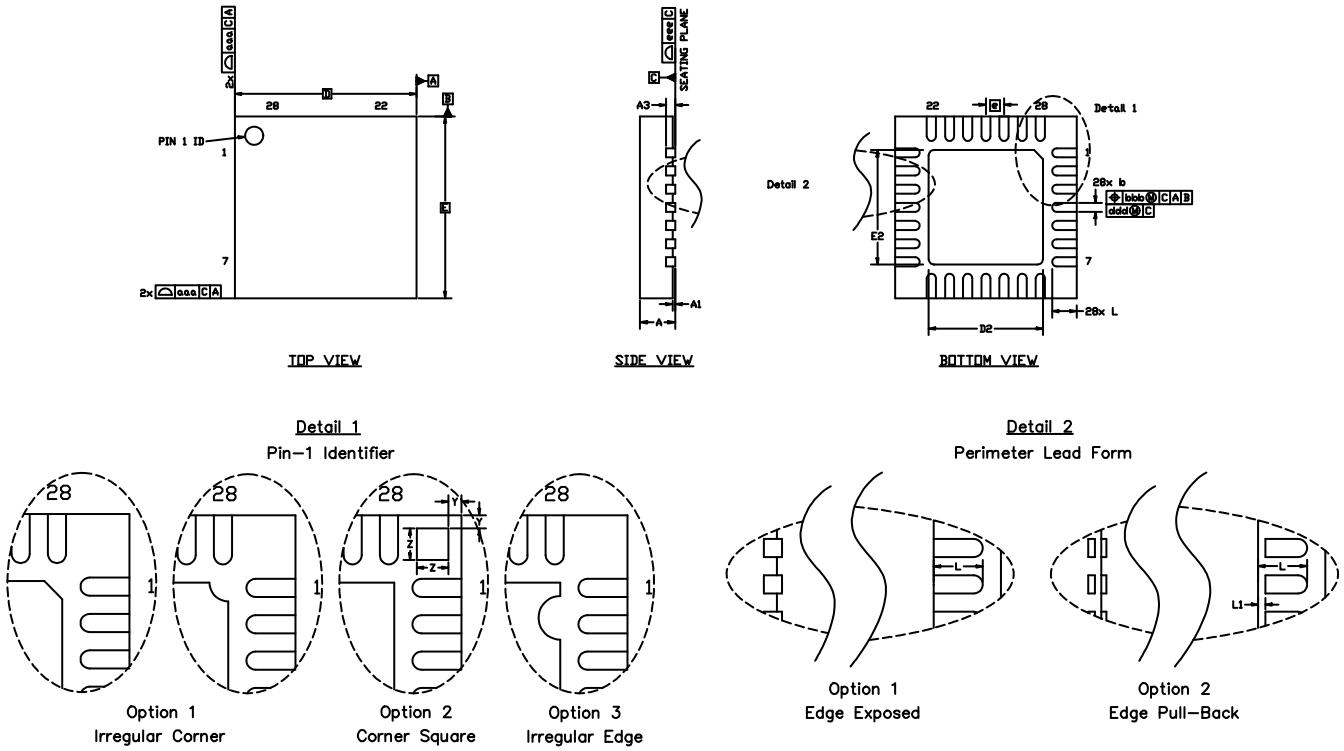

Figure 7.1. QFN28 Package Drawing

Table 7.1. QFN28 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.25	3.35
e		0.50 BSC	
E	4.90	5.00	5.10
E2	3.15	3.25	3.35
L	0.45	0.55	0.65
aaa		0.15	
bbb		0.10	
ddd		0.05	

Dimension	Min	Typ	Max
eee		0.08	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Dimension	Min	Max
Y2	3.35	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.2 mm square openings on a 1.5 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN28 Package Marking

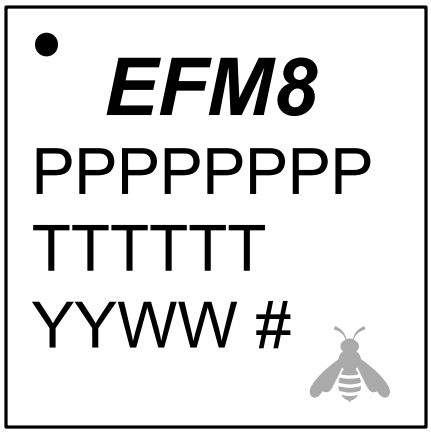

Figure 7.3. QFN28 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8.2 QSOP24 PCB Land Pattern

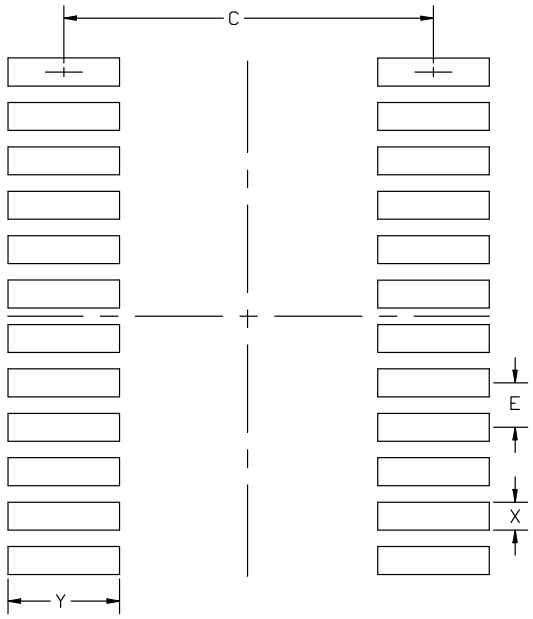

Figure 8.2. QSOP24 PCB Land Pattern Drawing

Table 8.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Revision History

10.1 Revision 1.1

December 16, 2015

Updated 3.2 Power to properly reflect that a comparator falling edge wakes the device from Suspend and Snooze.

Added Note 4 to Table 4.1 Recommended Operating Conditions on page 12.

Added 5.3 Debug.

10.2 Revision 1.0

Updated any TBD numbers in 4.1 Electrical Characteristics and adjusted various specifications.

Updated VOH and VOL graphs in Figure 4.6 Typical V_{OH} Curves on page 28 and Figure 4.7 Typical V_{OL} Curves on page 28 and updated the VOH and VOL specifications in Table 4.13 Port I/O on page 22.

Added more information to 3.10 Bootloader.

Updated part numbers to Revision C.

10.3 Revision 0.3

Updated QFN20 packaging and landing diagram dimensions.

Updated QFN28 D and E minimum value.

Updated some characterization TBD values.

Added maximum allowable voltages on D+ and D- and added VBUS / P3.1 to the standard I/O row in Table 4.16 Absolute Maximum Ratings on page 24.

Added a diagram to 5.1 Power for cases when the internal 5 V-to-3.3 V regulator is not used.

Updated the 5 V-to-3.3 V regulator Electrical Characteristics table.

Added Stop mode to the Power Modes table in 3.2 Power.

10.4 Revision 0.2

Initial release.