Silicon Labs - EFM8UB10F8G-C-QFN20 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub10f8g-c-qfn20

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulators in normal bias mode for fast wake • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SUSPEND bit in PCON1	• USB0 Bus Activity • Timer 4 Event • SPI0 Activity • I2C0 Slave Activity • Port Match Event • Comparator 0 Falling Edge
Stop	• All internal power nets shut down • 5V regulator remains active (if enabled) • Internal 1.8 V LDO on • Pins retain state • Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulators in low bias current mode for energy savings • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SNOOZE bit in PCON1	• USB0 Bus Activity • Timer 4 Event • SPI0 Activity • I2C0 Slave Activity • Port Match Event • Comparator 0 Falling Edge
Shutdown	• All internal power nets shut down • 5V regulator remains active (if enabled) • Internal 1.8 V LDO off to save energy • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P3.0 and P3.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0.

The port control block offers the following features:

- Up to 22 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 20 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to ±2% over supply and temperature corners.
- 48 MHz internal oscillator (HFOSC1), accurate to ±1.5% over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- Automatic start and stop generation
- Single-byte buffer on transmit and receive

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break and sync field detection.
- CTS / RTS hardware flow control.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes.
- Supports external clock frequencies up to 12 Mbps in master or slave mode.
- Support for all clock phase and polarity modes.
- 8-bit programmable clock rate (master).
- Programmable receive timeout (slave).
- Four byte FIFO on transmit and receive.
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive buffers to help increase throughput in faster applications

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- USB reset

3.9 Debugging

The EFM8UB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1, 2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1, 2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming[3]	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUSPENDWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	$t_{SLEEPWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	12	—	µs

4.4 Typical Performance Curves

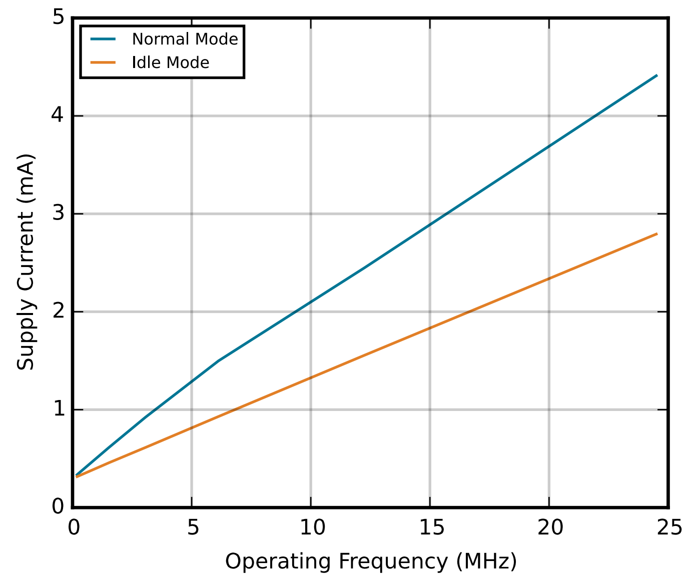

Figure 4.1. Typical Operating Supply Current using HFOSC0

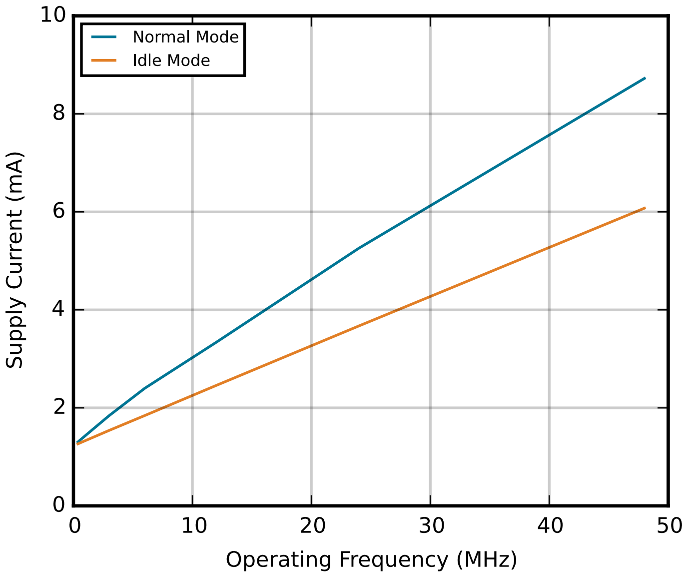

Figure 4.2. Typical Operating Supply Current using HFOSC1

5.2 USB

Figure 5.4 Bus-Powered Connection Diagram for USB Pins on page 31 shows a typical connection bus-powered diagram for the USB pins of the EFM8UB1 devices including ESD protection diodes on the USB pins.

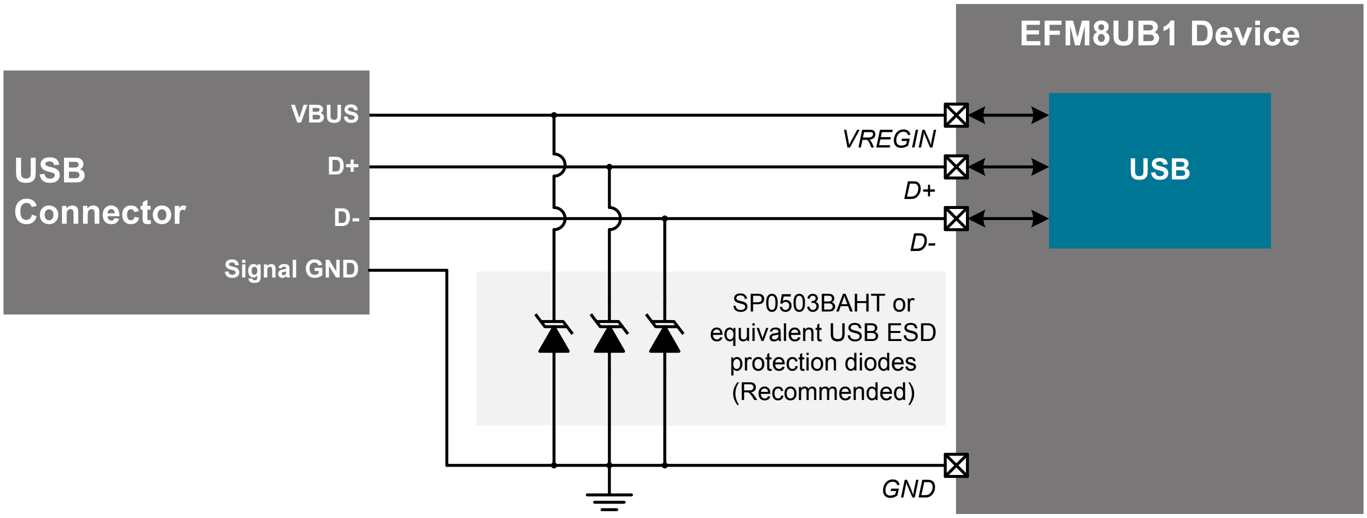

Figure 5.4. Bus-Powered Connection Diagram for USB Pins

Figure 5.5 Self-Powered Connection Diagram for USB Pins on page 31 shows a typical connection self-powered diagram for the USB pins of the EFM8UB1 devices including ESD protection diodes on the USB pins.

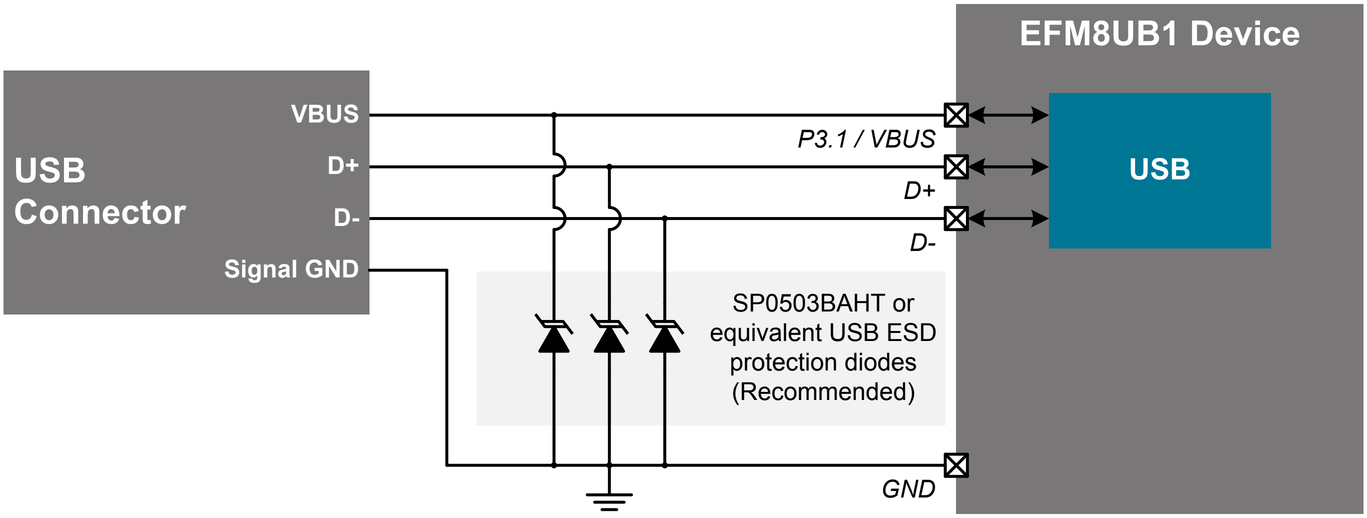

Figure 5.5. Self-Powered Connection Diagram for USB Pins

6. Pin Definitions

6.1 EFM8UB1x-QFN28 Pin Definitions

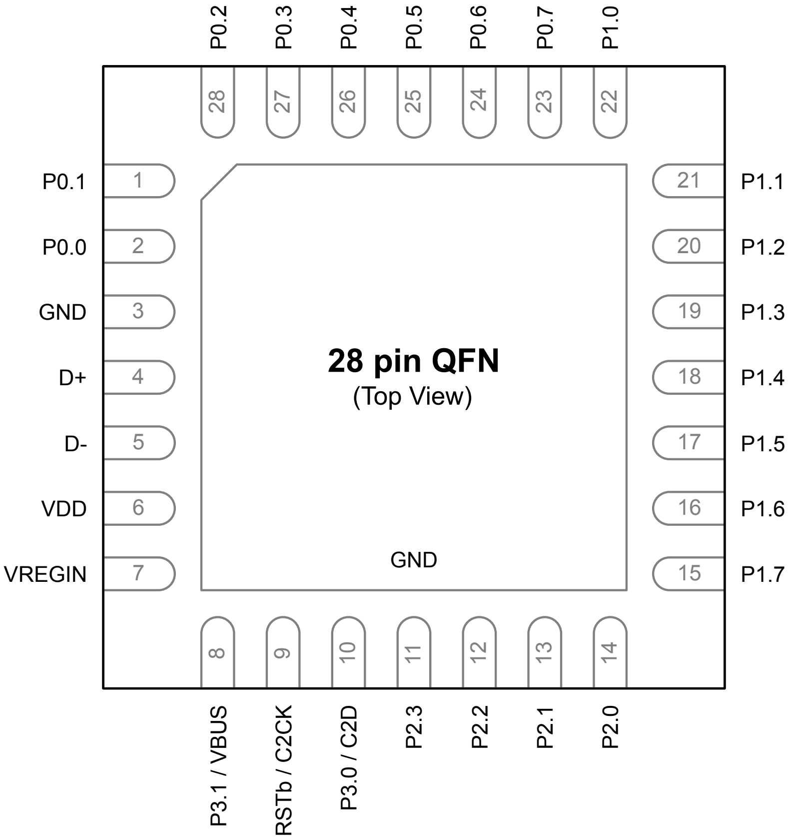

Figure 6.1. EFM8UB1x-QFN28 Pinout

Table 6.1. Pin Definitions for EFM8UB1x-QFN28

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
19	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
20	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
21	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1 CMP0P.10 CMP0N.10
22	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0 CMP0P.9 CMP0N.9
23	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
24	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
25	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5
26	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4

6.2 EFM8UB1x-QSOP24 Pin Definitions

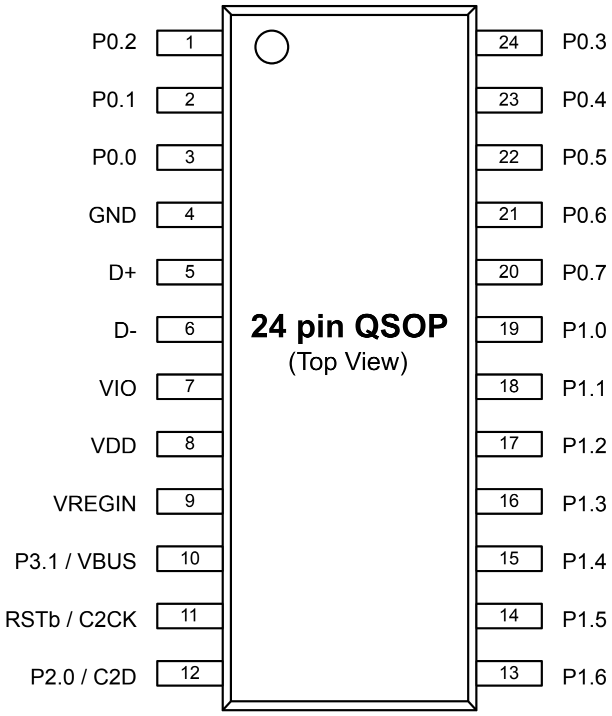

Figure 6.2. EFM8UB1x-QSOP24 Pinout

Table 6.2. Pin Definitions for EFM8UB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
4	GND	Ground			
5	D+	USB Data Positive			ADC0.28
6	D-	USB Data Negative			ADC0.29
7	VIO	I/O Power Input			
8	VDD	Supply Power Input / 5V Regulator Output			
9	VREGIN	5V Regulator Input			
10	P3.1	Multifunction I/O		VBUS	
11	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
12	P2.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		
13	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.9 CMP1N.9
14	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.7 CMP1N.7
15	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.6 CMP1N.6
16	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.5 CMP1N.5
17	P1.2	Multifunction I/O	Yes	P1MAT.2 I2C0_SCL	ADC0.10 CMP1P.4 CMP1N.4
18	P1.1	Multifunction I/O	Yes	P1MAT.1 I2C0_SDA	ADC0.9 CMP1P.3 CMP1N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.2 CMP1N.2
20	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP1P.1 CMP1N.1 CMP0P.7 CMP0N.7
21	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP1P.0 CMP1N.0 CMP0P.6 CMP0N.6
22	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5
23	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4
24	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3

7. QFN28 Package Specifications

7.1 QFN28 Package Dimensions

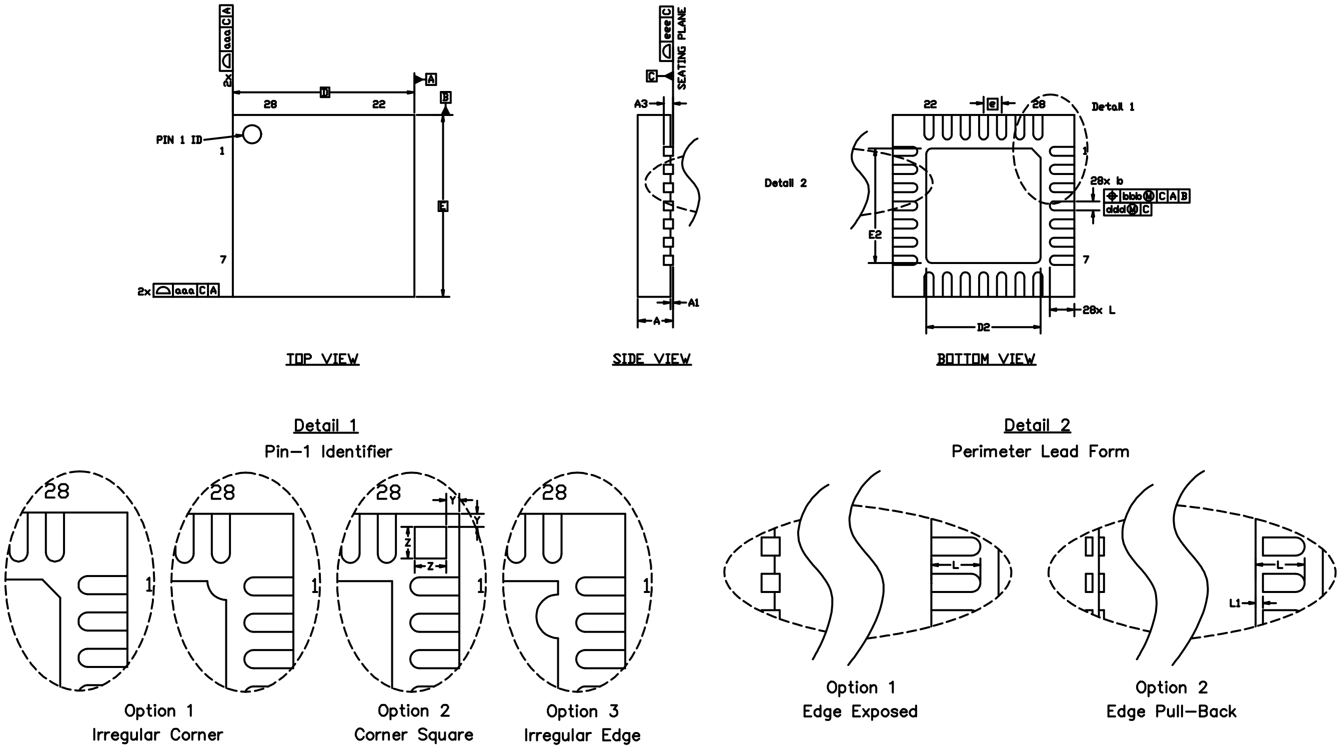

Figure 7.1. QFN28 Package Drawing

Table 7.1. QFN28 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.25	3.35
e	0.50 BSC		
E	4.90	5.00	5.10
E2	3.15	3.25	3.35
L	0.45	0.55	0.65
aaa	0.15		
bbb	0.10		
ddd	0.05		

Dimension	Min	Max
Y2	3.35	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.2 mm square openings on a 1.5 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN28 Package Marking

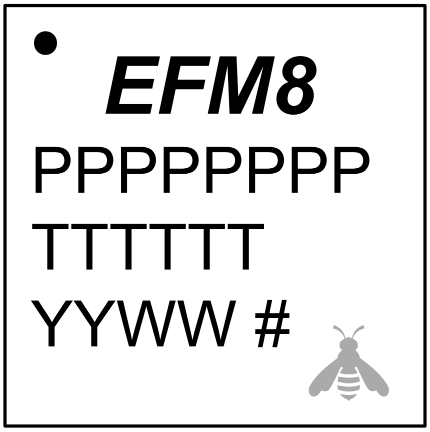

Figure 7.3. QFN28 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. QFN20 Package Specifications

9.1 QFN20 Package Dimensions

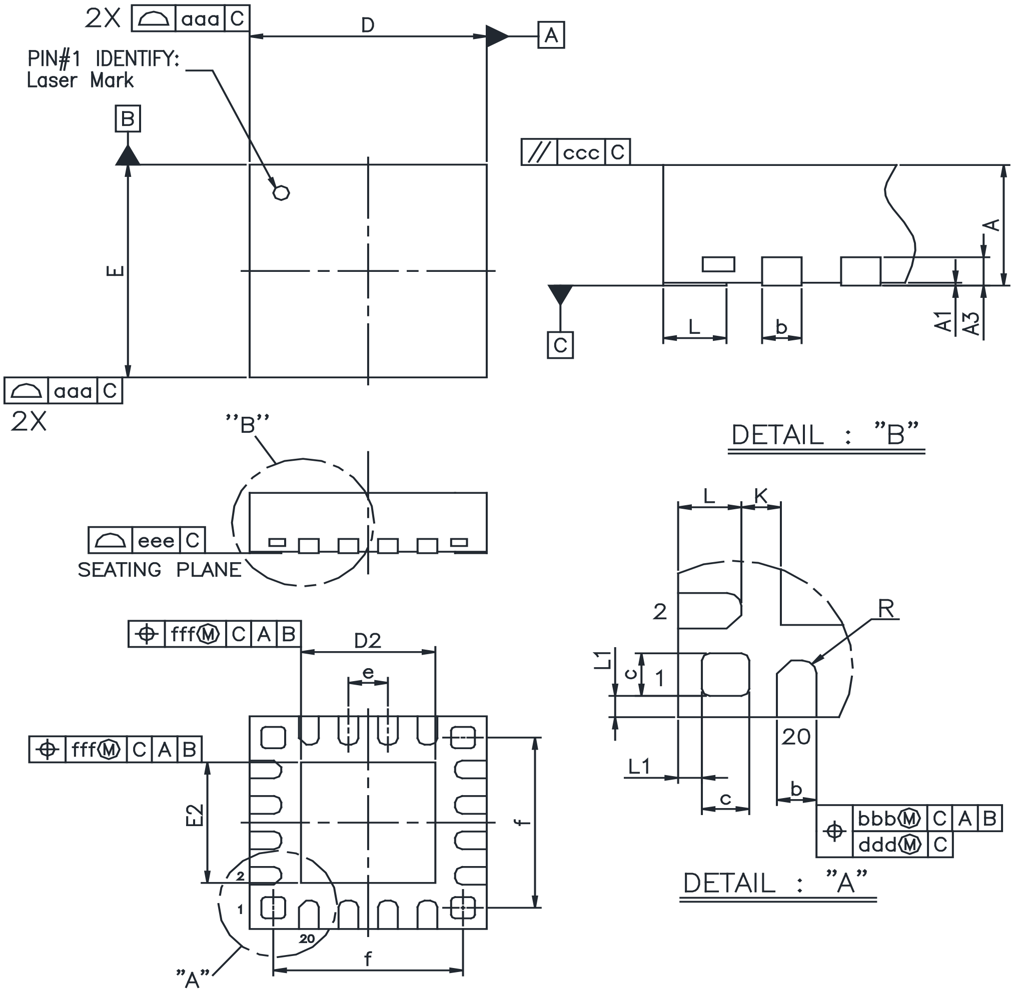

Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D		3.00 BSC	
D2	1.6	1.70	1.80
e		0.50 BSC	

Dimension	Min	Typ	Max
E	3.00 BSC		
E2	1.60	1.70	1.80
f	2.50 BSC		
L	0.30	0.40	0.50
K	0.25 REF		
R	0.09	0.125	0.15
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 6. The stencil thickness should be 0.125 mm (5 mils). 7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads. 8. A 2 x 2 array of 0.75 mm openings on a 0.95 mm pitch should be used for the center pad to assure proper paste volume. 9. A No-Clean, Type-3 solder paste is recommended. 10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

9.3 QFN20 Package Marking

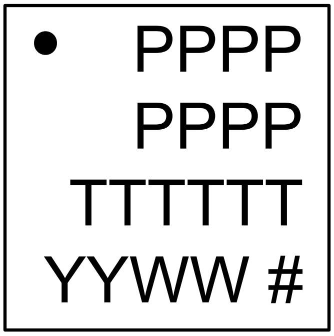

Figure 9.3. QFN20 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

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