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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8ub10f8g-c-qfn20r">https://www.e-xfl.com/product-detail/silicon-labs/efm8ub10f8g-c-qfn20r</a>

## 1. Feature List

The EFM8UB1 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- Memory:
  - Up to 16 KB flash memory, in-system re-programmable from firmware, including 1 KB of 64-byte sectors and 15 KB of 512-byte sectors.
  - Up to 2304 bytes RAM (including 256 bytes standard 8051 RAM, 1024 bytes on-chip XRAM, and 1024 bytes of USB buffer)
- Power:
  - 5 V-input LDO regulator for direct connection to USB supply
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 22 total multifunction I/O pins:
  - All pins 5 V tolerant under bias
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 48 MHz oscillator with accuracy of  $\pm 1.5\%$  stand-alone and  $\pm 0.25\%$  using USB clock recovery
  - Internal 24.5 MHz oscillator with  $\pm 2\%$  accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
- Timers/Counters and PWM:
  - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 5 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
  - USB 2.0-compliant full speed with integrated low-power transceiver, 4 bidirectional endpoints, and dedicated 1 KB buffer
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I2C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
  - 12-Bit Analog-to-Digital Converter (ADC)
  - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded USB bootloader
- Temperature range -40 to 85 °C
- Single power supply of 2.2 to 3.6 V or 3.0 to 5.25 V
- QSOP24, QFN28, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. The on-chip 5V-to-3.3V regulator enables operation from 2.2 V up to a 5.25 V supply. Devices are available in 28-pin QFN, 20-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive)
- 8- or 9-bit data
- Automatic start and stop generation
- Single-byte buffer on transmit and receive

### Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive).
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break and sync field detection.
- CTS / RTS hardware flow control.

### Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes.
- Supports external clock frequencies up to 12 Mbps in master or slave mode.
- Support for all clock phase and polarity modes.
- 8-bit programmable clock rate (master).
- Programmable receive timeout (slave).
- Four byte FIFO on transmit and receive.
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte.
- Support for multiple masters on the same data lines.

## System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive buffers to help increase throughput in faster applications

## I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition

## 16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

## 3.7 Analog

### 12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

### Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 12 (CMP1) external positive inputs
- Up to 10 (CMP0) or 12 (CMP1) external negative inputs
- Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and  $\pm 20$  mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions](#) on page 12, unless stated otherwise.

#### 4.1.1 Recommended Operating Conditions

**Table 4.1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD <sup>1</sup>	V <sub>DD</sub>		2.2	—	3.6	V
Operating Supply Voltage on VIO <sup>3</sup>	V <sub>IO</sub>		1.71	—	V <sub>DD</sub>	V
Operating Supply Voltage on VREGIN	V <sub>REGIN</sub>		3.0	—	5.25	V
System Clock Frequency	f <sub>SYSCLK</sub>		0	—	50	MHz
Operating Ambient Temperature	T <sub>A</sub>		-40	—	85	°C

**Note:**

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation.
2. All voltages with respect to GND.
3. On devices without a VIO pin, V<sub>IO</sub> = V<sub>DD</sub>.
4. GPIO levels are undefined whenever VIO is less than 1 V.

## 4.1.2 Power Consumption

**Table 4.2. Power Consumption**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Digital Core Supply Current</b>						
Normal Mode-Full speed with code executing from flash	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 48 MHz <sup>2</sup>	—	8.9	9.8	mA
		F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	4.3	4.9	mA
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	600	—	μA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	145	—	μA
Idle Mode-Core halted with peripherals running	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 48 MHz <sup>2</sup>	—	6	6.6	mA
		F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	2.8	3.2	mA
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	440	—	μA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	130	—	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I <sub>DD</sub>	LFO Running	—	125	—	μA
		LFO Stopped	—	120	—	μA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I <sub>DD</sub>	LFO Running	—	25	—	μA
		LFO Stopped	—	20	—	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I <sub>DD</sub>		—	120	—	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I <sub>DD</sub>		—	0.2	—	μA
<b>Analog Peripheral Supply Currents</b>						
High-Frequency Oscillator 0	I <sub>HFOSC0</sub>	Operating at 24.5 MHz, T <sub>A</sub> = 25 °C	—	105	—	μA
High-Frequency Oscillator 1	I <sub>HFOSC1</sub>	Operating at 48 MHz, T <sub>A</sub> = 25 °C	—	850	—	μA
Low-Frequency Oscillator	I <sub>LFOSC</sub>	Operating at 80 kHz, T <sub>A</sub> = 25 °C	—	4	—	μA

#### 4.1.6 Internal Oscillators

**Table 4.6. Internal Oscillators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	$f_{\text{HFOSC0}}$	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC0}}$	$T_A = 25\text{ }^\circ\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC0}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	40	—	ppm/ $^\circ\text{C}$
High Frequency Oscillator 1 (48 MHz)						
Oscillator Frequency	$f_{\text{HFOSC1}}$	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC1}}$	$T_A = 25\text{ }^\circ\text{C}$	—	0.02	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC1}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	45	—	ppm/ $^\circ\text{C}$
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	$f_{\text{LFOSC}}$	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$\text{PSS}_{\text{LFOSC}}$	$T_A = 25\text{ }^\circ\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{LFOSC}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	65	—	ppm/ $^\circ\text{C}$

#### 4.1.7 External Clock Input

**Table 4.7. External Clock Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	$f_{\text{CMOS}}$		0	—	50	MHz
External Input CMOS Clock High Time	$t_{\text{CMOSH}}$		9	—	—	ns
External Input CMOS Clock Low Time	$t_{\text{CMOSL}}$		9	—	—	ns



### 4.3 Absolute Maximum Ratings

Stresses above those listed in 4.3 Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.16. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	$T_{BIAS}$		-55	125	°C
Storage Temperature	$T_{STG}$		-65	150	°C
Voltage on VDD	$V_{DD}$		GND-0.3	4.2	V
Voltage on VIO <sup>2</sup>	$V_{IO}$		GND-0.3	4.2	V
Voltage on VREGIN	$V_{REGIN}$		GND-0.3	5.8	V
Voltage on D+ or D-	$V_{USBD}$		GND-0.3	$V_{DD}+0.3$	V
Voltage on I/O pins (including VBUS / P3.1) or RSTb	$V_{IN}$	$V_{IO} > 3.3\text{ V}$	GND-0.3	5.8	V
		$V_{IO} < 3.3\text{ V}$	GND-0.3	$V_{IO}+2.5$	V
Total Current Sunk into Supply Pin	$I_{VDD}$		—	400	mA
Total Current Sourced out of Ground Pin	$I_{GND}$		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	$I_{IO}$		-100	100	mA
Operating Junction Temperature	$T_J$		-40	105	°C

**Note:**

1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. On devices without a VIO pin,  $V_{IO} = V_{DD}$

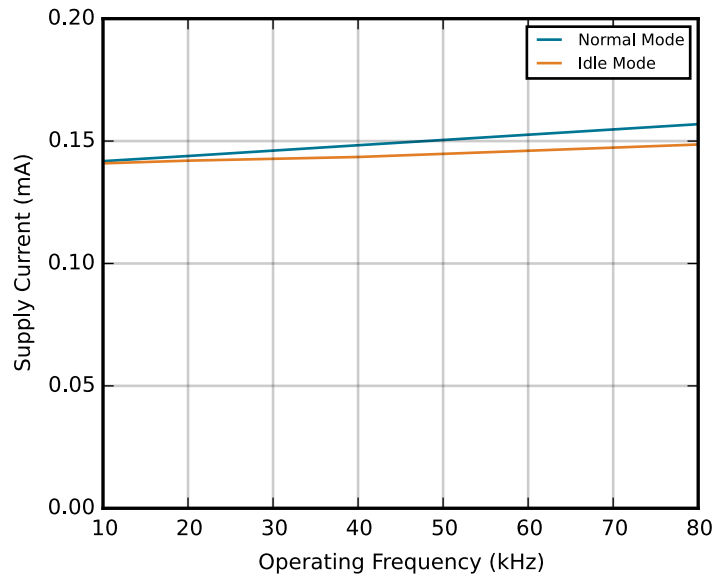


Figure 4.3. Typical Operating Supply Current using LFOSC

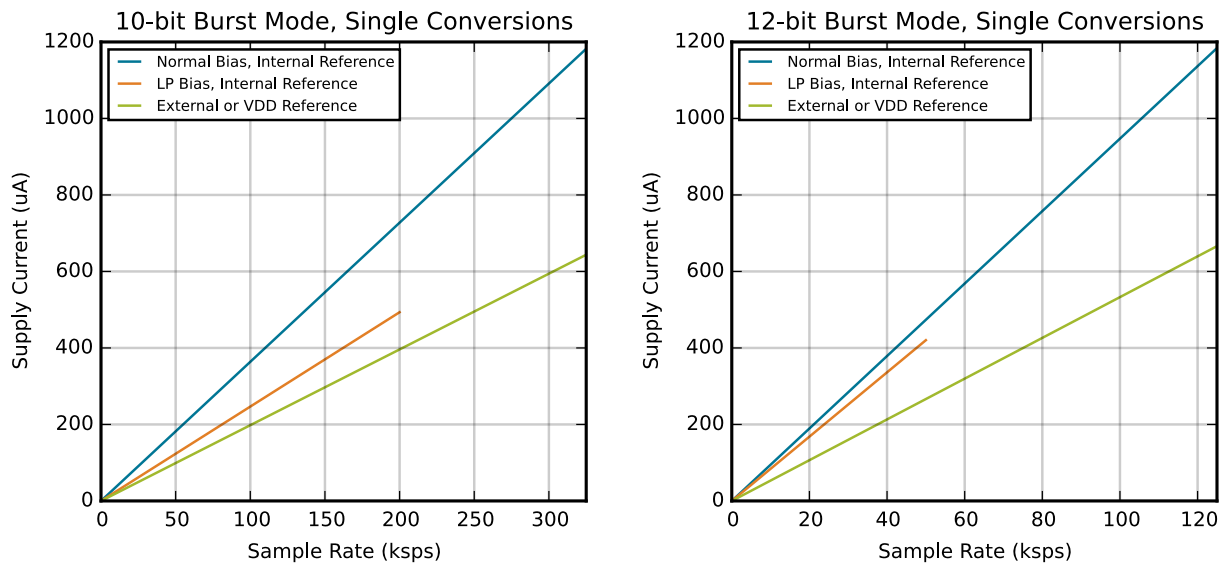


Figure 4.4. Typical ADC0 and Internal Reference Supply Current in Burst Mode

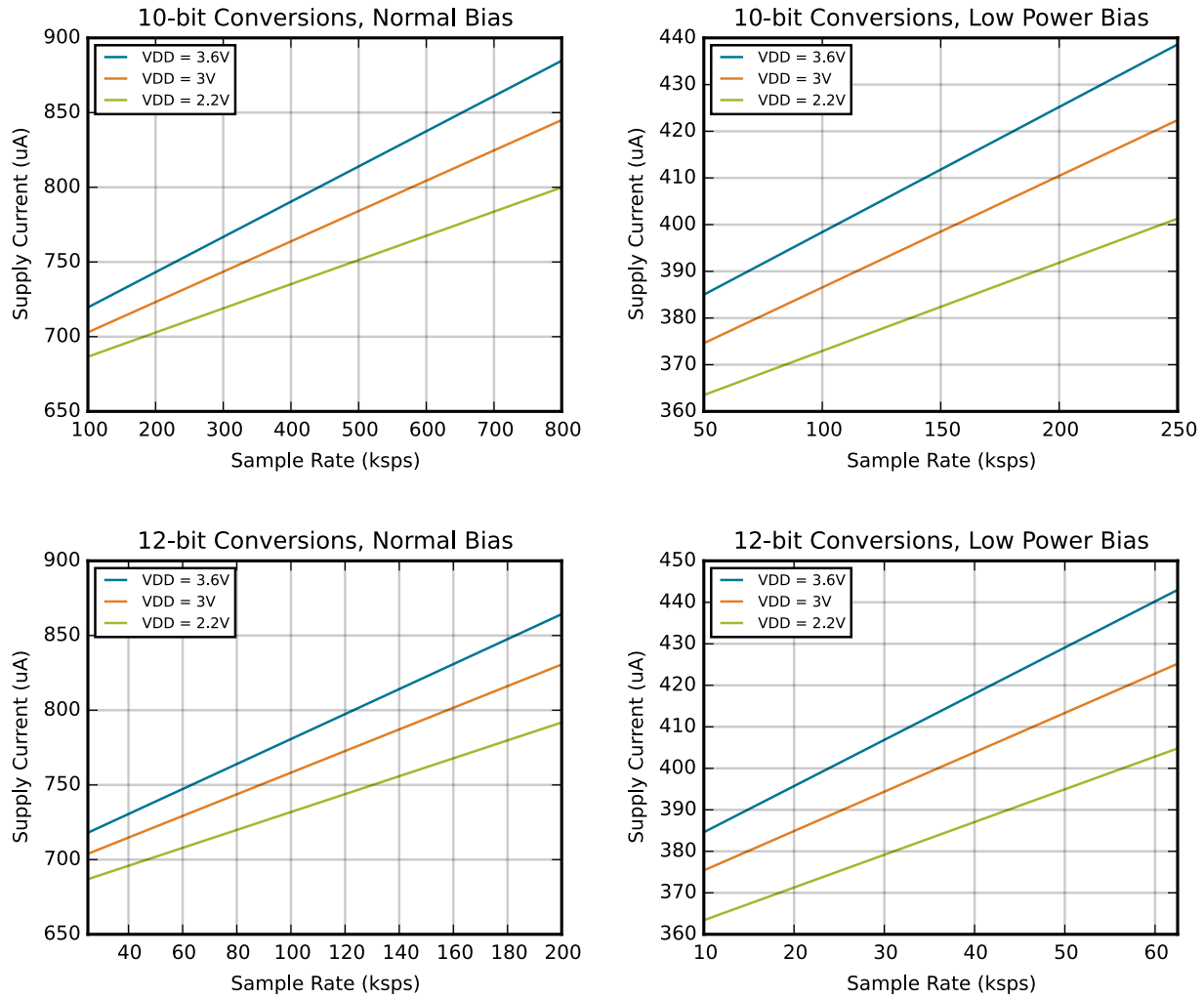


Figure 4.5. Typical ADC0 Supply Current in Normal (always-on) Mode

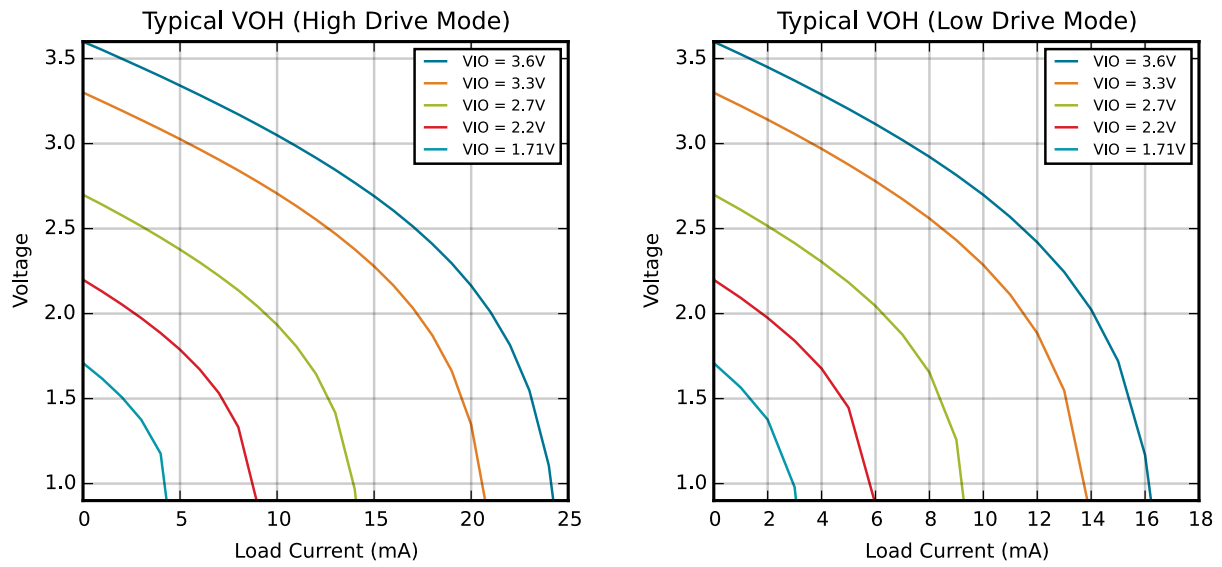


Figure 4.6. Typical VOH Curves

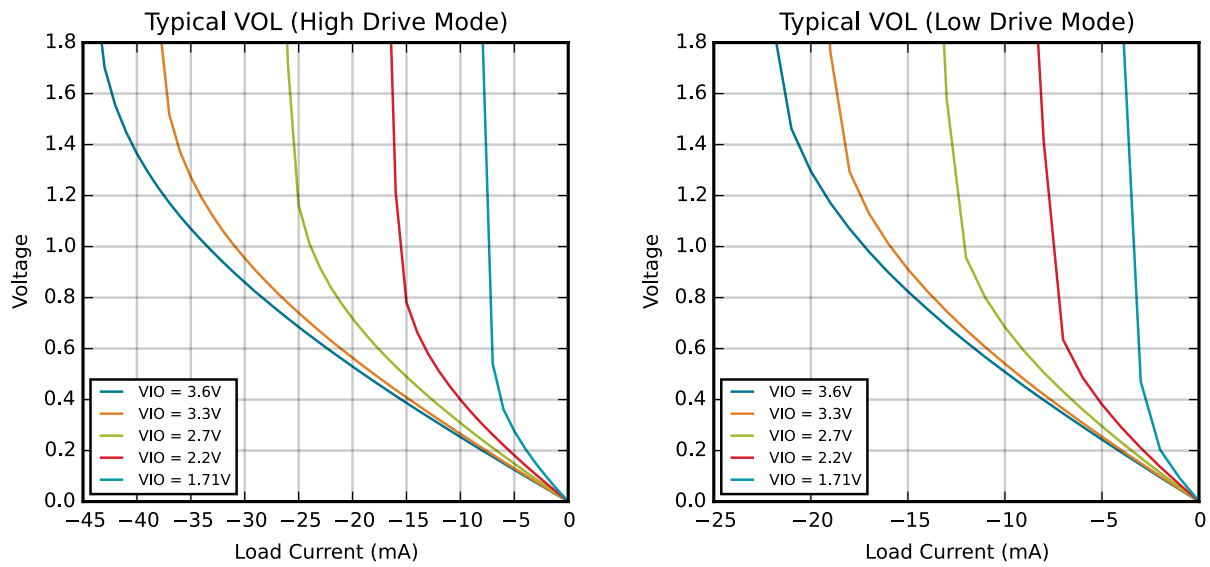


Figure 4.7. Typical VOL Curves

## 5.2 USB

Figure 5.4 Bus-Powered Connection Diagram for USB Pins on page 31 shows a typical connection bus-powered diagram for the USB pins of the EFM8UB1 devices including ESD protection diodes on the USB pins.

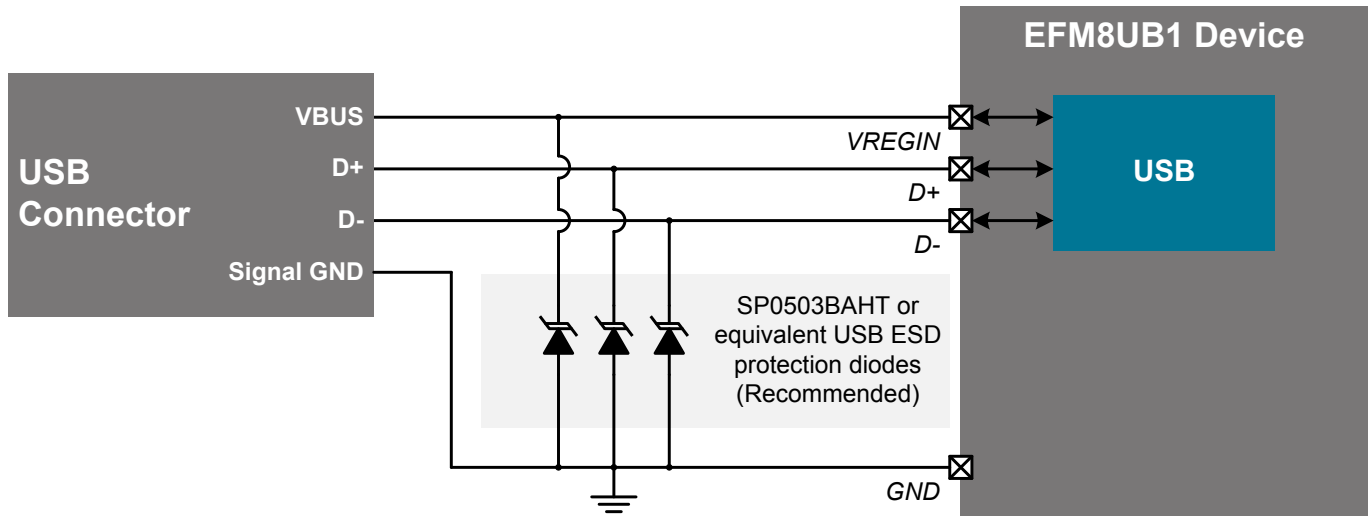


Figure 5.4. Bus-Powered Connection Diagram for USB Pins

Figure 5.5 Self-Powered Connection Diagram for USB Pins on page 31 shows a typical connection self-powered diagram for the USB pins of the EFM8UB1 devices including ESD protection diodes on the USB pins.

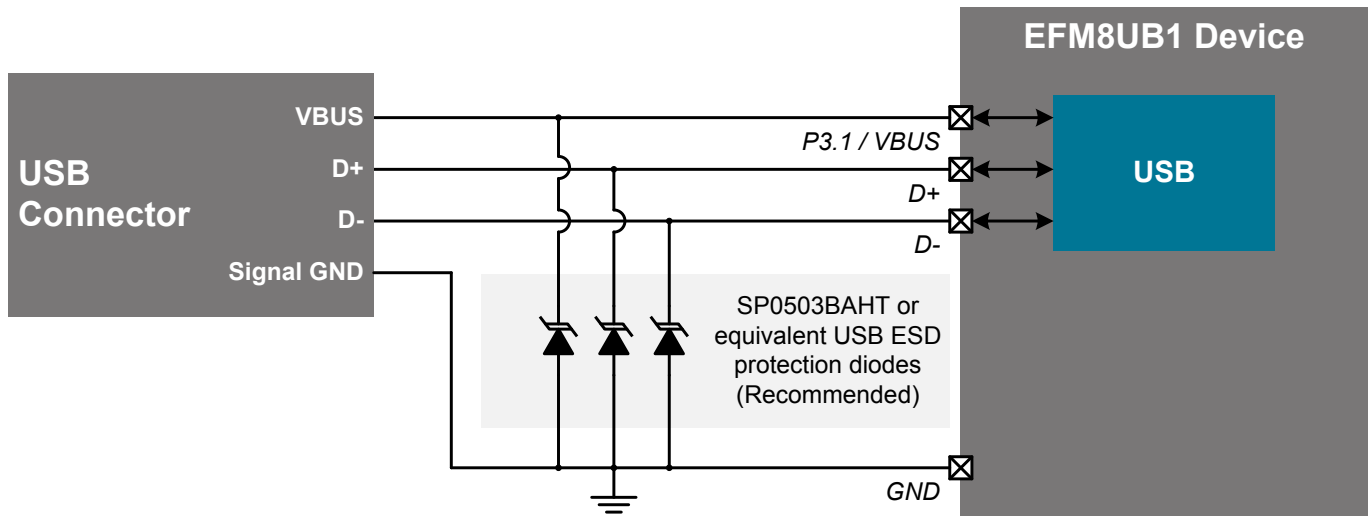


Figure 5.5. Self-Powered Connection Diagram for USB Pins

## 6.2 EFM8UB1x-QSOP24 Pin Definitions

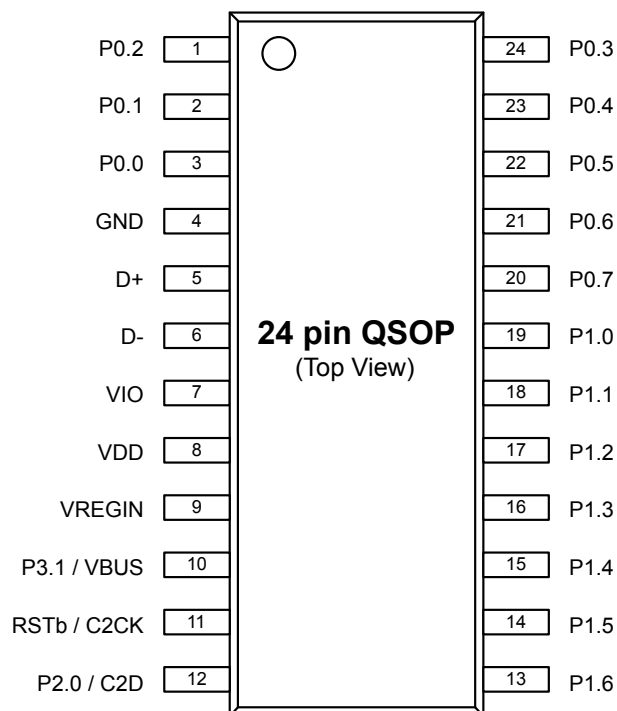


Figure 6.2. EFM8UB1x-QSOP24 Pinout

Table 6.2. Pin Definitions for EFM8UB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

7.2 QFN28 PCB Land Pattern

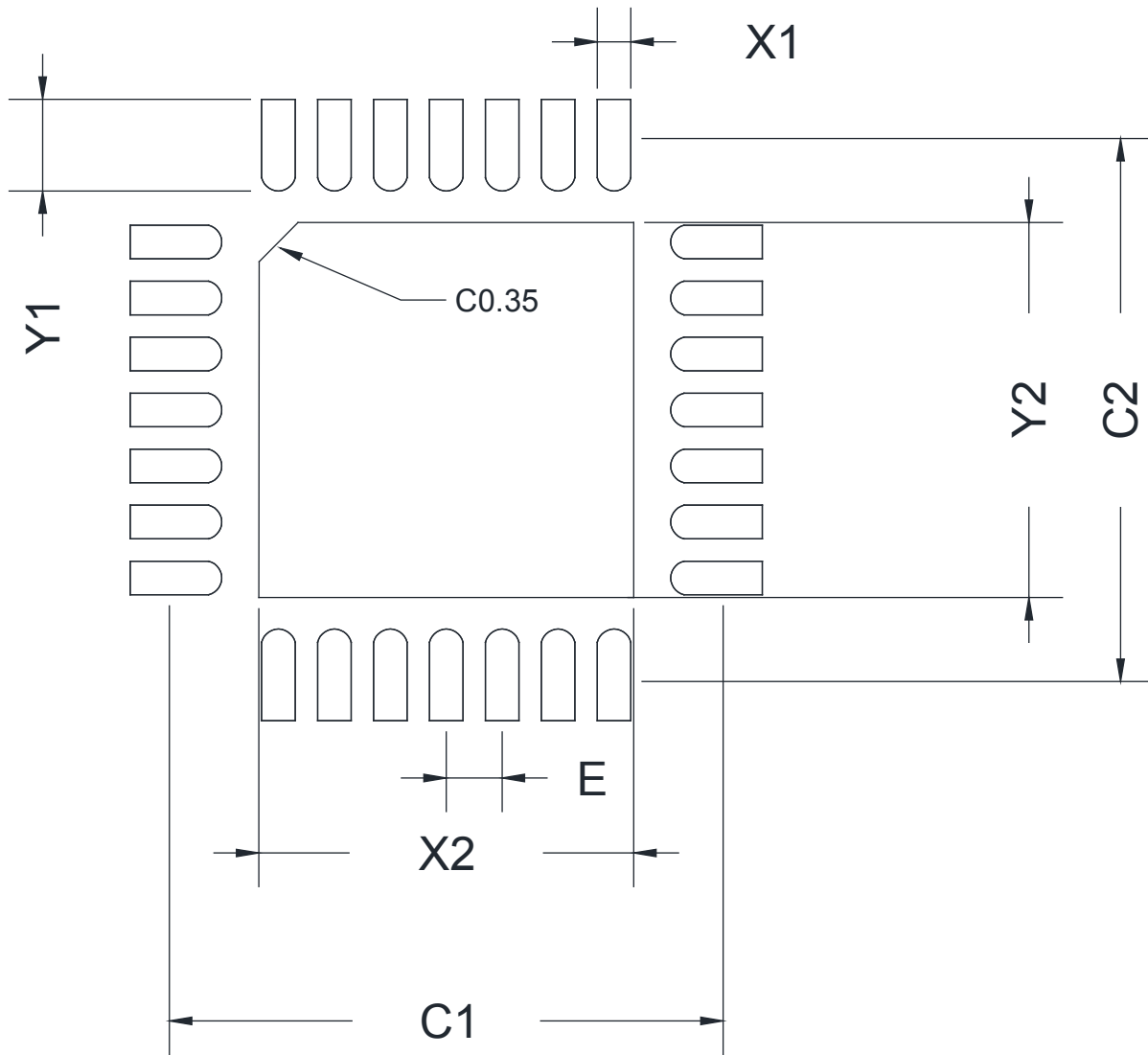


Figure 7.2. QFN28 PCB Land Pattern Drawing

Table 7.2. QFN28 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		4.80
C2		4.80
E		0.50
X1		0.30
X2		3.35
Y1		0.95



Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 8.3 QSOP24 Package Marking



Figure 8.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 9. QFN20 Package Specifications

### 9.1 QFN20 Package Dimensions

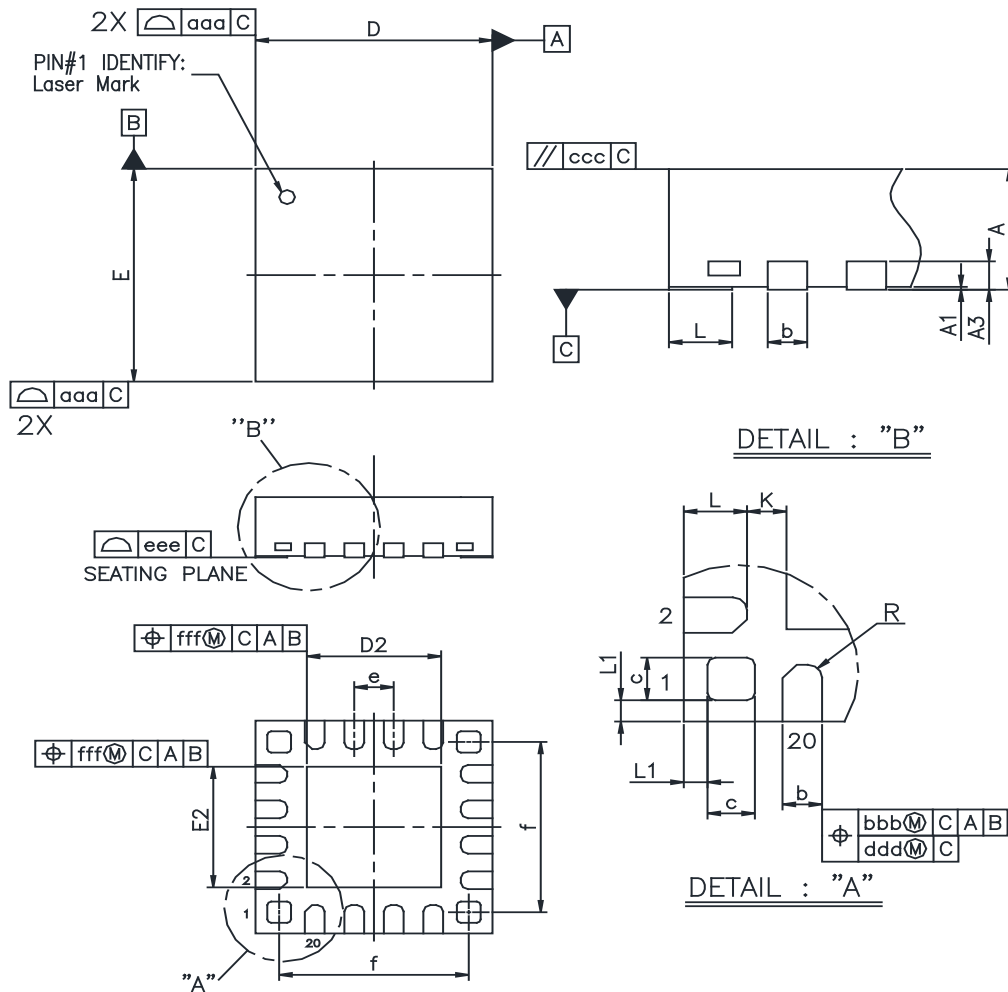


Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D	3.00 BSC		
D2	1.6	1.70	1.80
e	0.50 BSC		

9.2 QFN20 PCB Land Pattern

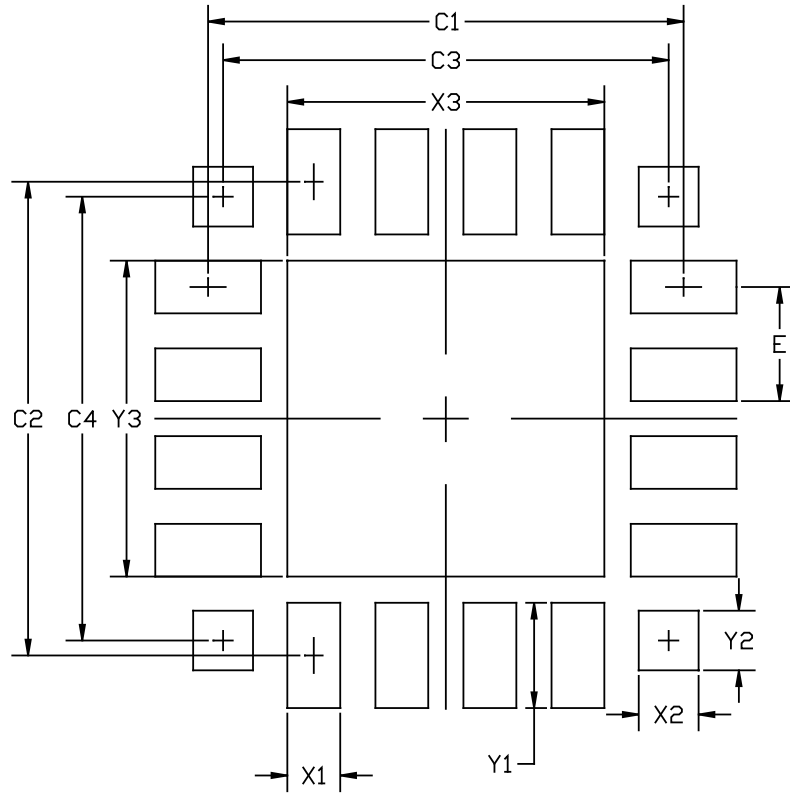


Figure 9.2. QFN20 PCB Land Pattern Drawing

Table 9.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.10
C2		3.10
C3		2.50
C4		2.50
E		0.50
X1		0.30
X2	0.25	0.35
X3		1.80
Y1		0.90
Y2	0.25	0.35
Y3		1.80

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