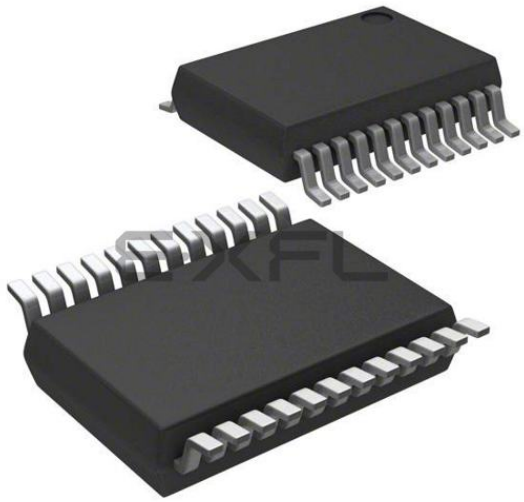
Silicon Labs - EFM8UB11F16G-C-QSOP24 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub11f16g-c-qsop24

1. Feature List

The EFM8UB1 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- Memory:
  - Up to 16 KB flash memory, in-system re-programmable from firmware, including 1 KB of 64-byte sectors and 15 KB of 512-byte sectors.
  - Up to 2304 bytes RAM (including 256 bytes standard 8051 RAM, 1024 bytes on-chip XRAM, and 1024 bytes of USB buffer)
- Power:
  - 5 V-input LDO regulator for direct connection to USB supply
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 22 total multifunction I/O pins:
  - All pins 5 V tolerant under bias
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 48 MHz oscillator with accuracy of ±1.5% standalone and ±0.25% using USB clock recovery
  - Internal 24.5 MHz oscillator with ±2% accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
- Timers/Counters and PWM:
  - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 5 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
  - USB 2.0-compliant full speed with integrated low-power transceiver, 4 bidirectional endpoints, and dedicated 1 KB buffer
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I^2C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
  - 12-Bit Analog-to-Digital Converter (ADC)
  - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded USB bootloader
- Temperature range -40 to 85 ºC
- Single power supply of 2.2 to 3.6 V or 3.0 to 5.25 V
- QSOP24, QFN28, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. The on-chip 5V-to-3.3V regulator enables operation from 2.2 V up to a 5.25 V supply. Devices are available in 28-pin QFN, 20-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

2. Ordering Information

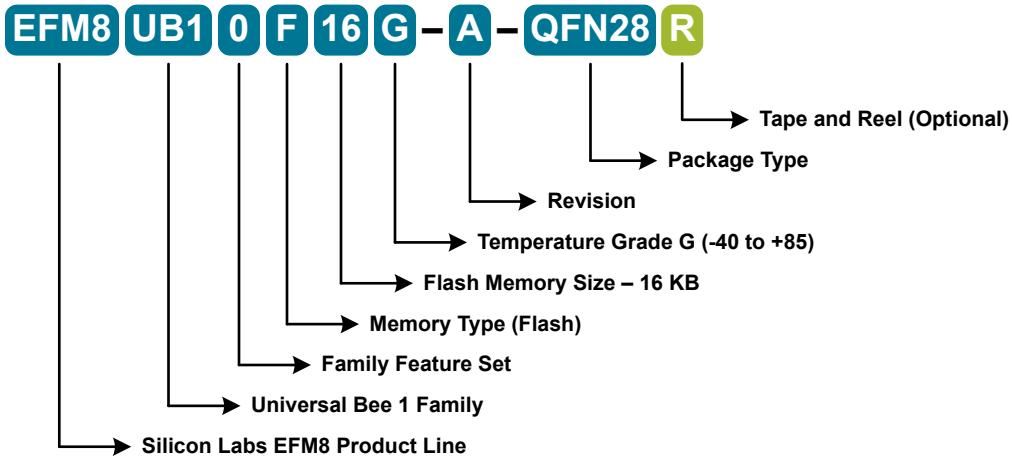

Figure 2.1. EFM8UB1 Part Numbering

All EFM8UB1 family members have the following features:

- CIP-51 Core running up to 50 MHz
- Three Internal Oscillators (48 MHz, 24.5 MHz and 80 kHz)
- USB Full/Low speed Function Controller
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 5 16-bit Timers
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- Pre-loaded USB bootloader

In addition to these features, each part number in the EFM8UB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Separate VIO and VDD Pins	Temperature Range	Package
EFM8UB10F16G-C-QFN28	16	2304	22	20	10	12	Yes	—	-40 to +85 °C	QFN28
EFM8UB11F16G-C-QSOP24	16	2304	17	15	8	9	Yes	Yes	-40 to +85 °C	QSOP24
EFM8UB10F16G-C-QFN20	16	2304	13	11	8	5	Yes	—	-40 to +85 °C	QFN20
EFM8UB10F8G-C-QFN20	8	2304	13	11	8	5	Yes	—	-40 to +85 °C	QFN20

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to ±2% over supply and temperature corners.
- 48 MHz internal oscillator (HFOSC1), accurate to ±1.5% over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive buffers to help increase throughput in faster applications

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

3.10 Bootloader

All devices come pre-programmed with a USB bootloader. This bootloader resides in the code security page and last pages of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

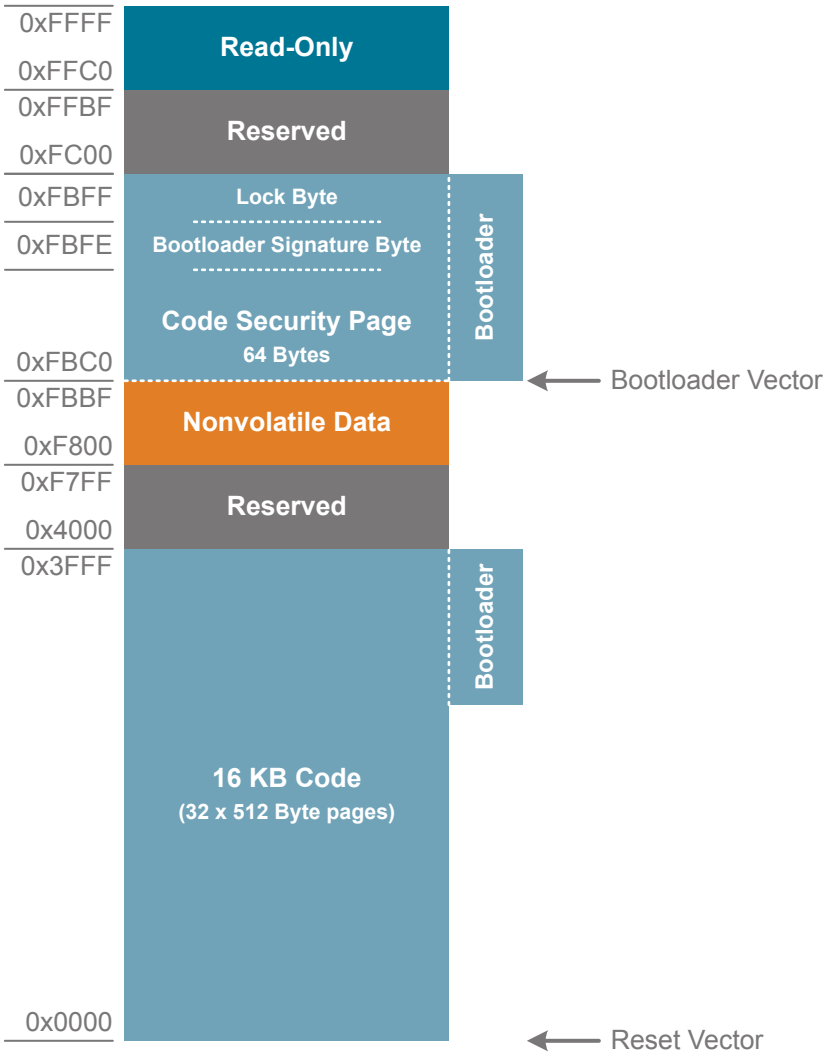

Figure 3.2. Flash Memory Map with Bootloader—16 KB Devices

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 12, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD [1]	V_{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO [3]	V_{IO}		1.71	—	V_{DD}	V
Operating Supply Voltage on VREGIN	V_{REGIN}		3.0	—	5.25	V
System Clock Frequency	f_{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation.
2. All voltages with respect to GND.
3. On devices without a VIO pin, $V_{IO} = V_{DD}$.
4. GPIO levels are undefined whenever VIO is less than 1 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on [4]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	820	1200	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	405	580	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	370	—	µA
		100 ksps, V_{DD} = 3.0 V	—	185	—	µA
		10 ksps, V_{DD} = 3.0 V	—	20	—	µA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	485	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	25	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	505	—	µA
		50 ksps, V_{DD} = 3.0 V	—	255	—	µA
		10 ksps, V_{DD} = 3.0 V	—	50	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	415	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	80	—	µA
Internal ADC0 Reference, Always-on [5]	I_{VREFFS}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	170	210	µA
Temperature Sensor	I_{TSENSE}		—	70	120	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	µA
		CPMD = 10	—	3	—	µA
		CPMD = 01	—	8.5	—	µA
		CPMD = 00	—	22.5	—	µA
Comparator Reference	I_{CPREF}		—	1.2	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.		1.1		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{IO}	V
Input Voltage Range [1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	-1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	-3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	-2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C

4.1.13 Port I/O

Table 4.13. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 3.6 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = -4.75 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -2.25 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.2 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 6.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 3.5 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Input High Voltage (all port pins including VBUS)	V_{IH}		V_{IO} - 0.6	—	—	V
Input Low Voltage (all port pins including VBUS)	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-30	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	-1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.0 V	0	5	150	µA

4.1.14 USB Transceiver

Table 4.14. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmitter						
Output High Voltage	V_{OH}	V_{DD} ≥3.0V	2.8	—	—	V
Output Low Voltage	V_{OL}	V_{DD} ≥3.0V	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	28	36	44	Ω
		Driving Low	28	36	44	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
		Low Speed (D- Pull-up)				
Output Rise Time	T_R	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Output Fall Time	T_F	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Receiver						
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

4.2 Thermal Conditions

Table 4.15. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN-20 Packages	—	60	—	°C/W
		QFN-28 Packages	—	26	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

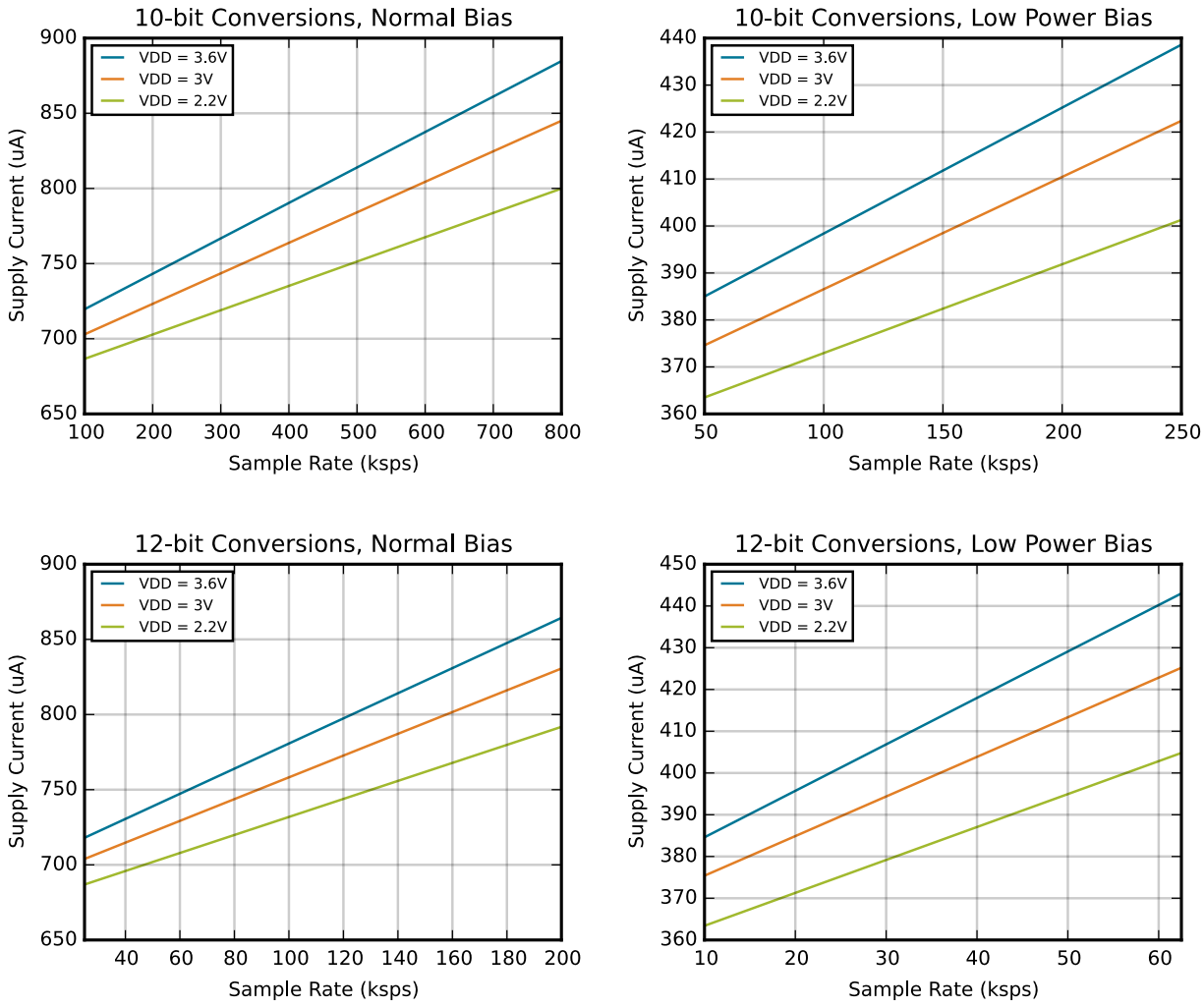

Figure 4.5. Typical ADC0 Supply Current in Normal (always-on) Mode

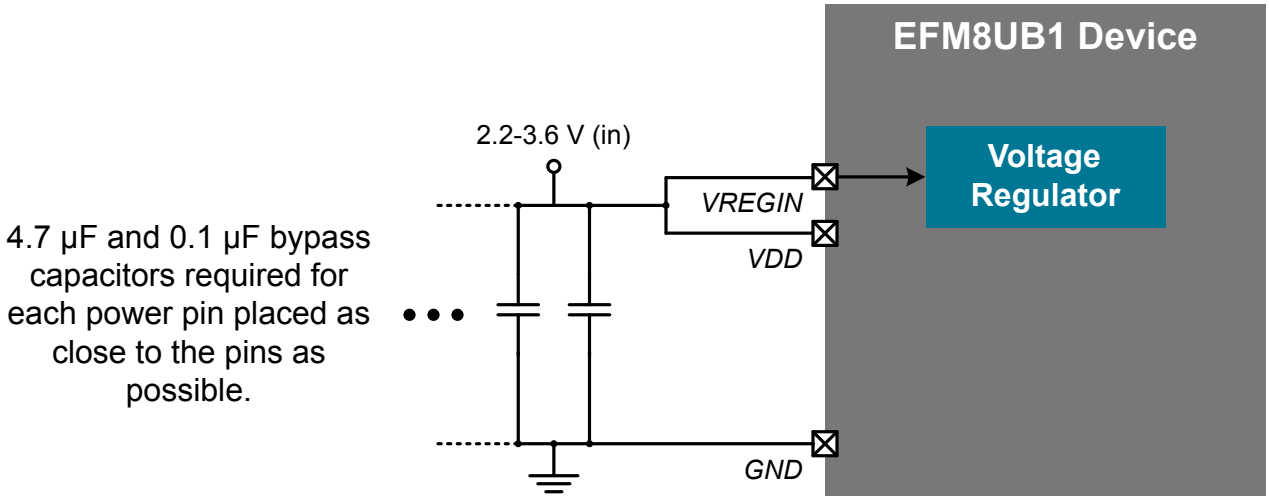

Figure 5.3. Connection Diagram with Voltage Regulator Not Used

5.2 USB

Figure 5.4 Bus-Powered Connection Diagram for USB Pins on page 31 shows a typical connection bus-powered diagram for the USB pins of the EFM8UB1 devices including ESD protection diodes on the USB pins.

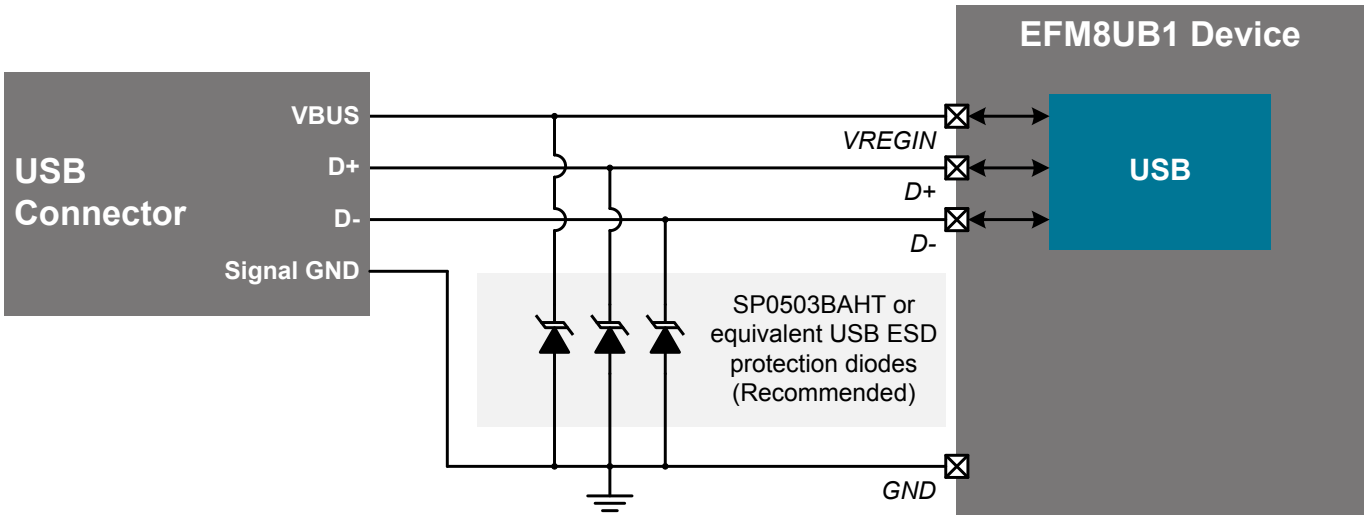

Figure 5.4. Bus-Powered Connection Diagram for USB Pins

Figure 5.5 Self-Powered Connection Diagram for USB Pins on page 31 shows a typical connection self-powered diagram for the USB pins of the EFM8UB1 devices including ESD protection diodes on the USB pins.

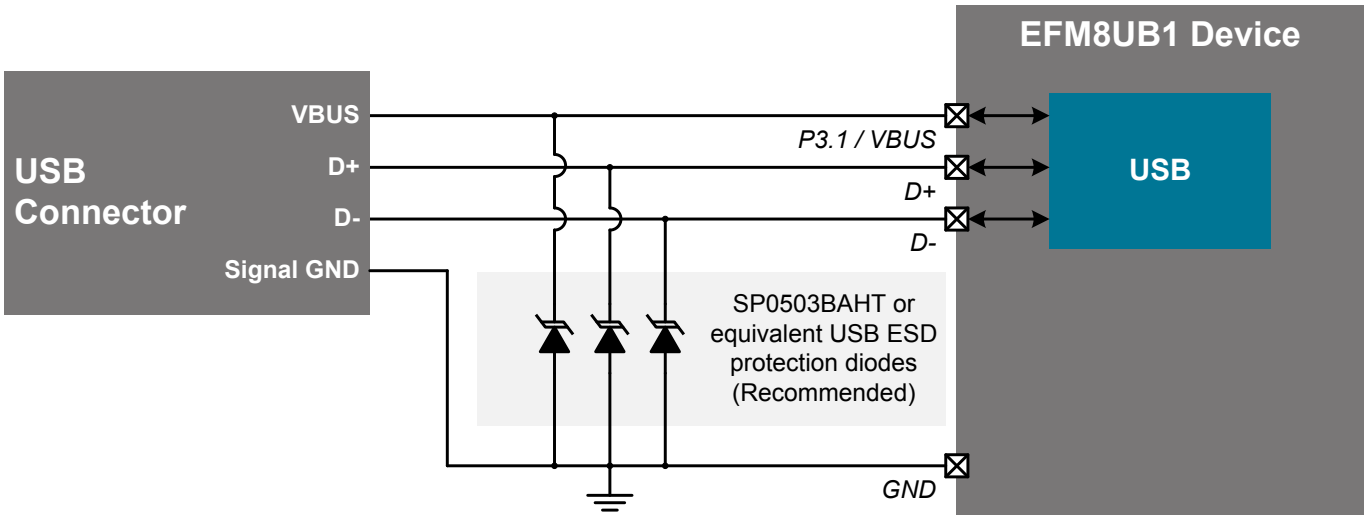

Figure 5.5. Self-Powered Connection Diagram for USB Pins

6. Pin Definitions

6.1 EFM8UB1x-QFN28 Pin Definitions

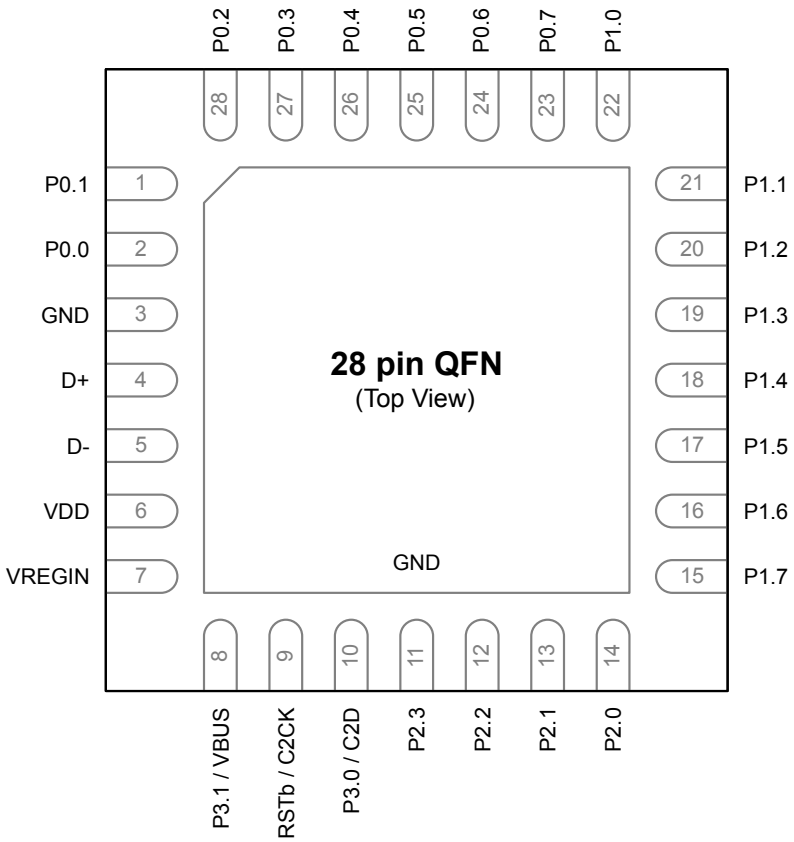

Figure 6.1. EFM8UB1x-QFN28 Pinout

Table 6.1. Pin Definitions for EFM8UB1x-QFN28

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
19	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
20	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
21	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1 CMP0P.10 CMP0N.10
22	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0 CMP0P.9 CMP0N.9
23	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
24	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
25	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5
26	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4

6.2 EFM8UB1x-QSOP24 Pin Definitions

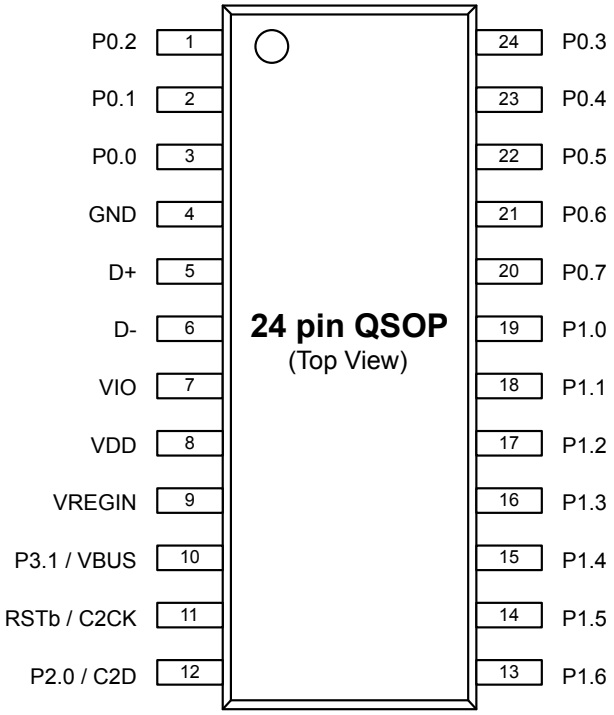

Figure 6.2. EFM8UB1x-QSOP24 Pinout

Table 6.2. Pin Definitions for EFM8UB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

Dimension	Min	Max
Y2	3.35	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.2 mm square openings on a 1.5 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN28 Package Marking

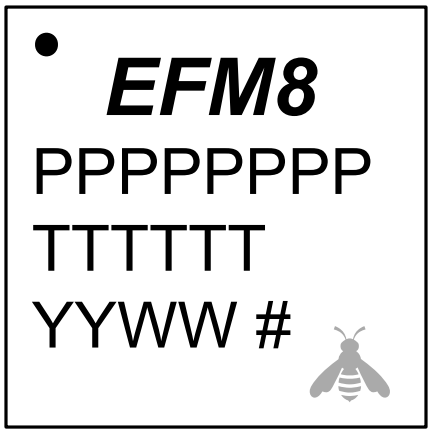

Figure 7.3. QFN28 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8.3 QSOP24 Package Marking

Figure 8.3. QSOP24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. Revision History

10.1 Revision 1.1

December 16, 2015

Updated 3.2 Power to properly reflect that a comparator falling edge wakes the device from Suspend and Snooze.

Added Note 4 to Table 4.1 Recommended Operating Conditions on page 12.

Added 5.3 Debug.

10.2 Revision 1.0

Updated any TBD numbers in 4.1 Electrical Characteristics and adjusted various specifications.

Updated VOH and VOL graphs in Figure 4.6 Typical V_{OH} Curves on page 28 and Figure 4.7 Typical V_{OL} Curves on page 28 and updated the VOH and VOL specifications in Table 4.13 Port I/O on page 22.

Added more information to 3.10 Bootloader.

Updated part numbers to Revision C.

10.3 Revision 0.3

Updated QFN20 packaging and landing diagram dimensions.

Updated QFN28 D and E minimum value.

Updated some characterization TBD values.

Added maximum allowable voltages on D+ and D- and added VBUS / P3.1 to the standard I/O row in Table 4.16 Absolute Maximum Ratings on page 24.

Added a diagram to 5.1 Power for cases when the internal 5 V-to-3.3 V regulator is not used.

Updated the 5 V-to-3.3 V regulator Electrical Characteristics table.

Added Stop mode to the Power Modes table in 3.2 Power.

10.4 Revision 0.2

Initial release.