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Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), CANbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f551-imr

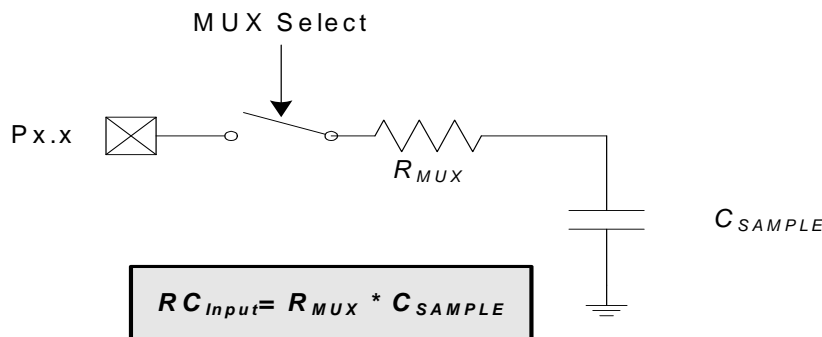


Figure 6.5. ADC0 Equivalent Input Circuit

6.3. Selectable Gain

ADC0 on the C8051F55x/56x/57x family of devices implements a selectable gain adjustment option. By writing a value to the gain adjust address range, the user can select gain values between 0 and 1.016.

For example, three analog sources to be measured have full-scale outputs of 5.0 V, 4.0 V, and 3.0 V, respectively. Each ADC measurement would ideally use the full dynamic range of the ADC with an internal voltage reference of 1.5 V or 2.2 V (set to 2.2 V for this example). When selecting the first source (5.0 V full-scale), a gain value of 0.44 (5 V full scale x 0.44 = 2.2 V full scale) provides a full-scale signal of 2.2 V when the input signal is 5.0 V. Likewise, a gain value of 0.55 (4 V full scale x 0.55 = 2.2 V full scale) for the second source and 0.73 (3 V full scale x 0.73 = 2.2 V full scale) for the third source provide full-scale ADC0 measurements when the input signal is full-scale.

Additionally, some sensors or other input sources have small part-to-part variations that must be accounted for to achieve accurate results. In this case, the programmable gain value could be used as a calibration value to eliminate these part-to-part variations.

6.3.1. Calculating the Gain Value

The ADC0 selectable gain feature is controlled by 13 bits in three registers. ADC0GNH contains the 8 upper bits of the gain value and ADC0GNL contains the 4 lower bits of the gain value. The final GAINADD bit (ADC0GNA.0) controls an optional extra 1/64 (0.016) of gain that can be added in addition to the ADC0GNH and ADC0GNL gain. The ADC0GNA.0 bit is set to 1 after a power-on reset.

The equivalent gain for the ADC0GNH, ADC0GNL and ADC0GNA registers is as follows:

$$\text{gain} = \left(\frac{\text{GAIN}}{4096} \right) + \text{GAINADD} \times \left(\frac{1}{64} \right)$$

Equation 6.2. Equivalent Gain from the ADC0GNH and ADC0GNL Registers

Where:

GAIN is the 12-bit word of ADC0GNH[7:0] and ADC0GNL[7:4]

GAINADD is the value of the GAINADD bit (ADC0GNA.0)

gain is the equivalent gain value from 0 to 1.016

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For example, if ADC0GNH = 0xFC, ADC0GNL = 0x00, and GAINADD = 1, GAIN = 0xFC0 = 4032, and the resulting equation is as follows:

$$\text{GAIN} = \left(\frac{4032}{4096}\right) + 1 \times \left(\frac{1}{64}\right) = 0.984 + 0.016 = 1.0$$

The table below equates values in the ADC0GNH, ADC0GNL, and ADC0GNA registers to the equivalent gain using this equation.

ADC0GNH Value	ADC0GNL Value	GAINADD Value	GAIN Value	Equivalent Gain
0xFC (default)	0x00 (default)	1 (default)	4032 + 64	1.0 (default)
0x7C	0x00	1	1984 + 64	0.5
0xBC	0x00	1	3008 + 64	0.75
0x3C	0x00	1	960 + 64	0.25
0xFF	0xF0	0	4095 + 0	~1.0
0xFF	0xF0	1	4096 + 64	1.016

For any desired gain value, the GAIN registers can be calculated by the following:

$$\text{GAIN} = \left(\text{gain} - \text{GAINADD} \times \left(\frac{1}{64}\right)\right) \times 4096$$

Equation 6.3. Calculating the ADC0GNH and ADC0GNL Values from the Desired Gain

Where:

GAIN is the 12-bit word of ADC0GNH[7:0] and ADC0GNL[7:4]

GAINADD is the value of the GAINADD bit (ADC0GNA.0)

gain is the equivalent gain value from 0 to 1.016

When calculating the value of GAIN to load into the ADC0GNH and ADC0GNL registers, the GAINADD bit can be turned on or off to reach a value closer to the desired gain value.

For example, the initial example in this section requires a gain of 0.44 to convert 5 V full scale to 2.2 V full scale. Using Equation 6.3:

$$\text{GAIN} = \left(0.44 - \text{GAINADD} \times \left(\frac{1}{64}\right)\right) \times 4096$$

If GAINADD is set to 1, this makes the equation:

$$\text{GAIN} = \left(0.44 - 1 \times \left(\frac{1}{64}\right)\right) \times 4096 = 0.424 \times 4096 = 1738 = 0x06CA$$

The actual gain from setting GAINADD to 1 and ADC0GNH and ADC0GNL to 0x6CA is 0.4399. A similar gain can be achieved if GAINADD is set to 0 with a different value for ADC0GNH and ADC0GNL.

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SFR Definition 6.13. ADC0MX: ADC0 Channel Select

Bit	7	6	5	4	3	2	1	0
Name								ADC0MX[5:0]
Type	R	R						R/W
Reset	0	0	1	1	1	1	1	1

SFR Address = 0xBB; SFR Page = 0x00;

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5:0	AMX0P[5:0]	AMUX0 Positive Input Selection. 000000: P0.0 000001: P0.1 000010: P0.2 000011: P0.3 000100: P0.4 000101: P0.5 000110: P0.6 000111: P0.7 001000: P1.0 001001: P1.1 001010: P1.2 001011: P1.3 001100: P1.4 001101: P1.5 001110: P1.6 001111: P1.7 010000: P2.0 010001: P2.1 010010: P2.2 (Only available on 40-pin and 32-pin package devices) 010011: P2.3 (Only available on 40-pin and 32-pin package devices) 010100: P2.4 (Only available on 40-pin and 32-pin package devices) 010101: P2.5 (Only available on 40-pin and 32-pin package devices) 010110: P2.6 (Only available on 40-pin and 32-pin package devices) 010111: P2.7 (Only available on 40-pin and 32-pin package devices) 011000: P3.0 (Only available on 40-pin and 32-pin package devices) 011001: P3.1 (Only available on 40-pin package devices) 011010: P3.2 (Only available on 40-pin package devices) 011011: P3.3 (Only available on 40-pin package devices) 011100: P3.4 (Only available on 40-pin package devices) 011101: P3.5 (Only available on 40-pin package devices) 011110: P3.6 (Only available on 40-pin package devices) 011111: P3.7 (Only available on 40-pin package devices) 100000–101111: Reserved 110000: Temp Sensor 110001: V _{DD} 110010–111111: GND

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SFR Definition 7.1. REF0CN: Reference Control

Bit	7	6	5	4	3	2	1	0
Name			ZTCEN	REFLV	REFSL	TEMPE	BIASE	REFBE
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD1; SFR Page = 0x00

Bit	Name	Function
7:6	Unused	Read = 00b; Write = don't care.
5	ZTCEN	Zero Temperature Coefficient Bias Enable Bit. This bit must be set to 1b before entering oscillator suspend mode. 0: ZeroTC Bias Generator automatically enabled when required. 1: ZeroTC Bias Generator forced on.
4	REFLV	Voltage Reference Output Level Select. This bit selects the output voltage level for the internal voltage reference 0: Internal voltage reference set to 1.5 V. 1: Internal voltage reference set to 2.20 V.
3	REFSL	Voltage Reference Select. This bit selects the ADCs voltage reference. 0: V_{REF} pin used as voltage reference. 1: V_{DD} used as voltage reference. If V_{DD} is selected as the voltage reference and the ADC is enabled in the ADC0CN register, the P0.0/VREF pin cannot operate as a general purpose I/O pin in open-drain mode. With the above settings, this pin can operate in push-pull output mode or as an analog input.
2	TEMPE	Temperature Sensor Enable Bit. 0: Internal Temperature Sensor off. 1: Internal Temperature Sensor on.
1	BIASE	Internal Analog Bias Generator Enable Bit. 0: Internal Bias Generator off. 1: Internal Bias Generator on.
0	REFBE	On-chip Reference Buffer Enable Bit. 0: On-chip Reference Buffer off. 1: On-chip Reference Buffer on. Internal voltage reference driven on the V_{REF} pin.

8. Comparators

The C8051F55x/56x/57x devices include two on-chip programmable voltage Comparators. A block diagram of the comparators is shown in Figure 8.1, where “n” is the comparator number (0 or 1). The two Comparators operate identically except that Comparator0 can also be used a reset source. For input selection details, refer to SFR Definition 8.5 and SFR Definition 8.6.

Each Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0, CP1), or an asynchronous “raw” output (CP0A, CP1A). The asynchronous signal is available even when the system clock is not active. This allows the Comparators to operate and generate an output with the device in STOP mode. When assigned to a Port pin, the Comparator outputs may be configured as open drain or push-pull (see Section “19.4. Port I/O Initialization” on page 174). Comparator0 may also be used as a reset source (see Section “16.5. Comparator0 Reset” on page 142).

The Comparator0 inputs are selected in the CPT0MX register (SFR Definition 8.5). The CMX0P1-CMX0P0 bits select the Comparator0 positive input; the CMX0N1-CMX0N0 bits select the Comparator0 negative input. The Comparator1 inputs are selected in the CPT1MX register (SFR Definition 8.6). The CMX1P1-CMX1P0 bits select the Comparator1 positive input; the CMX1N1-CMX1N0 bits select the Comparator1 negative input.

Important Note About Comparator Inputs: The Port pins selected as Comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “19.1. Port I/O Modes of Operation” on page 170).

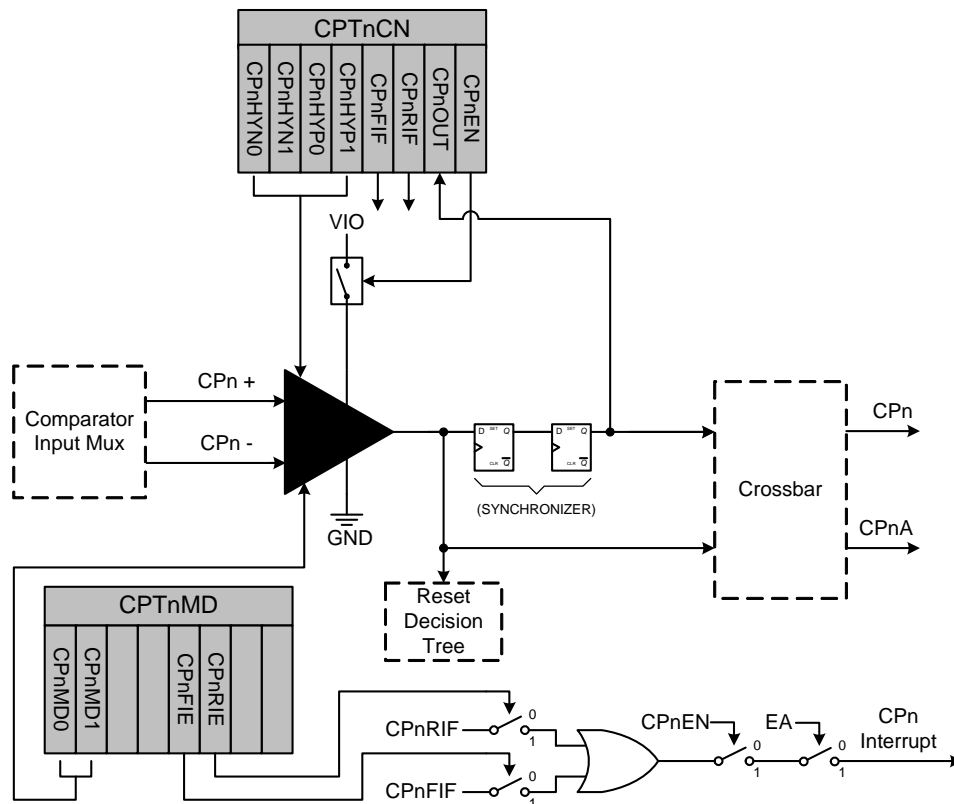


Figure 8.1. Comparator Functional Block Diagram

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SFR Definition 12.1. SFR0CN: SFR Page Control

Bit	7	6	5	4	3	2	1	0
Name								SFRPGEN
Type	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	0	0	0	1

SFR Address = 0x84; SFR Page = 0x0F

Bit	Name	Function
7:1	Unused	Read = 0000000b; Write = Don't Care
0	SFRPGEN	SFR Automatic Page Control Enable. Upon interrupt, the C8051 Core will vector to the specified interrupt service routine and automatically switch the SFR page to the corresponding peripheral or function's SFR page. This bit is used to control this autopaging function. 0: SFR Automatic Paging disabled. The C8051 core will not automatically change to the appropriate SFR page (i.e., the SFR page that contains the SFRs for the peripheral/function that was the source of the interrupt). 1: SFR Automatic Paging enabled. Upon interrupt, the C8051 will switch the SFR page to the page that contains the SFRs for the peripheral or function that is the source of the interrupt.

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SFR Definition 12.3. SFRNEXT: SFR Next

Bit	7	6	5	4	3	2	1	0
Name	SFRNEXT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x85; SFR Page = All Pages

Bit	Name	Function
7:0	SFRNEXT[7:0]	<p>SFR Page Bits.</p> <p>This is the value that will go to the SFR Page register upon a return from interrupt.</p> <p>Write: Sets the SFR Page contained in the second byte of the SFR Stack. This will cause the SFRPAGE SFR to have this SFR page value upon a return from interrupt.</p> <p>Read: Returns the value of the SFR page contained in the second byte of the SFR stack.</p> <p>SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFRLAST is the third entry. The SFR stack bytes may be used alter the context in the SFR Page Stack, and will not cause the stack to “push” or “pop”. Only interrupts and return from interrupts cause pushes and pops of the SFR Page Stack.</p>

Table 12.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
IT01CF	0xE4	INT0/INT1 Configuration	123
LIN0ADR	0xD3	LIN0 Address	200
LIN0CF	0xC9	LIN0 Configuration	200
LIN0DAT	0xD2	LIN0 Data	201
OSICN	0xA1	Internal Oscillator Control	160
OSICRS	0xA2	Internal Oscillator Coarse Control	161
OSCIFIN	0x9E	Internal Oscillator Fine Calibration	161
OSXCN	0x9F	External Oscillator Control	165
P0	0x80	Port 0 Latch	183
P0MASK	0xF2	Port 0 Mask Configuration	179
P0MAT	0xF1	Port 0 Match Configuration	179
P0MDIN	0xF1	Port 0 Input Mode Configuration	184
P0MDOUT	0xA4	Port 0 Output Mode Configuration	184
P0SKIP	0xD4	Port 0 Skip	185
P1	0x90	Port 1 Latch	185
P1MASK	0xF4	Port 1 Mask Configuration	180
P1MAT	0xF3	Port 1 Match Configuration	180
P1MDIN	0xF2	Port 1 Input Mode Configuration	186
P1MDOUT	0xA5	Port 1 Output Mode Configuration	186
P1SKIP	0xD5	Port 1 Skip	187
P2	0xA0	Port 2 Latch	187
P2MASK	0xB2	Port 2 Mask Configuration	181
P2MAT	0xB1	Port 2 Match Configuration	181
P2MDIN	0xF3	Port 2 Input Mode Configuration	188
P2MDOUT	0xA6	Port 2 Output Mode Configuration	188
P2SKIP	0xD6	Port 2 Skip	189
P3	0xB0	Port 3 Latch	189
P3MASK	0xAF	Port 3 Mask Configuration	182
P3MAT	0xAE	Port 3 Match Configuration	182
P3MDIN	0xF4	Port 3 Input Mode Configuration	190
P3MDOUT	0xAE	Port 3 Output Mode Configuration	190
P3SKIP	0xD7	Port 3 Skip	191
P4	0xB5	Port 4 Latch	191
P4MDOUT	0xAF	Port 4 Output Mode Configuration	192
PCA0CN	0xD8	PCA Control	294
PCA0CPH0	0xFC	PCA Capture 0 High	299

13.2. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described in this section. Refer to the data sheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

SFR Definition 13.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	ELIN0	ET3	ECP1	ECP0	EPCA0	EADC0	EWADC0	ESMB0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE6; SFR Page = All Pages

Bit	Name	Function
7	ELIN0	Enable LIN0 Interrupt. This bit sets the masking of the LIN0 interrupt. 0: Disable LIN0 interrupts. 1: Enable interrupt requests generated by the LIN0INT flag.
6	ET3	Enable Timer 3 Interrupt. This bit sets the masking of the Timer 3 interrupt. 0: Disable Timer 3 interrupts. 1: Enable interrupt requests generated by the TF3L or TF3H flags.
5	ECP1	Enable Comparator1 (CP1) Interrupt. This bit sets the masking of the CP1 interrupt. 0: Disable CP1 interrupts. 1: Enable interrupt requests generated by the CP1RIF or CP1FIF flags.
4	ECP0	Enable Comparator0 (CP0) Interrupt. This bit sets the masking of the CP0 interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the CP0RIF or CP0FIF flags.
3	EPCA0	Enable Programmable Counter Array (PCA0) Interrupt. This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
2	EADC0	Enable ADC0 Conversion Complete Interrupt. This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the AD0INT flag.
1	EWADC0	Enable Window Comparison ADC0 Interrupt. This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (AD0WINT).
0	ESMB0	Enable SMBus (SMB0) Interrupt. This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

17.6.1.2. 8-bit MOVX without Bank Select: EMI0CF[4:2] = 001 or 011

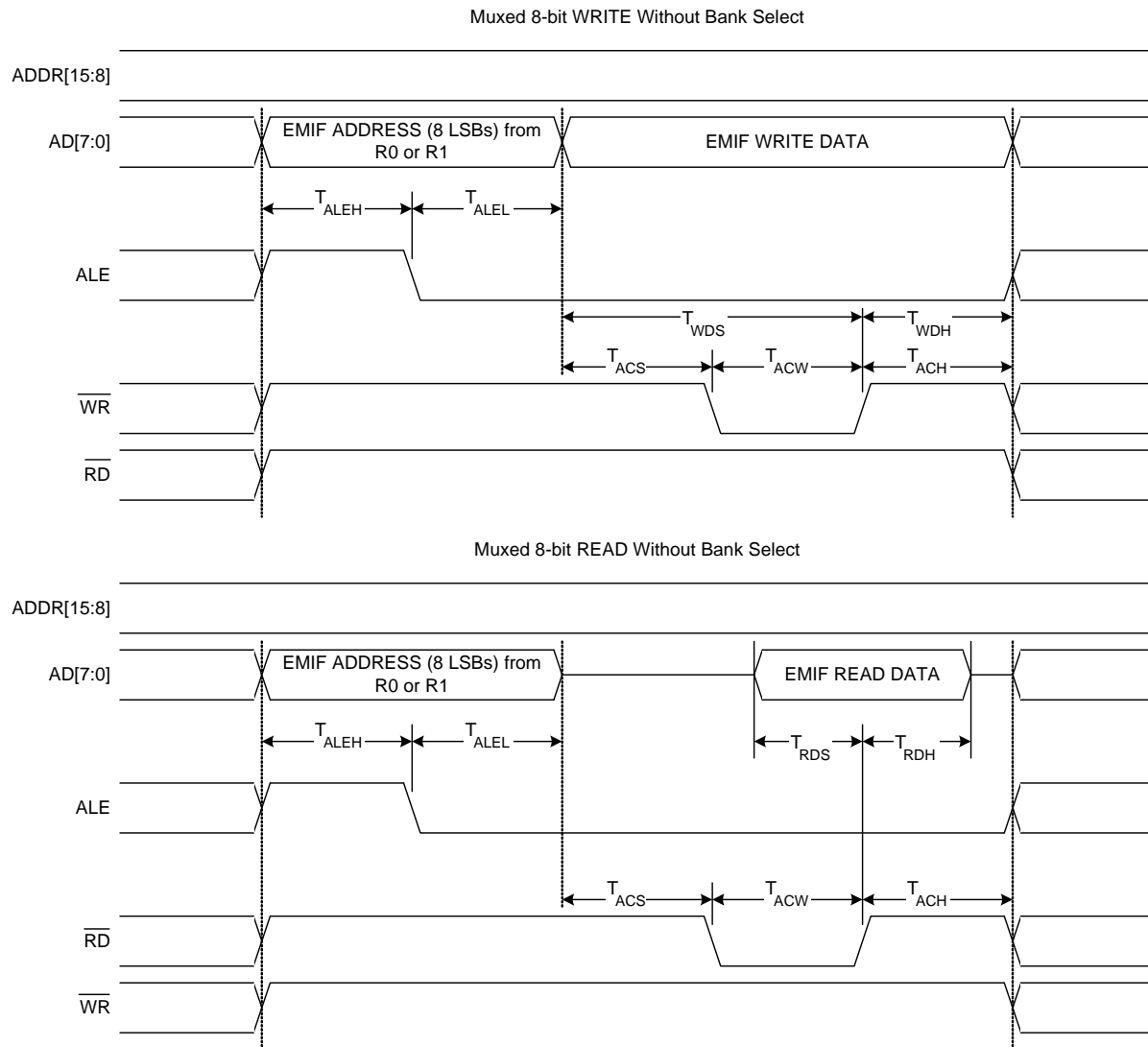


Figure 17.4. Multiplexed 8-bit MOVX without Bank Select Timing

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SFR Definition 19.1. XBR0: Port I/O Crossbar Register 0

Bit	7	6	5	4	3	2	1	0
Name	CP1AE	CP1E	CP0AE	CP0E	SMB0E	SPI0E	CAN0E	URT0E
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE1; SFR Page = 0x0F

Bit	Name	Function
7	CP1AE	Comparator1 Asynchronous Output Enable. 0: Asynchronous CP1 unavailable at Port pin. 1: Asynchronous CP1 routed to Port pin.
6	CP1E	Comparator1 Output Enable. 0: CP1 unavailable at Port pin. 1: CP1 routed to Port pin.
5	CP0AE	Comparator0 Asynchronous Output Enable. 0: Asynchronous CP0 unavailable at Port pin. 1: Asynchronous CP0 routed to Port pin.
4	CP0E	Comparator0 Output Enable. 0: CP0 unavailable at Port pin. 1: CP0 routed to Port pin.
3	SMB0E	SMBus I/O Enable. 0: SMBus I/O unavailable at Port pins. 1: SMBus I/O routed to Port pins.
2	SPI0E	SPI I/O Enable. 0: SPI I/O unavailable at Port pins. 1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO pins.
1	CAN0E	CAN I/O Output Enable. 0: CAN I/O unavailable at Port pins. 1: CAN_TX, CAN_RX routed to Port pins P0.6 and P0.7.
0	URT0E	UART I/O Output Enable. 0: UART I/O unavailable at Port pin. 1: UART TX0, RX0 routed to Port pins P0.4 and P0.5.

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21.2.4. CAN Register Assignment

The standard Bosch CAN registers are mapped to SFR space as shown below and their full definitions are available in the CAN User's Guide. The name shown in the Name column matches what is provided in the CAN User's Guide. One additional SFR which is not a standard Bosch CAN register, CAN0CFG, is provided to configure the CAN clock. All CAN registers are located on SFR Page 0x0C.

Table 21.2. Standard CAN Registers and Reset Values

CAN Addr.	Name	SFR Name (High)	SFR Addr.	SFR Name (Low)	SFR Addr.	16-bit SFR	Reset Value
0x00	CAN Control Register	—	—	CAN0CN	0xC0	—	0x01
0x02	Status Register	—	—	CAN0STAT	0x94	—	0x00
0x04	Error Counter ¹	CAN0ERRH	0x97	CAN0ERRL	0x96	CAN0ERR	0x0000
0x06	Bit Timing Register ²	CAN0BTH	0x9B	CAN0BTL	0x9A	CAN0BT	0x2301
0x08	Interrupt Register ¹	CAN0IIDH	0x9D	CAN0IIDL	0x9C	CAN0IID	0x0000
0x0A	Test Register	—	—	CAN0TST	0x9E	—	0x00 ^{3,4}
0x0C	BRP Extension Register ²	—	—	CAN0BRPE	0xA1	—	0x00
0x10	IF1 Command Request	CAN0IF1CRH	0xBF	CAN0IF1CRL	0xBE	CAN0IF1CR	0x0001
0x12	IF1 Command Mask	CAN0IF1CMH	0xC3	CAN0IF1CML	0xC2	CAN0IF1CM	0x0000
0x14	IF1 Mask 1	CAN0IF1M1H	0xC5	CAN0IF1M1L	0xC4	CAN0IF1M1	0xFFFF
0x16	IF1 Mask 2	CAN0IF1M2H	0xC7	CAN0IF1M2L	0xC6	CAN0IF1M2	0xFFFF
0x18	IF1 Arbitration 1	CAN0IF1A1H	0xCB	CAN0IF1A1L	0xCA	CAN0IF1A1	0x0000
0x1A	IF1 Arbitration 2	CAN0IF1A2H	0xCD	CAN0IF1A2L	0xCC	CAN0IF1A2	0x0000
0x1C	IF1 Message Control	CAN0IF1MCH	0xD3	CAN0IF1MCL	0xD2	CAN0IF1MC	0x0000
0x1E	IF1 Data A 1	CAN0IF1DA1H	0xD5	CAN0IF1DA1L	0xD4	CAN0IF1DA1	0x0000
0x20	IF1 Data A 2	CAN0IF1DA2H	0xD7	CAN0IF1DA2L	0xD6	CAN0IF1DA2	0x0000
0x22	IF1 Data B 1	CAN0IF1DB1H	0xDB	CAN0IF1DB1L	0xDA	CAN0IF1DB1	0x0000
0x24	IF1 Data B 2	CAN0IF1DB2H	0xDD	CAN0IF1DB2L	0xDC	CAN0IF1DB2	0x0000
0x40	IF2 Command Request	CAN0IF2CRH	0xDF	CAN0IF2CRL	0xDE	CAN0IF2CR	0x0001
0x42	IF2 Command Mask	CAN0IF2CMH	0xE3	CAN0IF2CML	0xE2	CAN0IF2CM	0x0000
0x44	IF2 Mask 1	CAN0IF2M1H	0xEB	CAN0IF2M1L	0xEA	CAN0IF2M1	0xFFFF
0x46	IF2 Mask 2	CAN0IF2M2H	0xED	CAN0IF2M2L	0xEC	CAN0IF2M2	0xFFFF
0x48	IF2 Arbitration 1	CAN0IF2A1H	0xEF	CAN0IF2A1L	0xEE	CAN0IF2A1	0x0000
0x4A	IF2 Arbitration 2	CAN0IF2A2H	0xF3	CAN0IF2A2L	0xF2	CAN0IF2A2	0x0000
0x4C	IF2 Message Control	CAN0IF2MCH	0xCF	CAN0IF2MCL	0xCE	CAN0IF2MC	0x0000
0x4E	IF2 Data A 1	CAN0IF2DA1H	0xF7	CAN0IF2DA1L	0xF6	CAN0IF2DA1	0x0000
Notes: <ol style="list-style-type: none"> 1. Read-only register. 2. Write-enabled by CCE. 3. The reset value of CAN0TST could also be r0000000b, where r signifies the value of the CAN RX pin. 4. Write-enabled by Test. 							

SFR Definition 23.2. SMOD0: Serial Port 0 Control

Bit	7	6	5	4	3	2	1	0
Name	MCE0	S0PT[1:0]		PE0	S0DL[1:0]		XBE0	SBL0
Type	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	0	0

SFR Address = 0xA9; SFR Page = 0x00

Bit	Name	Function
7	MCE0	Multiprocessor Communication Enable. 0: RI0 will be activated if stop bit(s) are 1. 1: RI0 will be activated if stop bit(s) and extra bit are 1. Extra bit must be enabled using XBE0.
6:5	S0PT[1:0]	Parity Type Select Bits. 00: Odd Parity 01: Even Parity 10: Mark Parity 11: Space Parity.
4	PE0	Parity Enable. This bit enables hardware parity generation and checking. The parity type is selected by bits S0PT[1:0] when parity is enabled. 0: Hardware parity is disabled. 1: Hardware parity is enabled.
3:2	S0DL[1:0]	Data Length. 00: 5-bit data 01: 6-bit data 10: 7-bit data 11: 8-bit data
1	XBE0	Extra Bit Enable. When enabled, the value of TBX0 will be appended to the data field 0: Extra Bit is disabled. 1: Extra Bit is enabled.
0	SBL0	Stop Bit Length. 0: Short—stop bit is active for one bit time 1: Long—stop bit is active for two bit times (data length = 6, 7, or 8 bits), or 1.5 bit times (data length = 5 bits).

This mode allows software to determine the external oscillator frequency when an RC network or capacitor is used to generate the clock source.

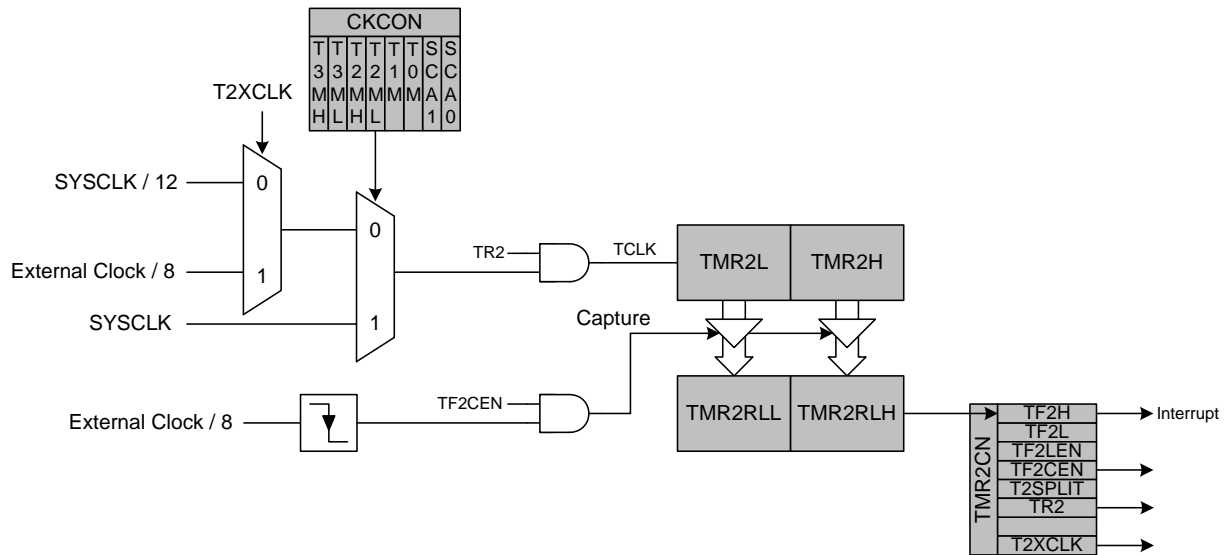


Figure 25.6. Timer 2 External Oscillator Capture Mode Block Diagram

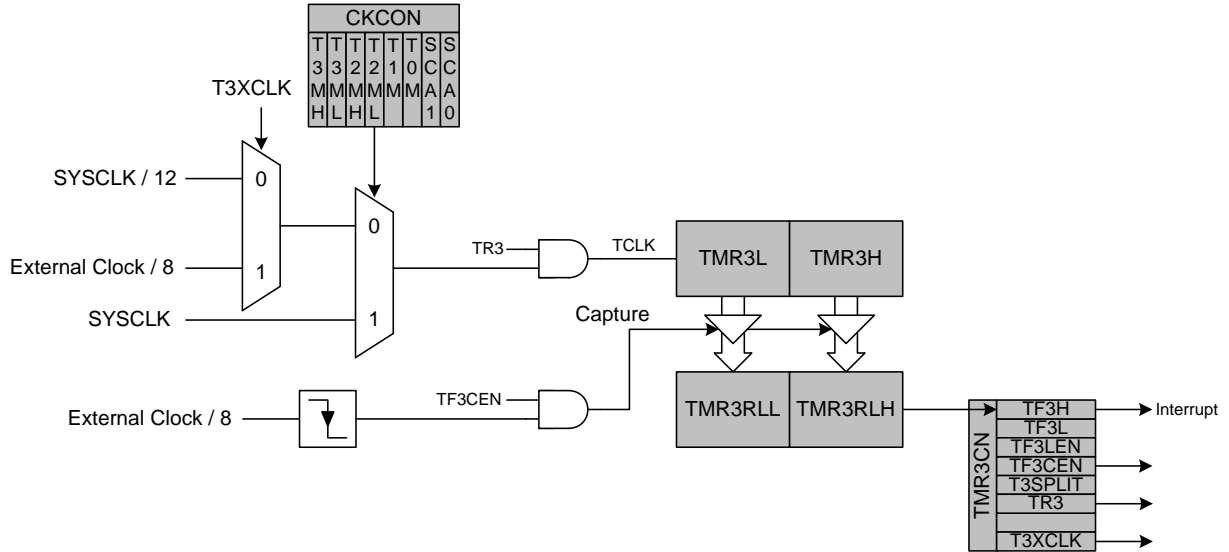


Figure 25.9. Timer 3 External Oscillator Capture Mode Block Diagram

Table 26.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Modules

Operational Mode Bit Number	PCA0CPMn								PCA0PWM				
	7	6	5	4	3	2	1	0	7	6	5	4–2	1–0
Capture triggered by positive edge on CEXn	X	X	1	0	0	0	0	A	0	X	B	XXX	XX
Capture triggered by negative edge on CEXn	X	X	0	1	0	0	0	A	0	X	B	XXX	XX
Capture triggered by any transition on CEXn	X	X	1	1	0	0	0	A	0	X	B	XXX	XX
Software Timer	X	C	0	0	1	0	0	A	0	X	B	XXX	XX
High Speed Output	X	C	0	0	1	1	0	A	0	X	B	XXX	XX
Frequency Output	X	C	0	0	0	1	1	A	0	X	B	XXX	XX
8-Bit Pulse Width Modulator (7)	0	C	0	0	E	0	1	A	0	X	B	XXX	00
9-Bit Pulse Width Modulator (7)	0	C	0	0	E	0	1	A	D	X	B	XXX	01
10-Bit Pulse Width Modulator (7)	0	C	0	0	E	0	1	A	D	X	B	XXX	10
11-Bit Pulse Width Modulator (7)	0	C	0	0	E	0	1	A	D	X	B	XXX	11
16-Bit Pulse Width Modulator	1	C	0	0	E	0	1	A	0	X	B	XXX	XX
Notes: <ol style="list-style-type: none"> 1. X = Don't Care (no functional difference for individual module if 1 or 0). 2. A = Enable interrupts for this module (PCA interrupt triggered on CCFn set to 1). 3. B = Enable 8th, 9th, 10th or 11th bit overflow interrupt (Depends on setting of CLSEL[1:0]). 4. C = When set to 0, the digital comparator is off. For high speed and frequency output modes, the associated pin will not toggle. In any of the PWM modes, this generates a 0% duty cycle (output = 0). 5. D = Selects whether the Capture/Compare register (0) or the Auto-Reload register (1) for the associated channel is accessed via addresses PCA0CPHn and PCA0CPLn. 6. E = When set, a match event will cause the CCFn flag for the associated channel to be set. 7. All modules set to 8, 9, 10 or 11-bit PWM mode use the same cycle length setting. 													

26.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

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SFR Definition 26.5. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF9; SFR Page = 0x00

Bit	Name	Function
7:0	PCA0[7:0]	PCA Counter/Timer Low Byte. The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.
Note: When the WDTE bit is set to 1, the PCA0L register cannot be modified by software. To change the contents of the PCA0L register, the Watchdog Timer must first be disabled.		

SFR Definition 26.6. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFA; SFR Page = 0x00

Bit	Name	Function
7:0	PCA0[15:8]	PCA Counter/Timer High Byte. The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a “snapshot” register, whose contents are updated only when the contents of PCA0L are read (see Section 26.1).
Note: When the WDTE bit is set to 1, the PCA0H register cannot be modified by software. To change the contents of the PCA0H register, the Watchdog Timer must first be disabled.		

C2 Register Definition 27.4. FPCTL: C2 Flash Programming Control

Bit	7	6	5	4	3	2	1	0
Name	FPCTL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0x02

Bit	Name	Function
7:0	FPCTL[7:0]	Flash Programming Control Register. This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 27.5. FPDAT: C2 Flash Programming Data

Bit	7	6	5	4	3	2	1	0
Name	FPDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xB4

Bit	Name	Function	
7:0	FPDAT[7:0]	C2 Flash Programming Data Register.	
		This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.	
		Code	Command
		0x06	Flash Block Read
		0x07	Flash Block Write
		0x08	Flash Page Erase
		0x03	Device Erase

Revision 1.1 to Revision 1.2

- Updated the note in “Power-Fail Reset/VDD Monitor” on page 140 to use a larger font.
- Added the note regarding the voltage regulator and VDD monitor in the high setting from “Power-Fail Reset/VDD Monitor” on page 140 to “Voltage Regulator (REG0)” on page 79 and “V_{DD} Maintenance and the V_{DD} monitor” on page 129.
- Updated the steps in “V_{DD} Maintenance and the V_{DD} monitor” on page 129 to mention using the VDD monitor in the high setting during flash write/erase operations.
- Updated the SUSPEND bit description in OSCICN (SFR Definition 18.2) to mention that firmware must set the ZTCEN bit in REF0CN (SFR Definition 7.1) before entering suspend.
- Added a note to the IFRDY flag in the OSCICN register (SFR Definition 18.2) that the flag may not accurately reflect the state of the oscillator.
- Added VREGIN Ramp Time for Power On spec to Table 5.4, “Reset Electrical Characteristics,” on page 41.
- Updated “V_{DD} Maintenance and the V_{DD} monitor” on page 129 to refer to V_{REGIN} ramp time instead of V_{DD} ramp time.
- Added a note regarding programming at cold temperatures on –I devices to “Programming The Flash Memory” on page 124 and added Temperature during Programming Operations specification to Table 5.5, “Flash Electrical Characteristics,” on page 41.
- Added a note regarding P0.0/VREF when VDD is used as the reference to Table 19.1, “Port I/O Assignment for Analog Functions,” on page 171 and to the description of the REFSL bit in REF0CN (SFR Definition 7.1).
- Added a note regarding a potential unknown state on GPIO during power up if VIO ramps significantly before VDD to “Port Input/Output” on page 169 and “Reset Sources” on page 138.
- Added steps to set the FLEWT bit in the FLSCCL register (SFR Definition 14.3) in the flash write/erase procedures in “Flash Erase Procedure” on page 125, “Flash Write Procedure” on page 125, and “Flash Write Optimization” on page 126.
- Added a note regarding fast changes on VDD causing the V_{DD} Monitor to trigger to “Power-Fail Reset/VDD Monitor” on page 140.
- Added notes regarding UART TX and RX behavior in “Data Transmission” on page 238, “Data Reception” on page 238, and the THRE0 description in the SCON0 register (SFR Definition 23.1).
- Added a note regarding an issue with /RST low time on some older devices to “16.1. Power-On Reset” .