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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f553-imr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Figure 4.2. QFN-40 Landing Diagram

Table 4.2. QFN-40 Landing Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Мах
C1	5.80	5.90	X2	4.10	4.20
C2	5.80	5.90	Y1	0.75	0.85
е	0.50 BSC		Y2	4.10	4.20
X1	0.15	0.25			

Notes:

General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimension and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 3. This Land Pattern Design is based on the IPC-SM-7351 guidelines.
- **4.** All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be $60 \ \mu m$ minimum, all the way around the pad.

Stencil Design

- 6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 7. The stencil thickness should be 0.125 mm (5 mils).
- 8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
- 9. A 4x4 array of 0.80 mm square openings on a 1.05 mm pitch should be used for the center ground pad.

Card Assembly

- **10.** A No-Clean, Type-3 solder paste is recommended.
- **11.** Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



Table 5.7. Clock Multiplier Electrical Specifications

 V_{DD} = 1.8 to 2.75 V, -40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Тур	Max	Units
Input Frequency (Fcm _{in})		2	—	—	MHz
Output Frequency				50	MHz
Power Supply Current		_	0.9	1.9	mA

Table 5.8. Voltage Regulator Electrical Characteristics

 V_{DD} = 1.8 to 2.75 V, -40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Тур	Max	Units	
Input Voltage Range (V _{REGIN})		1.8*	_	5.25	V	
Dropout Voltage (V _{DO})	Maximum Current = 50 mA	—	10	_	mV/mA	
Output Voltage (Vpp)	2.1 V operation (REG0MD = 0)	2.0	2.1	2.25	V	
	2.6 V operation (REG0MD = 1)	2.5	2.6	2.75	v	
Bias Current		—	1	9	μA	
Dropout Indicator Detection Threshold	With respect to VDD	-0.21	_	-0.02	V	
Output Voltage Temperature Coefficient		_	0.29	_	mV/°C	
VREG Settling Time	50 mA load with $V_{REGIN} = 2.4 V$ and V_{DD} load capacitor of 4.8 μ F		450	_	μs	
*Note: The minimum input voltage is 1.8 V or V _{DD} + V _{DO} (max load), whichever is greater						



6.2. Output Code Formatting

The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code. When the repeat count is set to 1, conversion codes are represented in 12-bit unsigned integer format and the output conversion code is updated after each conversion. Inputs are measured from 0 to $V_{REF} \times 4095/4096$. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.2). Unused bits in the ADC0H and ADC0L registers are set to 0. Example codes are shown below for both right-justified and left-justified data.

Input Voltage	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
VREF x 4095/4096	0x0FFF	0xFFF0
VREF x 2048/4096	0x0800	0x8000
VREF x 2047/4096	0x07FF	0x7FF0
0	0x0000	0x0000

When the ADC0 Repeat Count is greater than 1, the output conversion code represents the accumulated result of the conversions performed and is updated after the last conversion in the series is finished. Sets of 4, 8, or 16 consecutive samples can be accumulated and represented in unsigned integer format. The repeat count can be selected using the AD0RPT bits in the ADC0CF register. The value must be right-justified (AD0LJST = 0), and unused bits in the ADC0H and ADC0L registers are set to 0. The following example shows right-justified codes for repeat counts greater than 1. Notice that accumulating 2^n samples is equivalent to left-shifting by *n* bit positions when all samples returned from the ADC have the same value.

Input Voltage	Repeat Count = 4	Repeat Count = 8	Repeat Count = 16
V _{REF} x 4095/4096	0x3FFC	0x7FF8	0xFFF0
V _{REF} x 2048/4096	0x2000	0x4000	0x8000
V _{REF} x 2047/4096	0x1FFC	0x3FF8	0x7FF0
0	0x0000	0x0000	0x0000

6.2.1. Settling Time Requirements

A minimum tracking time is required before an accurate conversion is performed. This tracking time is determined by any series impedance, including the AMUX0 resistance, the ADC0 sampling capacitance, and the accuracy required for the conversion.

Figure 6.5 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 6.1. When measuring the Temperature Sensor output, use the settling time specified in Table 5.10. When measuring V_{DD} with respect to GND, R_{TOTAL} reduces to R_{MUX} . See Table 5.9 for ADC0 minimum settling time requirements as well as the mux impedance and sampling capacitor values.

$$t = ln\left(\frac{2^{n}}{SA}\right) \times R_{TOTAL}C_{SAMPLE}$$

Equation 6.1. ADC0 Settling Time Requirements

Where:

SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB). *t* is the required settling time in seconds. R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance. *n* is the ADC resolution in bits (10).



SFR Definition 7.1. REF0CN: Reference Control

Bit	7	6	5	4	3	2	1	0
Name			ZTCEN	REFLV	REFSL	TEMPE	BIASE	REFBE
Туре	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD1; SFR Page = 0x00

Bit	Name	Function
7:6	Unused	Read = 00b; Write = don't care.
5	ZTCEN	Zero Temperature Coefficient Bias Enable Bit.
		This bit must be set to 1b before entering oscillator suspend mode.
		0: Zero I C Bias Generator automatically enabled when required.
4	DEELV	Voltage Peterance Output Level Select
4	NEFLV	This bit selects the output voltage level for the internal voltage reference
		0: Internal voltage reference set to 1.5 V.
		1: Internal voltage reference set to 2.20 V.
3	REFSL	Voltage Reference Select.
		This bit selects the ADCs voltage reference.
		0: V _{REF} pin used as voltage reference.
		ADC is enabled in the ADC0CN register, the P0.0/VREF pin cannot operate as a gen-
		eral purpose I/O pin in open-drain mode. With the above settings, this pin can operate in push-pull output mode or as an analog input.
2	TEMPE	Temperature Sensor Enable Bit.
		0: Internal Temperature Sensor off.
		1: Internal Temperature Sensor on.
1	BIASE	Internal Analog Bias Generator Enable Bit.
		0: Internal Bias Generator off.
		1: Internal Bias Generator on.
0	REFBE	On-chip Reference Buffer Enable Bit.
		U: Un-chip Reference Buffer off.
		The only relation be build on internal voltage reference driven of the VREF pin.



Table 10.1. CIP-51 Instruction Set Summary

Mnemonic	Description	Bytes	Clock Cycles
Arithmetic Operations	1	I	-1
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add indirect RAM to A	1	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add indirect RAM to A with carry	1	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	1	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment indirect RAM	1	2
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement indirect RAM	1	2
INC DPTR	Increment Data Pointer	1	1
MUL AB	Multiply A and B	1	4
DIV AB	Divide A by B	1	8
DA A	Decimal adjust A	1	1
Logical Operations			
ANL A, Rn	AND Register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND indirect RAM to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	2
ANL direct, #data	AND immediate to direct byte	3	3
ORL A, Rn	OR Register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR indirect RAM to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate to direct byte	3	3
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2
Note: Certain instructions take the FLRT setting (SFR	e a variable number of clock cycles to execute depending Definition 14.3).	on instruction a	alignment and



On exit from the PCA interrupt service routine, the CIP-51 will return to the CAN0 ISR. On execution of the RETI instruction, SFR Page 0x00 used to access the PCA registers will be automatically popped off of the SFR Page Stack, and the contents of the SFRNEXT register will be moved to the SFRPAGE register. Software in the CAN0 ISR can continue to access SFRs as it did prior to the PCA interrupt. Likewise, the contents of SFRLAST are moved to the SFRNEXT register. Recall this was the SFR Page value 0x00 being used to access SPI0DAT before the CAN0 interrupt occurred. See Figure 12.5.



Figure 12.5. SFR Page Stack Upon Return From PCA Interrupt



On the execution of the RETI instruction in the CAN0 ISR, the value in SFRPAGE register is overwritten with the contents of SFRNEXT. The CIP-51 may now access the SPI0DAT register as it did prior to the interrupts occurring. See Figure 12.6.



Figure 12.6. SFR Page Stack Upon Return From CAN0 Interrupt

In the example above, all three bytes in the SFR Page Stack are accessible via the SFRPAGE, SFRNEXT, and SFRLAST special function registers. If the stack is altered while servicing an interrupt, it is possible to return to a different SFR Page upon interrupt exit than selected prior to the interrupt call. Direct access to the SFR Page stack can be useful to enable real-time operating systems to control and manage context switching between multiple tasks.

Push operations on the SFR Page Stack only occur on interrupt service, and pop operations only occur on interrupt exit (execution on the RETI instruction). The automatic switching of the SFRPAGE and operation of the SFR Page Stack as described above can be disabled in software by clearing the SFR Automatic Page Enable Bit (SFRPGEN) in the SFR Page Control Register (SFR0CN). See SFR Definition 12.1.



SFR Definition 12.2. SFRPAGE: SFR Page

Bit	7	6	5	4	3	2	1	0
Name		SFRPAGE[7:0]						
Туре		R/W						
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA7; SFR Page = All Pages

Bit	Name	Function
7:0	SFRPAGE[7:0]	SFR Page Bits.
		Represents the SFR Page the C8051 core uses when reading or modifying SFRs.
		Write: Sets the SFR Page.
		Read: Byte is the SFR page the C8051 core is using.
		When enabled in the SFR Page Control Register (SFR0CN), the C8051 core will automatically switch to the SFR Page that contains the SFRs of the corresponding peripheral/function that caused the interrupt, and return to the previous SFR page upon return from interrupt (unless SFR Stack was altered before a returning from the interrupt). SFRPAGE is the top byte of the SFR Page Stack, and push/pop events of this stack are caused by interrupts (and not by reading/writing to the SFRPAGE register)



	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
F8			CAN0IF2DA2L	CAN0IF2DA2H	CAN0IF2DB1L	CAN0IF2DB1H	CAN0IF2DB2L	CAN0IF2DB2H
_ 1	_							
F0	B (All Dogoo)		CAN0IF2A2L	CAN0IF2A2H			CAN0IF2DA1L	CAN0IF2DA1H
F8	(All Fages)		CANOIE2M11	CANOIE2M1H		CANOIE2M2H		
LU								
E0	ACC		CAN0IF2CML	CAN0IF2CMH		-	EIE1	EIE2
	(All Pages)						(All Pages)	(All Pages)
D8		_	CAN0IF1DB1L	CAN0IF1DB1H	CAN0IF1DB2L	CAN0IF1DB2H	CAN0IF2CRL	CAN0IF2CRH
D 0								
DU	PSW (All Pages)		CANUFTWICL	CANUFINCH	CANUFIDATE	CANUFIDATH	CANULTIDAZE	CANUFIDAZH
C8	(, , agee)		CAN0IF1A1L	CAN0IF1A1H	CAN0IF1A2L	CAN0IF1A2H	CAN0IF2MCL	CAN0IF2MCH
C0	CAN0CN		CAN0IF1CML	CAN0IF1CMH	CAN0IF1M1L	CAN0IF1M1H	CAN0IF1M2L	CAN0IF1M2H
1								
B8	IP		CAN0MV1L	CAN0MV1H	CAN0MV2L	CAN0MV2H	CAN0IF1CRL	CAN0IF1CRH
BU						D/		
БО	(All Pages)		CANOFZE	CANOFZIT		(All Pages)	(All Pages)	(All Pages)
A8	IE		CAN0ND1L	CAN0ND1H	CAN0ND2L	CAN0ND2H	CAN0IP1L	CAN0IP1H
	(All Pages)							
A0	P2	CAN0BRPE	CAN0TR1L	CAN0TR1H	CAN0TR2L	CAN0TR2H		SFRPAGE
	(All Pages)							(All Pages)
98	SCON0		CANOBIL	CANOBIH	CANOIIDL	CANOIIDH	CANOISI	
90	(All Lages) P1		CANOCEG		CANOSTAT		CANOERRI	CANOERRH
00	(All Pages)		0/110010		0/1100 //1		O, INDERINE	O/ NOERIAN
88	TCON	TMOD	TLO	TL1	TH0	TH1	CKCON	
	(All Pages)	(All Pages)	(All Pages)	(All Pages)	(All Pages)	(All Pages)	(All Pages)	
80	P0	SP	DPL	DPH		SFRNEXT	SFRLAST	PCON
	(All Pages)	(All Pages)	(All Pages)	(All Pages)		(All Pages)	(All Pages)	(All Pages)
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
	(bit addres	sable)						

Table 12.2. Special Function Register (SFR) Memory Map for Page 0x0C



Table 12.3. Special Function Registers (Continued)

Register	Address	Description	Page
SMB0CF	0xC1	SMBus0 Configuration	224
SMB0CN	0xC0	SMBus0 Control	226
SMB0DAT	0xC2	SMBus0 Data	228
SMOD0	0xA9	UART0 Mode	243
SN0	0xF9	Serial Number 0	91
SN1	0xFA	Serial Number 1	91
SN2	0xFB	Serial Number 2	91
SN3	0xFC	Serial Number 3	91
SP	0x81	Stack Pointer	89
SPI0CFG	0xA1	SPI0 Configuration	253
SPIOCKR	0xA2	SPI0 Clock Rate Control	255
SPI0CN	0xF8	SPI0 Control	254
SPI0DAT	0xA3	SPI0 Data	255
TCON	0x88	Timer/Counter Control	265
TH0	0x8C	Timer/Counter 0 High	268
TH1	0x8D	Timer/Counter 1 High	268
TL0	0x8A	Timer/Counter 0 Low	267
TL1	0x8B	Timer/Counter 1 Low	267
TMOD	0x89	Timer/Counter Mode	266
TMR2CN	0xC8	Timer/Counter 2 Control	272
TMR2H	0xCD	Timer/Counter 2 High	274
TMR2L	0xCC	Timer/Counter 2 Low	274
TMR2RLH	0xCB	Timer/Counter 2 Reload High	273
TMR2RLL	0xCA	Timer/Counter 2 Reload Low	273
TMR3CN	0x91	Timer/Counter 3 Control	278
TMR3H	0x95	Timer/Counter 3 High	280
TMR3L	0x94	Timer/Counter 3 Low	280
TMR3RLH	0x93	Timer/Counter 3 Reload High	279
TMR3RLL	0x92	Timer/Counter 3 Reload Low	279
VDM0CN	0xFF	V _{DD} Monitor Control	141
XBR0	0xE1	Port I/O Crossbar Control 0	176
XBR1	0xE2	Port I/O Crossbar Control 1	177
XBR2	0xC7	Port I/O Crossbar Control 2	178



18.4.1. External Crystal Example

If a crystal or ceramic resonator is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 18.1, Option 1. The External Oscillator Frequency Control value (XFCN) should be chosen from the Crystal column of the table in SFR Definition 18.6 (OSCXCN register). For example, an 11.0592 MHz crystal requires an XFCN setting of 111b and a 32.768 kHz Watch Crystal requires an XFCN setting of 001b. After an external 32.768 kHz oscillator is stabilized, the XFCN setting can be switched to 000 to save power. It is recommended to enable the missing clock detector before switching the system clock to any external oscillator source.

When the crystal oscillator is first enabled, the oscillator amplitude detection circuit requires a settling time to achieve proper bias. Introducing a delay of 1 ms between enabling the oscillator and checking the XTLVLD bit will prevent a premature switch to the external oscillator as the system clock. Switching to the external oscillator before the crystal oscillator has stabilized can result in unpredictable behavior. The recommended procedure is:

- 1. Force XTAL1 and XTAL2 to a high state. This involves enabling the Crossbar and writing 1 to the port pins associated with XTAL1 and XTAL2.
- 2. Configure XTAL1 and XTAL2 as analog inputs using.
- 3. Enable the external oscillator.
- 4. Wait at least 1 ms.
- 5. Poll for XTLVLD => 1.
- 6. Enable the Missing Clock Detector.
- 7. Switch the system clock to the external oscillator.

Important Note on External Crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The desired load capacitance depends upon the crystal and the manufacturer. Refer to the crystal data sheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 18.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 18.3.



SFR Definition 19.13. P0MDIN: Port 0 Input Mode

Bit	7	6	5	4	3	2	1	0				
Name	POMDIN[7:0]											
Туре	R/W											
Reset	1	1	1	1	1	1	1	1				

SFR Address = 0xF1; SFR Page = 0x0F

Bit	Name	Function
7:0	P0MDIN[7:0]	Analog Configuration Bits for P0.7–P0.0 (respectively).
		 Port pins configured for analog mode have their weak pull-up and digital receiver disabled. For analog mode, the pin also needs to be configured for open-drain mode in the P0MDOUT register. 0: Corresponding P0.n pin is configured for analog mode. 1: Corresponding P0.n pin is not configured for analog mode.

SFR Definition 19.14. P0MDOUT: Port 0 Output Mode

Bit	7	6	5	4	3	2	1	0				
Name	P0MDOUT[7:0]											
Туре	R/W											
Reset	0	0	0	0	0	0	0	0				

SFR Address = 0xA4; SFR Page = 0x0F

Bit	Name	Function
7:0	P0MDOUT[7:0]	Output Configuration Bits for P0.7–P0.0 (respectively).
		These bits are ignored if the corresponding bit in register P0MDIN is logic 0. 0: Corresponding P0.n Output is open-drain. 1: Corresponding P0.n Output is push-pull.



The CAN controller clock must be less than or equal to 25 MHz. If the CIP-51 system clock is above 25 MHz, the divider in the CAN0CFG register must be set to divide the CAN controller clock down to an appropriate speed.

21.1.2. CAN Register Access

The CAN controller clock divider selected in the CAN0CFG SFR affects how the CAN registers can be accessed. If the divider is set to 1, then a CAN SFR can immediately be read after it is written. If the divider is set to a value other than 1, then a read of a CAN SFR that has just been written must be delayed by a certain number of cycles. This delay can be performed using a NOP or some other instruction that does not attempt to read the register. This access limitation applies to read and read-modify-write instructions that occur immediately after a write. The full list of affected instructions is ANL, ORL, MOV, XCH, and XRL.

For example, with the CAN0CFG divider set to 1, the CAN0CN SFR can be accessed as follows:

MOV CANOCN, #041	;	Enable access to	Bit	Timing	Register
MOV R7, CANOCN	;	Copy CANOCN to R	.7		

With the CAN0CFG divider set to /2, the same example code requires an additional NOP:

MOV	CAN0CN, #041	;	Enabl	e acces	ss to	Bit	Timing	Regis	ter
NOP		;	Wait	for wri	lte to	o com	plete		
MOV	R7, CANOCN	;	Сору	CANOCN	to R'	7			

The number of delay cycles required is dependent on the divider setting. With a divider of 2, the read must wait for 1 system clock cycle. With a divider of 4, the read must wait 3 system clock cycles, and with the divider set to 8, the read must wait 7 system clock cycles. The delay only needs to be applied when reading the same register that was written. The application can write and read other CAN SFRs without any delay.

21.1.3. Example Timing Calculation for 1 Mbit/Sec Communication

This example shows how to configure the CAN controller timing parameters for a 1 Mbit/Sec bit rate. Table 21.1 shows timing-related system parameters needed for the calculation.

Parameter	Value	Description
CIP-51 system clock (SYSCLK)	24 MHz	Internal Oscillator Max
CAN controller clock (fsys)	24 MHz	CAN0CFG divider set to 1
CAN clock period (tsys)	41.667 ns	Derived from 1/fsys
CAN time quantum (tq)	41.667 ns	Derived from tsys x BRP ^{1,2}
CAN bus length	10 m	5 ns/m signal delay between CAN nodes
Propogation delay time ³	400 ns	2 x (transceiver loop delay + bus line delay)

Table 21.1. Background System Information

Notes:

1. The CAN time quantum is the smallest unit of time recognized by the CAN controller. Bit timing parameters are specified in integer multiples of the time quantum.

- 2. The Baud Rate Prescaler (BRP) is defined as the value of the BRP Extension Register plus 1. The BRP extension register has a reset value of 0x0000. The BRP has a reset value of 1.
- **3.** Based on an ISO-11898 compliant transceiver. CAN does not specify a physical layer.

Each bit transmitted on a CAN network has 4 segments (Sync_Seg, Prop_Seg, Phase_Seg1, and Phase_Seg2), as shown in Figure 18.3. The sum of these segments determines the CAN bit time (1/bit rate). In this example, the desired bit rate is 1 Mbit/sec; therefore, the desired bit time is 1000 ns.



All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data a byte at a time waiting for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 22.3 illustrates a typical SMBus transaction.



Figure 22.3. SMBus Transaction

22.3.1. Transmitter Vs. Receiver

On the SMBus communications interface, a device is the "transmitter" when it is sending an address or data byte to another device on the bus. A device is a "receiver" when an address or data byte is being sent to it from another device on the bus. The transmitter controls the SDA line during the address or data byte. After each byte of address or data information is sent by the transmitter, the receiver sends an ACK or NACK bit during the ACK phase of the transfer, during which time the receiver controls the SDA line.

22.3.2. Arbitration

A master may start a transfer only if the bus is free. The bus is free after a STOP condition or after the SCL and SDA lines remain high for a specified time (see Section "22.3.5. SCL High (SMBus Free) Timeout" on page 221). In the event that two or more devices attempt to begin a transfer at the same time, an arbitration scheme is employed to force one master to give up the bus. The master devices continue transmitting until one attempts a HIGH while the other transmits a LOW. Since the bus is open-drain, the bus will be pulled LOW. The master attempting the HIGH will detect a LOW SDA and lose the arbitration. The winning master continues its transmission without interruption; the losing master becomes a slave and receives the rest of the transfer if addressed. This arbitration scheme is non-destructive: one device always wins, and no data is lost.

22.3.3. Clock Low Extension

SMBus provides a clock synchronization mechanism, similar to I²C, which allows devices with different speed capabilities to coexist on the bus. A clock-low extension is used during a transfer in order to allow slower slave devices to communicate with faster masters. The slave may temporarily hold the SCL line LOW to extend the clock low period, effectively decreasing the serial clock frequency.

22.3.4. SCL Low Timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a "timeout" condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.

When the SMBTOE bit in SMB0CF is set, Timer 3 is used to detect SCL low timeouts. Timer 3 is forced to reload when SCL is high, and allowed to count when SCL is low. With Timer 3 enabled and configured to



22.4.2. SMB0CN Control Register

SMB0CN is used to control the interface and to provide status information (see SFR Definition 22.2). The higher four bits of SMB0CN (MASTER, TXMODE, STA, and STO) form a status vector that can be used to jump to service routines. MASTER indicates whether a device is the master or slave during the current transfer. TXMODE indicates whether the device is transmitting or receiving data for the current byte.

STA and STO indicate that a START and/or STOP has been detected or generated since the last SMBus interrupt. STA and STO are also used to generate START and STOP conditions when operating as a master. Writing a 1 to STA will cause the SMBus interface to enter Master Mode and generate a START when the bus becomes free (STA is not cleared by hardware after the START is generated). Writing a 1 to STO while in Master Mode will cause the interface to generate a STOP and end the current transfer after the next ACK cycle. If STO and STA are both set (while in Master Mode), a STOP followed by a START will be generated.

As a receiver, writing the ACK bit defines the outgoing ACK value; as a transmitter, reading the ACK bit indicates the value received during the last ACK cycle. ACKRQ is set each time a byte is received, indicating that an outgoing ACK value is needed. When ACKRQ is set, software should write the desired outgoing value to the ACK bit before clearing SI. A NACK will be generated if software does not write the ACK bit before clearing SI. SDA will reflect the defined ACK value immediately following a write to the ACK bit; however SCL will remain low until SI is cleared. If a received slave address is not acknowledged, further slave events will be ignored until the next START is detected.

The ARBLOST bit indicates that the interface has lost an arbitration. This may occur anytime the interface is transmitting (master or slave). A lost arbitration while operating as a slave indicates a bus error condition. ARBLOST is cleared by hardware each time SI is cleared.

The SI bit (SMBus Interrupt Flag) is set at the beginning and end of each transfer, after each byte frame, or when an arbitration is lost; see Table 22.3 for more details.

Important Note About the SI Bit: The SMBus interface is stalled while SI is set; thus SCL is held low, and the bus is stalled until software clears SI.



SFR	Definition	23.1.	SCON0:	Serial	Port 0	Control
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Bit	7	6	5	4	3	2	1	0
Name	OVR0	PERR0	THRE0	REN0	TBX0	RBX0	TI0	RI0
Туре	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

SFR Definition 25.2. TCON: Timer Control

Bit	Bit 7 6 5 4 3 2 1							0	
Nam	e TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
Туре	R/W	R/W R/W R/W R/W R/W							
Rese	t 0	0	0	0	0	0	0	0	
SFR A	ddress = 0x8	0x88; Bit-Addressable; SFR Page = All Pages							
Bit	Name		Function						
7	TF1	Timer 1 Overflow Flag. Set to 1 by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.							
6	TR1	Timer 1 Ru Timer 1 is e	Timer 1 Run Control. Timer 1 is enabled by setting this bit to 1.						
5	TF0	Timer 0 Ov	erflow Flag	•					
		Set to 1 by l but is autom routine.	Set to 1 by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.						
4	TR0	Timer 0 Run Control.							
		Timer 0 is enabled by setting this bit to 1.							
3	IE1	External In	terrupt 1.						
		This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode.							
2	IT1	Interrupt 1 Type Select.							
		This bit selects whether the configured INT1 interrupt will be edge or level sensitive. INT1 is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 13.7). 0: INT1 is level triggered. 1: INT1 is edge triggered.							
1	IE0	External Interrupt 0.							
		This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode.							
0	IT0	Interrupt 0 Type Select.							
		This bit selects whether the configured INT0 interrupt will be edge or level sensitive. INT0 is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 13.7). 0: INT0 is level triggered. 1: INT0 is edge triggered.							



SFR Definition 25.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0		
Nam	e	TH0[7:0]								
Туре	9	R/W								
Rese	et 0	0	0	0	0	0	0	0		
SFR Address = 0x8C; SFR Page = All Pages										
Bit	Name	Function								
7:0	TH0[7:0]	Timer 0 Hig	jh Byte.							

	The TH0	register	is the	high	byte	of the	16-bit	Timer	0.
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SFR Definition 25.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Nam	> TH1[7:0]							
Туре	R/W							
Rese	et 0	0	0	0	0	0	0	0
SFR Address = 0x8D; SFR Page = All Pages								
Bit	Name	Function						
7:0	TH1[7:0]	[7:0] Timer 1 High Byte.						
		The TH1 register is the high byte of the 16-bit Timer 1.						





Figure 26.8. PCA 8-Bit PWM Mode Diagram

26.3.5.2. 9/10/11-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 9/10/11-bit PWM mode should be varied by writing to an "Auto-Reload" Register, which is dual-mapped into the PCA0CPHn and PCA0CPLn register locations. The data written to define the duty cycle should be right-justified in the registers. The auto-reload registers are accessed (read or written) when the bit ARSEL in PCA0PWM is set to 1. The capture/compare registers are accessed when ARSEL is set to 0.

When the least-significant N bits of the PCA0 counter match the value in the associated module's capture/compare register (PCA0CPn), the output on CEXn is asserted high. When the counter overflows from the Nth bit, CEXn is asserted low (see Figure 26.9). Upon an overflow from the Nth bit, the COVF flag is set, and the value stored in the module's auto-reload register is loaded into the capture/compare register. The value of N is determined by the CLSEL bits in register PCA0PWM.

The 9, 10 or 11-bit PWM mode is selected by setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to the desired cycle length (other than 8-bits). If the MATn bit is set to 1, the CCFn flag for the module will be set each time a comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 512 (9-bit), 1024 (10-bit) or 2048 (11-bit) PCA clock cycles. The duty cycle for 9/10/11-Bit PWM Mode is given in Equation 26.2, where N is the number of bits in the PWM cycle.

Important Note About PCA0CPHn and PCA0CPLn Registers: When writing a 16-bit value to the PCA0CPn registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

Duty Cycle =
$$\frac{(2^{N} - PCA0CPn)}{2^{N}}$$

Equation 26.3. 9, 10, and 11-Bit PWM Duty Cycle

A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

