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Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), CANbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f555-imr

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Gain Register Definition 6.3. ADC0GNA: ADC0 Additional Selectable Gain

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GAINADD
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	1

Indirect Address = 0x08;

Bit	Name	Function
7:1	Reserved	Must Write 0000000b.
0	GAINADD	ADC0 Additional Gain Bit. Setting this bit add 1/64 (0.016) gain to the gain value in the ADC0GNH and ADC0GNL registers.

Note: This register is accessed indirectly; See Section 6.3.2 for details for writing this register.

6.6. Temperature Sensor

An on-chip temperature sensor is included on the C8051F55x/56x/57x devices which can be directly accessed via the ADC multiplexer in single-ended configuration. To use the ADC to measure the temperature sensor, the ADC multiplexer channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 6.9. The output voltage (V_{TEMP}) is the positive ADC input is selected by bits AD0MX[4:0] in register ADC0MX. The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 7.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 5.10 for the slope and offset parameters of the temperature sensor.

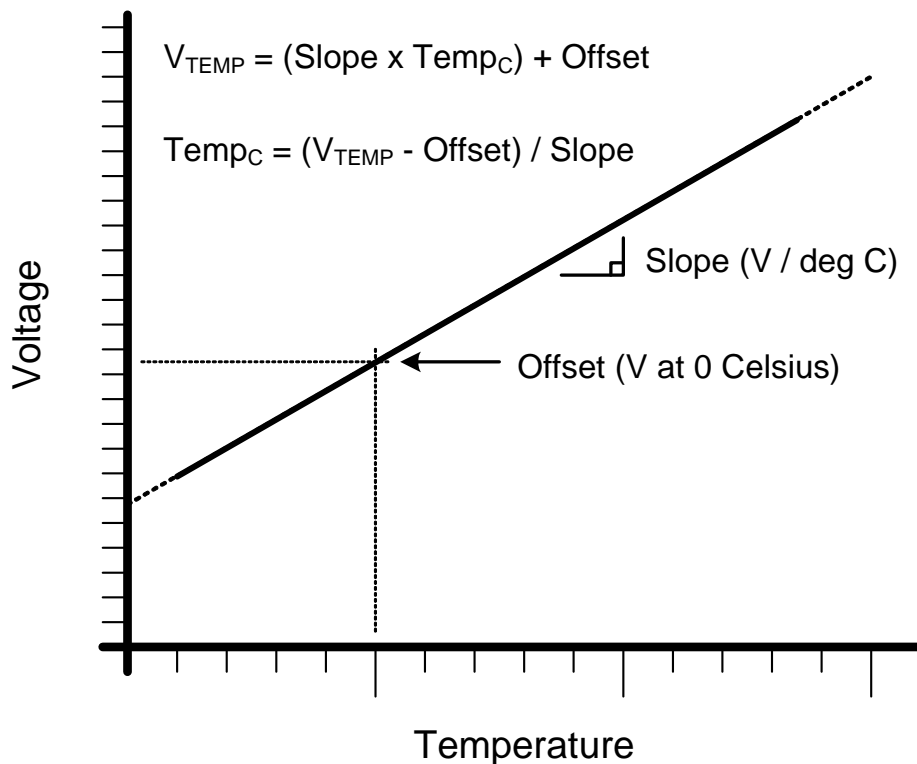


Figure 6.9. Temperature Sensor Transfer Function

8.1. Comparator Multiplexer

C8051F55x/56x/57x devices include an analog input multiplexer for each of the comparators to connect Port I/O pins to the comparator inputs. The Comparator0 inputs are selected in the CPT0MX register (SFR Definition 8.5). The CMX0P3–CMX0P0 bits select the Comparator0 positive input; the CMX0N3–CMX0N0 bits select the Comparator0 negative input. Similarly, the Comparator1 inputs are selected in the CPT1MX register using the CMX1P3–CMX1P0 bits and CMX1N3–CMX1N0 bits. The same pins are available to both multiplexers at the same time and can be used by both comparators simultaneously.

Important Note About Comparator Inputs: The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “19.6. Special Function Registers for Accessing and Configuring Port I/O” on page 183).

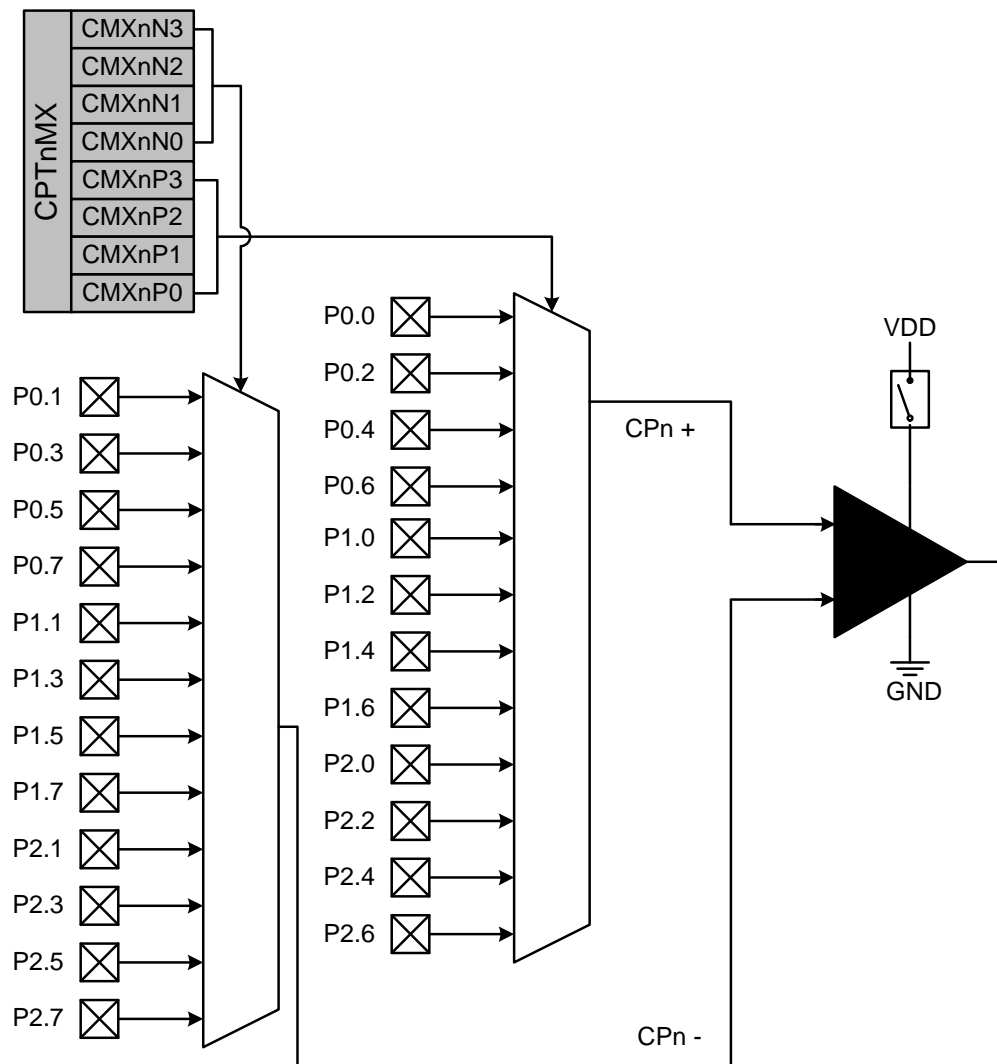


Figure 8.3. Comparator Input Multiplexer Block Diagram

SFR Definition 14.4. CCH0CN: Cache Control

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	CHPFEN	Reserved	Reserved	Reserved	Reserved	CHBLKW
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

SFR Address = 0xE3; SFR Page = 0x0F

Bit	Name	Function
7:6	Reserved	Must Write 00b
5	CHPFEN	Cache Prefect Enable Bit. 0: Prefetch engine is disabled. 1: Prefetch engine is enabled.
4:1	Reserved	Must Write 0000b.
0	CHBLKW	Block Write Enable Bit. This bit allows block writes to Flash memory from firmware. 0: Each byte of a software Flash write is written individually. 1: Flash bytes are written in groups of two.

SFR Definition 14.5. ONSHOT: Flash Oneshot Period

Bit	7	6	5	4	3	2	1	0
Name					PERIOD[3:0]			
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

SFR Address = 0xBE; SFR Page = 0x0F

Bit	Name	Function
7:4	Unused	Read = 0000b. Write = don't care.
3:0	PERIOD[3:0]	Oneshot Period Control Bits. These bits limit the internal Flash read strobe width as follows. When the Flash read strobe is de-asserted, the Flash memory enters a low-power state for the remainder of the system clock cycle. $FLASH_{RDMAX} = 5ns + (PERIOD \times 5ns)$

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When a digital I/O cell is placed in the high impedance state, a weak pull-up transistor pulls the Port pad to the VIO supply voltage to ensure the digital input is at a defined logic state. Weak pull-ups are disabled when the I/O cell is driven to GND to minimize power consumption and may be globally disabled by setting WEAKPUD to 1. The user should ensure that digital I/O are always internally or externally pulled or driven to a valid logic state to minimize power consumption. Port pins configured for digital I/O always read back the logic state of the Port pad, regardless of the output logic value of the Port pin.

19.1.3. Interfacing Port I/O in a Multi-Voltage System

All Port I/O are capable of interfacing to digital logic operating at a supply voltage higher than VDD and less than 5.25 V. Connect the VIO pin to the voltage source of the interface logic.

19.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins P0.0–P3.7 can be assigned to various analog, digital, and external interrupt functions. P4.0 can be assigned to only digital functions. The Port pins assigned to analog functions should be configured for analog I/O, and Port pins assigned to digital or external interrupt functions should be configured for digital I/O.

19.2.1. Assigning Port I/O Pins to Analog Functions

Table 19.1 shows all available analog functions that require Port I/O assignments. **Port pins selected for these analog functions should have their corresponding bit in PnSKIP set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the Crossbar. Table 19.1 shows the potential mapping of Port I/O to each analog function.

Table 19.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P3.7 ¹	ADC0MX, PnSKIP
Comparator0 or Comparator1 Input	P0.0–P2.7 ¹	CPT0MX, CPT1MX, PnSKIP
Voltage Reference (VREF0) ²	P0.0	REF0CN, PnSKIP
External Oscillator in Crystal Mode (XTAL1)	P0.2	OSCXCN, PnSKIP
External Oscillator in RC, C, or Crystal Mode (XTAL2)	P0.3	OSCXCN, PnSKIP
Notes:		
<ol style="list-style-type: none"> P3.1–P3.7 are available on the 40-pin packages. P2.2–P3.0 are available 40-pin and 32-pin packages. If VDD is selected as the voltage reference in the REF0CN register and the ADC is enabled in the ADC0CN register, the P0.0/VREF pin cannot operate as a general purpose I/O pin in open-drain mode. With the above settings, this pin can operate in push-pull output mode or as an analog input. 		

19.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to 1.** Table 19.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

C8051F55x/56x/57x

Port	P0							P1							P2							P3							P4				
															P2.2-P2.7, P3.0 available on 40-pin and 32-pin packages							P3.1-P3.7, P4.0 available on 40-pin packages											
PIN I/O	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
UART_TX																																	
UART_RX																																	
CAN_TX																																	
CAN_RX																																	
SCK																																	
MISO																																	
MOSI																																	
NSS																																	
SDA																																	
SCL																																	
CP0																																	
CP0A																																	
CP1																																	
CP1A																																	
SYSCLK																																	
CEX0																																	
CEX1																																	
CEX2																																	
CEX3																																	
CEX4																																	
CEX5																																	
ECI																																	
T0																																	
T1																																	
LIN_TX																																	
LIN_RX																																	

Figure 19.3. Peripheral Availability on Port I/O Pins

Registers XBR0, XBR1, and XBR2 are used to assign the digital I/O resources to the physical I/O Port pins. Note that when the SMBus is selected, the Crossbar assigns both pins associated with the SMBus (SDA and SCL); and similarly when the UART, CAN or LIN are selected, the Crossbar assigns both pins associated with the peripheral (TX and RX). UART0 pin assignments are fixed for bootloading purposes: UART TX0 is always assigned to P0.4; UART RX0 is always assigned to P0.5. CAN0 pin assignments are fixed to P0.6 for CAN_TX and P0.7 for CAN_RX. Standard Port I/Os appear contiguously after the prioritized functions have been assigned.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, pending the state of the NSS-MD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

As an example configuration, if CAN0, SPI0 in 4-wire mode, and PCA0 Modules 0, 1, and 2 are enabled on the crossbar with P0.1, P0.2, and P0.5 skipped, the registers should be set as follows: XBR0 = 0x06 (CAN0 and SPI0 enabled), XBR1 = 0x0C (PCA0 modules 0, 1, and 2 enabled), XBR2 = 0x40 (Crossbar enabled), and P0SKIP = 0x26 (P0.1, P0.2, and P0.5 skipped). The resulting crossbar would look as shown in Figure 19.4.

SFR Definition 19.15. P0SKIP: Port 0 Skip

Bit	7	6	5	4	3	2	1	0
Name	P0SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD4; SFR Page = 0x0F

Bit	Name	Function
7:0	P0SKIP[7:0]	<p>Port 0 Crossbar Skip Enable Bits.</p> <p>These bits select Port 0 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar.</p> <p>0: Corresponding P0.n pin is not skipped by the Crossbar.</p> <p>1: Corresponding P0.n pin is skipped by the Crossbar.</p>

SFR Definition 19.16. P1: Port 1

Bit	7	6	5	4	3	2	1	0
Name	P1[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0x90; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P1[7:0]	<p>Port 1 Data.</p> <p>Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.</p>	<p>0: Set output latch to logic LOW.</p> <p>1: Set output latch to logic HIGH.</p>	<p>0: P1.n Port pin is logic LOW.</p> <p>1: P1.n Port pin is logic HIGH.</p>

SFR Definition 19.23. P2SKIP: Port 2 Skip

Bit	7	6	5	4	3	2	1	0
Name	P2SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD6; SFR Page = 0x0F

Bit	Name	Function
7:0	P2SKIP[7:0]	<p>Port 2 Crossbar Skip Enable Bits.</p> <p>These bits select Port 2 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar.</p> <p>0: Corresponding P2.n pin is not skipped by the Crossbar.</p> <p>1: Corresponding P2.n pin is skipped by the Crossbar.</p>
<p>Note: P2.2-P2.7 are available on 40-pin and 32-pin packages.</p>		

SFR Definition 19.24. P3: Port 3

Bit	7	6	5	4	3	2	1	0
Name	P3[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xB0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P3[7:0]	<p>Port 3 Data.</p> <p>Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.</p>	<p>0: Set output latch to logic LOW.</p> <p>1: Set output latch to logic HIGH.</p>	<p>0: P3.n Port pin is logic LOW.</p> <p>1: P3.n Port pin is logic HIGH.</p>
<p>Note: P3.0 is available on 40-pin and 32-pin packages. P3.1-P3.7 are available on 40-pin packages</p>				

SFR Definition 19.27. P3SKIP: Port 3Skip

Bit	7	6	5	4	3	2	1	0
Name	P3SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD7; SFR Page = 0x0F

Bit	Name	Function
7:0	P3SKIP[7:0]	<p>Port 3 Crossbar Skip Enable Bits.</p> <p>These bits select Port 3 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar.</p> <p>0: Corresponding P3.n pin is not skipped by the Crossbar.</p> <p>1: Corresponding P3.n pin is skipped by the Crossbar.</p>

Note: P3.0 is available on 40-pin and 32-pin packages. P3.1-P3.7 are available on 40-pin packages

SFR Definition 19.28. P4: Port 4

Bit	7	6	5	4	3	2	1	0
Name	P4[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xB5; SFR Page = All Pages

Bit	Name	Description	Write	Read
7:0	P4[7:0]	<p>Port 4 Data.</p> <p>Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.</p>	<p>0: Set output latch to logic LOW.</p> <p>1: Set output latch to logic HIGH.</p>	<p>0: P4.n Port pin is logic LOW.</p> <p>1: P4.n Port pin is logic HIGH.</p>

Note: Port 4.0 is available on 40-pin packages.

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SFR Definition 21.1. CAN0CFG: CAN Clock Configuration

Bit	7	6	5	4	3	2	1	0
Name	Unused	Unused	Unused	Unused	Unused	Unused	SYSDIV[1:0]	
Type	R	R	R	R	R	R	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x92; SFR Page = 0x0C

Bit	Name	Function
7:2	Unused	Read = 000000b; Write = Don't Care.
1:0	SYSDIV[1:0]	CAN System Clock Divider Bits. The CAN controller clock is derived from the CIP-51 system clock. The CAN controller clock must be less than or equal to 25 MHz. 00: CAN controller clock = System Clock/1. 01: CAN controller clock = System Clock/2. 10: CAN controller clock = System Clock/4. 11: CAN controller clock = System Clock/8.

SFR Definition 22.2. SMB0CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER	TXMODE	STA	STO	ACKRQ	ARBLOST	ACK	SI
Type	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC0; Bit-Addressable; SFR Page =0x00

Bit	Name	Description	Read	Write
7	MASTER	SMBus Master/Slave Indicator. This read-only bit indicates when the SMBus is operating as a master.	0: SMBus operating in slave mode. 1: SMBus operating in master mode.	N/A
6	TXMODE	SMBus Transmit Mode Indicator. This read-only bit indicates when the SMBus is operating as a transmitter.	0: SMBus in Receiver Mode. 1: SMBus in Transmitter Mode.	N/A
5	STA	SMBus Start Flag.	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO	SMBus Stop Flag.	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmitted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ	SMBus Acknowledge Request.	0: No Ack requested 1: ACK requested	N/A
2	ARBLOST	SMBus Arbitration Lost Indicator.	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK	SMBus Acknowledge.	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SI	SMBus Interrupt Flag. This bit is set by hardware under the conditions listed in Table 15.3. SI must be cleared by software. While SI is set, SCL is held low and the SMBus is stalled.	0: No interrupt pending 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event. 1: Force interrupt.

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23.3. Configuration and Operation

UART0 provides standard asynchronous, full duplex communication. It can operate in a point-to-point serial communications application, or as a node on a multi-processor serial interface. To operate in a point-to-point application, where there are only two devices on the serial bus, the MCE0 bit in SMOD0 should be cleared to 0. For operation as part of a multi-processor communications bus, the MCE0 and XBE0 bits should both be set to 1. In both types of applications, data is transmitted from the microcontroller on the TX0 pin, and received on the RX0 pin. The TX0 and RX0 pins are configured using the crossbar and the Port I/O registers, as detailed in Section “19. Port Input/Output” on page 169.

In typical UART communications, The transmit (TX) output of one device is connected to the receive (RX) input of the other device, either directly or through a bus transceiver, as shown in Figure 23.5.

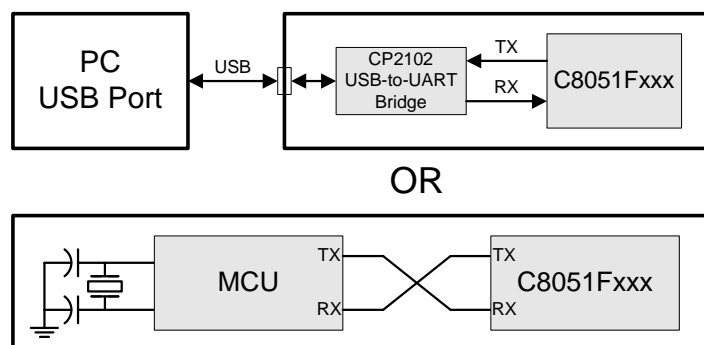


Figure 23.5. Typical UART Interconnect Diagram

23.3.1. Data Transmission

Data transmission is double-buffered and begins when software writes a data byte to the SBUF0 register. Writing to SBUF0 places data in the Transmit Holding Register, and the Transmit Holding Register Empty flag (THRE0) will be cleared to 0. If the UART's shift register is empty (i.e., no transmission in progress), the data will be placed in the Transmit Holding Register until the current transmission is complete. The TIO Transmit Interrupt Flag (SCON0.1) will be set at the end of any transmission (the beginning of the stop-bit time). If enabled, an interrupt will occur when TIO is set.

Note: THRE0 can have a momentary glitch high when the UART Transmit Holding Register is not empty. The glitch will occur some time after SBUF0 was written with the previous byte and does not occur if THRE0 is checked in the instruction(s) immediately following the write to SBUF0. When firmware writes SBUF0 and SBUF0 is not empty, TX0 will be stuck low until the next device reset. Firmware should use or poll on TIO rather than THRE0 for asynchronous UART writes that may have a random delay in between transactions.

If the extra bit function is enabled (XBE0 = 1) and the parity function is disabled (PE0 = '0'), the value of the TBX0 (SCON0.3) bit will be sent in the extra bit position. When the parity function is enabled (PE0 = 1), hardware will generate the parity bit according to the selected parity type (selected with S0PT[1:0]), and append it to the data field. Note: when parity is enabled, the extra bit function is not available.

23.3.2. Data Reception

Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be stored in the receive FIFO if the following conditions are met: the receive FIFO (3 bytes deep) must not be full, and the stop bit(s) must be logic 1. In the event that the receive FIFO is full, the incoming byte will be lost, and a Receive FIFO Overrun Error will be generated (OVR0 in register SCON0 will be set to logic 1). If the stop bit(s) were logic 0, the incoming data will not be stored in the receive FIFO. If the reception conditions are met, the data is stored in the receive FIFO, and

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SFR Definition 25.3. TMOD: Timer Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	C/T1	T1M[1:0]		GATE0	C/T0	T0M[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x89; SFR Page = All Pages

Bit	Name	Function
7	GATE1	Timer 1 Gate Control. 0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT1}}$ logic level. 1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT1}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 13.7).
6	C/T1	Counter/Timer 1 Select. 0: Timer: Timer 1 incremented by clock defined by T1M bit in register CKCON. 1: Counter: Timer 1 incremented by high-to-low transitions on external pin (T1).
5:4	T1M[1:0]	Timer 1 Mode Select. These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	Timer 0 Gate Control. 0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level. 1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 13.7).
2	C/T0	Counter/Timer 0 Select. 0: Timer: Timer 0 incremented by clock defined by T0M bit in register CKCON. 1: Counter: Timer 0 incremented by high-to-low transitions on external pin (T0).
1:0	T0M[1:0]	Timer 0 Mode Select. These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

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SFR Definition 25.11. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCC; SFR Page = 0x00

Bit	Name	Function
7:0	TMR2L[7:0]	Timer 2 Low Byte. In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

SFR Definition 25.12. TMR2H Timer 2 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCD; SFR Page = 0x00

Bit	Name	Function
7:0	TMR2H[7:0]	Timer 2 High Byte. In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

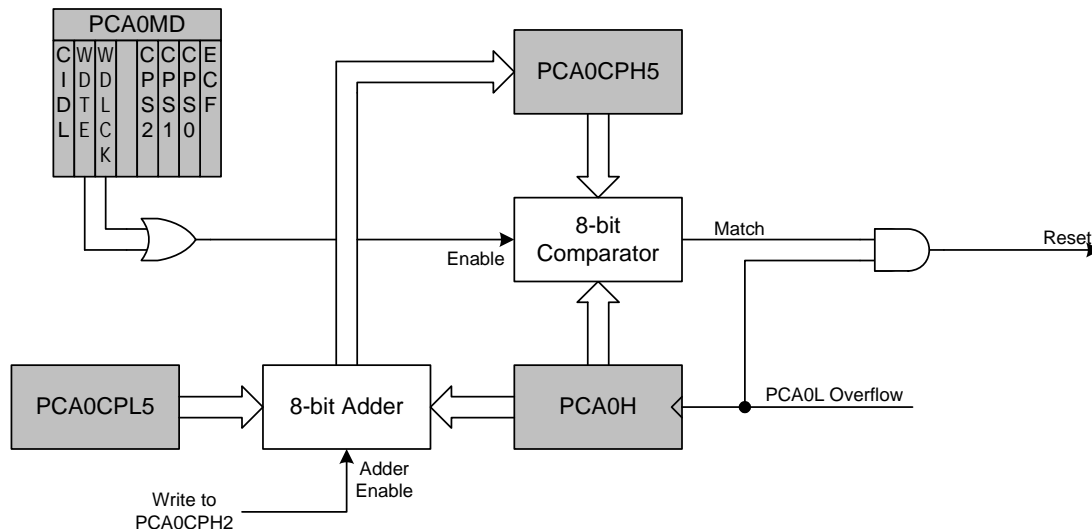


Figure 26.11. PCA Module 2 with Watchdog Timer Enabled

Note that the 8-bit offset held in PCA0CPH5 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 26.5, where PCA0L is the value of the PCA0L register at the time of the update.

$$\text{Offset} = (256 \times \text{PCA0CPL5}) + (256 - \text{PCA0L})$$

Equation 26.5. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH5 and PCA0H. Software may force a WDT reset by writing a 1 to the CCF5 flag (PCA0CN.5) while the WDT is enabled.

26.4.2. Watchdog Timer Usage

To configure the WDT, perform the following tasks:

- Disable the WDT by writing a 0 to the WDTE bit.
- Select the desired PCA clock source (with the CPS[2:0] bits).
- Load PCA0CPL5 with the desired WDT update offset value.
- Configure the PCA Idle mode (set CIDL if the WDT should be suspended while the CPU is in Idle mode).
- Enable the WDT by setting the WDTE bit to 1.
- Reset the WDT timer by writing to PCA0CPH5.

The PCA clock source and Idle mode select cannot be changed while the WDT is enabled. The watchdog timer is enabled by setting the WDTE or WDLCK bits in the PCA0MD register. When WDLCK is set, the WDT cannot be disabled until the next system reset. If WDLCK is not set, the WDT is disabled by clearing the WDTE bit.

The WDT is enabled following any reset. The PCA0 counter clock defaults to the system clock divided by 12, PCA0L defaults to 0x00, and PCA0CPL5 defaults to 0x00. Using Equation 26.5, this results in a WDT timeout interval of 256 PCA clock cycles, or 3072 system clock cycles. Table 26.3 lists some example timeout intervals for typical system clocks.

SFR Definition 26.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS[2:0]			ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Address = 0xD9; SFR Page = 0x00

Bit	Name	Function
7	CIDL	<p>PCA Counter/Timer Idle Control.</p> <p>Specifies PCA behavior when CPU is in Idle Mode.</p> <p>0: PCA continues to function normally while the system controller is in Idle Mode.</p> <p>1: PCA operation is suspended while the system controller is in Idle Mode.</p>
6	WDTE	<p>Watchdog Timer Enable</p> <p>If this bit is set, PCA Module 5 is used as the watchdog timer.</p> <p>0: Watchdog Timer disabled.</p> <p>1: PCA Module 5 enabled as Watchdog Timer.</p>
5	WDLCK	<p>Watchdog Timer Lock</p> <p>This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset.</p> <p>0: Watchdog Timer Enable unlocked.</p> <p>1: Watchdog Timer Enable locked.</p>
4	Unused	Read = 0b, Write = Don't care.
3:1	CPS[2:0]	<p>PCA Counter/Timer Pulse Select.</p> <p>These bits select the timebase source for the PCA counter</p> <p>000: System clock divided by 12</p> <p>001: System clock divided by 4</p> <p>010: Timer 0 overflow</p> <p>011: High-to-low transitions on ECI (max rate = system clock divided by 4)</p> <p>100: System clock</p> <p>101: External clock divided by 8 (synchronized with the system clock)</p> <p>11x: Reserved</p>
0	ECF	<p>PCA Counter/Timer Overflow Interrupt Enable.</p> <p>This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt.</p> <p>0: Disable the CF interrupt.</p> <p>1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.</p>

Note: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.

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SFR Definition 26.3. PCA0PWM: PCA PWM Configuration

Bit	7	6	5	4	3	2	1	0
Name	ARSEL	ECOV	COVF				CLSEL[1:0]	
Type	R/W	R/W	R/W	R	R	R	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD9; SFR Page = 0x0F

Bit	Name	Function
7	ARSEL	<p>Auto-Reload Register Select.</p> <p>This bit selects whether to read and write the normal PCA capture/compare registers (PCA0CPn), or the Auto-Reload registers at the same SFR addresses. This function is used to define the reload value for 9, 10, and 11-bit PWM modes. In all other modes, the Auto-Reload registers have no function.</p> <p>0: Read/Write Capture/Compare Registers at PCA0CPHn and PCA0CPLn. 1: Read/Write Auto-Reload Registers at PCA0CPHn and PCA0CPLn.</p>
6	ECOV	<p>Cycle Overflow Interrupt Enable.</p> <p>This bit sets the masking of the Cycle Overflow Flag (COVF) interrupt.</p> <p>0: COVF will not generate PCA interrupts. 1: A PCA interrupt will be generated when COVF is set.</p>
5	COVF	<p>Cycle Overflow Flag.</p> <p>This bit indicates an overflow of the 8th, 9th, 10th, or 11th bit of the main PCA counter (PCA0). The specific bit used for this flag depends on the setting of the Cycle Length Select bits. The bit can be set by hardware or software, but must be cleared by software.</p> <p>0: No overflow has occurred since the last time this bit was cleared. 1: An overflow has occurred since the last time this bit was cleared.</p>
4:2	Unused	Read = 000b; Write = Don't care.
1:0	CLSEL[1:0]	<p>Cycle Length Select.</p> <p>When 16-bit PWM mode is not selected, these bits select the length of the PWM cycle, between 8, 9, 10, or 11 bits. This affects all channels configured for PWM which are not using 16-bit PWM mode. These bits are ignored for individual channels configured to 16-bit PWM mode.</p> <p>00: 8 bits. 01: 9 bits. 10: 10 bits. 11: 11 bits.</p>

27. C2 Interface

C8051F55x/56x/57x devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

27.1. C2 Interface Registers

The following describes the C2 registers necessary to perform Flash programming through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 27.1. C2ADD: C2 Address

Bit	7	6	5	4	3	2	1	0
Name	C2ADD[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function										
7:0	C2ADD[7:0]	<p>C2 Address. The C2ADD register is accessed via the C2 interface to select the target Data register for C2 Data Read and Data Write commands.</p> <table border="1"> <thead> <tr> <th>Address</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Selects the Device ID register for Data Read instructions</td> </tr> <tr> <td>0x01</td> <td>Selects the Revision ID register for Data Read instructions</td> </tr> <tr> <td>0x02</td> <td>Selects the C2 Flash Programming Control register for Data Read/Write instructions</td> </tr> <tr> <td>0xB4</td> <td>Selects the C2 Flash Programming Data register for Data Read/Write instructions</td> </tr> </tbody> </table>	Address	Description	0x00	Selects the Device ID register for Data Read instructions	0x01	Selects the Revision ID register for Data Read instructions	0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions	0xB4	Selects the C2 Flash Programming Data register for Data Read/Write instructions
Address	Description											
0x00	Selects the Device ID register for Data Read instructions											
0x01	Selects the Revision ID register for Data Read instructions											
0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions											
0xB4	Selects the C2 Flash Programming Data register for Data Read/Write instructions											