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Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f557-im

C8051F55x/56x/57x

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6.2. Output Code Formatting

The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code. When the repeat count is set to 1, conversion codes are represented in 12-bit unsigned integer format and the output conversion code is updated after each conversion. Inputs are measured from 0 to $V_{REF} \times 4095/4096$. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.2). Unused bits in the ADC0H and ADC0L registers are set to 0. Example codes are shown below for both right-justified and left-justified data.

Input Voltage	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
$V_{REF} \times 4095/4096$	0x0FFF	0xFFFF0
$V_{REF} \times 2048/4096$	0x0800	0x8000
$V_{REF} \times 2047/4096$	0x07FF	0x7FF0
0	0x0000	0x0000

When the ADC0 Repeat Count is greater than 1, the output conversion code represents the accumulated result of the conversions performed and is updated after the last conversion in the series is finished. Sets of 4, 8, or 16 consecutive samples can be accumulated and represented in unsigned integer format. The repeat count can be selected using the AD0RPT bits in the ADC0CF register. The value must be right-justified (AD0LJST = 0), and unused bits in the ADC0H and ADC0L registers are set to 0. The following example shows right-justified codes for repeat counts greater than 1. Notice that accumulating 2^n samples is equivalent to left-shifting by n bit positions when all samples returned from the ADC have the same value.

Input Voltage	Repeat Count = 4	Repeat Count = 8	Repeat Count = 16
$V_{REF} \times 4095/4096$	0x3FFC	0x7FF8	0xFFFF0
$V_{REF} \times 2048/4096$	0x2000	0x4000	0x8000
$V_{REF} \times 2047/4096$	0x1FFC	0x3FF8	0x7FF0
0	0x0000	0x0000	0x0000

6.2.1. Settling Time Requirements

A minimum tracking time is required before an accurate conversion is performed. This tracking time is determined by any series impedance, including the AMUX0 resistance, the ADC0 sampling capacitance, and the accuracy required for the conversion.

Figure 6.5 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 6.1. When measuring the Temperature Sensor output, use the settling time specified in Table 5.10. When measuring V_{DD} with respect to GND, R_{TOTAL} reduces to R_{MUX} . See Table 5.9 for ADC0 minimum settling time requirements as well as the mux impedance and sampling capacitor values.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 6.1. ADC0 Settling Time Requirements

Where:

SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB).

t is the required settling time in seconds. R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance. n is the ADC resolution in bits (10).

10.2. Instruction Set

The instruction set of the CIP-51 System Controller is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can be used to develop software for the CIP-51. All CIP-51 instructions are the binary and functional equivalent of their MCS-51™ counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

10.2.1. Instruction and CPU Timing

In many 8051 implementations, a distinction is made between machine cycles and clock cycles, with machine cycles varying from 2 to 12 clock cycles in length. However, the CIP-51 implementation is based solely on clock cycle timing. All instruction timings are specified in terms of clock cycles.

Due to the pipelined architecture of the CIP-51, most instructions execute in the same number of clock cycles as there are program bytes in the instruction. Conditional branch instructions take one less clock cycle to complete when the branch is not taken as opposed to when the branch is taken. Table 10.1 is the CIP-51 Instruction Set Summary, which includes the mnemonic, number of bytes, and number of clock cycles for each instruction.

SFR Definition 10.3. SP: Stack Pointer

Bit	7	6	5	4	3	2	1	0
Name	SP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	1	1	1

SFR Address = 0x81; SFR Page = All Pages

Bit	Name	Function
7:0	SP[7:0]	Stack Pointer. The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 10.4. ACC: Accumulator

Bit	7	6	5	4	3	2	1	0
Name	ACC[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7:0	ACC[7:0]	Accumulator. This register is the accumulator for arithmetic operations.

SFR Definition 10.5. B: B Register

Bit	7	6	5	4	3	2	1	0
Name	B[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7:0	B[7:0]	B Register. This register serves as a second accumulator for certain arithmetic operations.

10.4. Serial Number Special Function Registers (SFRs)

The C8051F55x/56x/57x devices include four SFRs, SN0 through SN3, that are pre-programmed during production with a unique, 32-bit serial number. The serial number provides a unique identification number for each device and can be read from the application firmware. If the serial number is not used in the application, these four registers can be used as general purpose SFRs.

SFR Definition 10.7. SNn: Serial Number n

Bit	7	6	5	4	3	2	1	0
Name	SERNUMn[7:0]							
Type	R/W							
Reset	Varies—Unique 32-bit value							

SFR Addresses: SN0 = 0xF9; SN1 = 0xFA; SN2 = 0xFB; SN3 = 0xFC; SFR Page = 0x0F;

Bit	Name	Function
7:0	SERNUMn[7:0]	Serial Number Bits. The four serial number registers form a 32-bit serial number, with SN3 as the most significant byte and SN0 as the least significant byte.

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On exit from the PCA interrupt service routine, the CIP-51 will return to the CAN0 ISR. On execution of the RETI instruction, SFR Page 0x00 used to access the PCA registers will be automatically popped off of the SFR Page Stack, and the contents of the SFRNEXT register will be moved to the SFRPAGE register. Software in the CAN0 ISR can continue to access SFRs as it did prior to the PCA interrupt. Likewise, the contents of SFRLAST are moved to the SFRNEXT register. Recall this was the SFR Page value 0x00 being used to access SPI0DAT before the CAN0 interrupt occurred. See Figure 12.5.

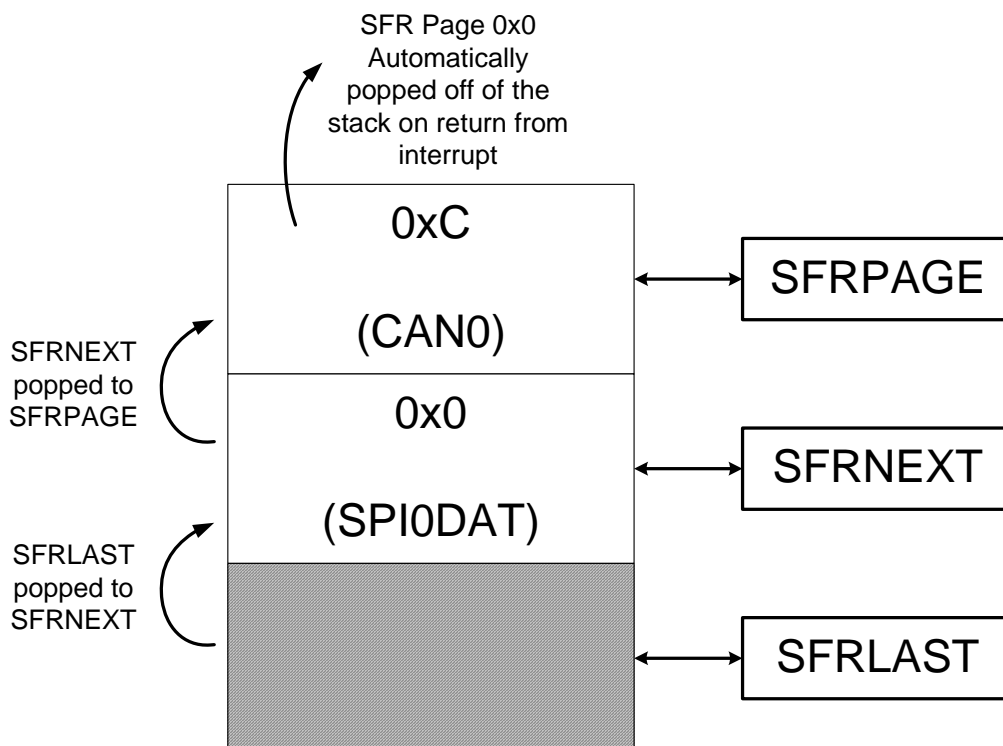


Figure 12.5. SFR Page Stack Upon Return From PCA Interrupt

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Table 12.1. Special Function Register (SFR) Memory Map for Pages 0x00 and 0x0F

Address	Page	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
F8 0		SPI0CN	PCA0L SN0	PCA0H SN1	PCA0CPL0 SN2	PCA0CPH0 SN3	PCACPL4	PCACPH4	VDM0CN
F0 0		B (All Pages)	P0MAT P0MDIN	P0MASK P1MDIN	P1MAT P2MDIN	P1MASK P3MDIN		EIP1 EIP1	EIP2 EIP2
E8 0		ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPL3	RSTSRC
E0 0		ACC (All Pages)	XBR0	XBR1	CCH0CN	IT01CF		EIE1 (All Pages)	EIE2 (All Pages)
D8 0		PCA0CN	PCA0MD PCA0PWM	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	PCA0CPM5
D0 0		PSW (All Pages)	REF0CN	LIN0DATA	LIN0ADDR	P0SKIP	P1SKIP	P2SKIP	P3SKIP
C8 0		TMR2CN	REG0CN LIN0CF	TMR2RLL	TMR2RLH	TMR2L	TMR2H	PCA0CPL5	PCA0CPH5
C0 0		SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	XBR2
B8 0		IP (All Pages)		ADC0TK	ADC0MX	ADC0CF	ADC0L	ADC0H	
B0 0		P3 (All Pages)	P2MAT	P2MASK EMI0CF			P4 (All Pages)	FLSCL (All Pages)	FLKEY (All Pages)
A8 0		IE (All Pages)	SMOD0	EMI0CN EMI0TC	SBCON0	SBRLLO	SBRLH0	P3MAT P3MDOUT	P3MASK P4MDOUT
A0 0		P2 (All Pages)	SPI0CFG OSCICN	SPI0CKR OSCICRS	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	SFRPAGE (All Pages)
98 0		SCON0	SBUF0	CPT0CN	CPT0MD	CPT0MX	CPT1CN	CPT1MD OSCIFIN	CPT1MX OSCXCN
90 0		P1 (All Pages)	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H		CLKMUL
88 0		TCON (All Pages)	TMOD (All Pages)	TL0 (All Pages)	TL1 (All Pages)	TH0 (All Pages)	TH1 (All Pages)	CKCON (All Pages)	PSCTL CLKSEL
80 0		P0 (All Pages)	SP (All Pages)	DPL (All Pages)	DPH (All Pages)	SFR0CN (All Pages)	SFRNEXT (All Pages)	SFRLAST (All Pages)	PCON (All Pages)
		0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

(bit addressable)

Table 17.1. EMIF Pinout (C8051F568-9 and 'F570-5)

Multiplexed Mode	
Signal Name	Port Pin
$\overline{\text{RD}}$	P1.6
$\overline{\text{WR}}$	P1.7
ALE	P1.5
D0/A0	P3.0
D1/A1	P3.1
D2/A2	P3.2
D3/A3	P3.3
D4/A4	P3.4
D5/A5	P3.5
D6/A6	P3.6
D7/A7	P3.7
A8	P2.0
A9	P2.1
A10	P2.2
A11	P2.3
A12	P2.4
A13	P2.5
A14	P2.6
A15	P2.7

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17.5.3. Split Mode with Bank Select

When EMI0CF[3:2] are set to 10, the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the internal XRAM size boundary will access on-chip XRAM space.
- Effective addresses above the internal XRAM size boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. The upper 8-bits of the Address Bus A[15:8] are determined by EMI0CN, and the lower 8-bits of the Address Bus A[7:0] are determined by R0 or R1. All 16-bits of the Address Bus A[15:0] are driven in "Bank Select" mode.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

17.5.4. External Only

When EMI0CF[3:2] are set to 11, all MOVX operations are directed to off-chip space. On-chip XRAM is not visible to the CPU. This mode is useful for accessing off-chip memory located between 0x0000 and the internal XRAM size boundary.

- 8-bit MOVX operations ignore the contents of EMI0CN. The upper Address bits A[15:8] are not driven (identical behavior to an off-chip access in "Split Mode without Bank Select" described above). This allows the user to manipulate the upper address bits at will by setting the Port state directly. The lower 8-bits of the effective address A[7:0] are determined by the contents of R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine the effective address A[15:0]. The full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

17.6. Timing

The timing parameters of the External Memory Interface can be configured to enable connection to devices having different setup and hold time requirements. The Address Setup time, Address Hold time, \overline{RD} and \overline{WR} strobe widths, and in multiplexed mode, the width of the ALE pulse are all programmable in units of SYSCLK periods through EMI0TC, shown in SFR Definition 17.3, and EMI0CF[1:0].

The timing for an off-chip MOVX instruction can be calculated by adding 4 SYSCLK cycles to the timing parameters defined by the EMI0TC register. Assuming non-multiplexed operation, the minimum execution time for an off-chip XRAM operation is 5 SYSCLK cycles (1 SYSCLK for \overline{RD} or \overline{WR} pulse + 4 SYSCLKs). For multiplexed operations, the Address Latch Enable signal will require a minimum of 2 additional SYSCLK cycles. Therefore, the minimum execution time for an off-chip XRAM operation in multiplexed mode is 7 SYSCLK cycles (2 for \overline{ALE} + 1 for \overline{RD} or \overline{WR} + 4). The programmable setup and hold times default to the maximum delay settings after a reset. Table 17.2 lists the ac parameters for the External Memory Interface, and Figure 17.3 through Figure 17.5 show the timing diagrams for the different External Memory Interface modes and MOVX operations.

Table 17.2. AC Parameters for External Memory Interface

Parameter	Description	Min*	Max*	Units
T_{ACS}	Address/Control Setup Time	0	$3 \times T_{SYSCLK}$	ns
T_{ACW}	Address/Control Pulse Width	$1 \times T_{SYSCLK}$	$16 \times T_{SYSCLK}$	ns
T_{ACH}	Address/Control Hold Time	0	$3 \times T_{SYSCLK}$	ns
T_{ALEH}	Address Latch Enable High Time	$1 \times T_{SYSCLK}$	$4 \times T_{SYSCLK}$	ns
T_{ALEL}	Address Latch Enable Low Time	$1 \times T_{SYSCLK}$	$4 \times T_{SYSCLK}$	ns
T_{WDS}	Write Data Setup Time	$1 \times T_{SYSCLK}$	$19 \times T_{SYSCLK}$	ns
T_{WDH}	Write Data Hold Time	0	$3 \times T_{SYSCLK}$	ns
T_{RDS}	Read Data Setup Time	20		ns
T_{RDH}	Read Data Hold Time	0		ns
*Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).				

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SFR Definition 19.1. XBR0: Port I/O Crossbar Register 0

Bit	7	6	5	4	3	2	1	0
Name	CP1AE	CP1E	CP0AE	CP0E	SMB0E	SPI0E	CAN0E	URT0E
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE1; SFR Page = 0x0F

Bit	Name	Function
7	CP1AE	Comparator1 Asynchronous Output Enable. 0: Asynchronous CP1 unavailable at Port pin. 1: Asynchronous CP1 routed to Port pin.
6	CP1E	Comparator1 Output Enable. 0: CP1 unavailable at Port pin. 1: CP1 routed to Port pin.
5	CP0AE	Comparator0 Asynchronous Output Enable. 0: Asynchronous CP0 unavailable at Port pin. 1: Asynchronous CP0 routed to Port pin.
4	CP0E	Comparator0 Output Enable. 0: CP0 unavailable at Port pin. 1: CP0 routed to Port pin.
3	SMB0E	SMBus I/O Enable. 0: SMBus I/O unavailable at Port pins. 1: SMBus I/O routed to Port pins.
2	SPI0E	SPI I/O Enable. 0: SPI I/O unavailable at Port pins. 1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO pins.
1	CAN0E	CAN I/O Output Enable. 0: CAN I/O unavailable at Port pins. 1: CAN_TX, CAN_RX routed to Port pins P0.6 and P0.7.
0	URT0E	UART I/O Output Enable. 0: UART I/O unavailable at Port pin. 1: UART TX0, RX0 routed to Port pins P0.4 and P0.5.

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SFR Definition 19.13. P0MDIN: Port 0 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF1; SFR Page = 0x0F

Bit	Name	Function
7:0	P0MDIN[7:0]	Analog Configuration Bits for P0.7–P0.0 (respectively). Port pins configured for analog mode have their weak pull-up and digital receiver disabled. For analog mode, the pin also needs to be configured for open-drain mode in the P0MDOUT register. 0: Corresponding P0.n pin is configured for analog mode. 1: Corresponding P0.n pin is not configured for analog mode.

SFR Definition 19.14. P0MDOUT: Port 0 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA4; SFR Page = 0x0F

Bit	Name	Function
7:0	P0MDOUT[7:0]	Output Configuration Bits for P0.7–P0.0 (respectively). These bits are ignored if the corresponding bit in register P0MDIN is logic 0. 0: Corresponding P0.n Output is open-drain. 1: Corresponding P0.n Output is push-pull.

SFR Definition 19.23. P2SKIP: Port 2 Skip

Bit	7	6	5	4	3	2	1	0
Name	P2SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD6; SFR Page = 0x0F

Bit	Name	Function
7:0	P2SKIP[7:0]	Port 2 Crossbar Skip Enable Bits. These bits select Port 2 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P2.n pin is not skipped by the Crossbar. 1: Corresponding P2.n pin is skipped by the Crossbar.
Note: P2.2-P2.7 are available on 40-pin and 32-pin packages.		

SFR Definition 19.24. P3: Port 3

Bit	7	6	5	4	3	2	1	0
Name	P3[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xB0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P3[7:0]	Port 3 Data. Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P3.n Port pin is logic LOW. 1: P3.n Port pin is logic HIGH.
Note: P3.0 is available on 40-pin and 32-pin packages. P3.1-P3.7 are available on 40-pin packages				

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20.7.2. LIN Indirect Access SFR Registers Definitions

Table 20.4 lists the 15 indirect registers used to configured and communicate with the LIN controller.

Table 20.4. LIN Registers* (Indirectly Addressable)

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LIN0DT1	0x00	DATA1[7:0]							
LIN0DT2	0x01	DATA2[7:0]							
LIN0DT3	0x02	DATA3[7:0]							
LIN0DT4	0x03	DATA4[7:0]							
LIN0DT5	0x04	DATA5[7:0]							
LIN0DT6	0x05	DATA6[7:0]							
LIN0DT7	0x06	DATA7[7:0]							
LIN0DT8	0x07	DATA8[7:0]							
LIN0CTRL	0x08	STOP(s)	SLEEP(s)	TXRX	DTACK(s)	RSTINT	RSTERR	WUPREQ	STREQ(m)
LIN0ST	0x09	ACTIVE	IDLTOU	ABORT(s)	DTREQ(s)	LININT	ERROR	WAKEUP	DONE
LIN0ERR	0x0A				SYNCH(s)	PRTY(s)	TOUT	CHK	BITERR
LIN0SIZE	0x0B	ENHCHK				LINSIZE[3:0]			
LIN0DIV	0x0C	DIVLSB[7:0]							
LIN0MUL	0x0D	PRESCL[1:0]		LINMUL[4:0]					DIV9
LIN0ID	0x0E			ID5	ID4	ID3	ID2	ID1	ID0
*Note: These registers are used in both master and slave mode. The register bits marked with (m) are accessible only in Master mode while the register bits marked with (s) are accessible only in slave mode. All other registers are accessible in both modes.									

LIN Register Definition 20.8. LIN0SIZE: LIN0 Message Size Register

Bit	7	6	5	4	3	2	1	0
Name	ENHCHK				LINSIZE[3:0]			
Type	R/W	R	R	R	R/W			
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x0B

Bit	Name	Function
7	ENHCHK	Checksum Selection Bit. 0: Use the classic, specification 1.3 compliant checksum. Checksum covers the data bytes. 1: Use the enhanced, specification 2.0 compliant checksum. Checksum covers data bytes and protected identifier.
6:4	Unused	Read = 000b; Write = Don't Care
3:0	LINSIZE[3:0]	Data Field Size. 0000: 0 data bytes 0001: 1 data byte 0010: 2 data bytes 0011: 3 data bytes 0100: 4 data bytes 0101: 5 data bytes 0110: 6 data bytes 0111: 7 data bytes 1000: 8 data bytes 1001-1110: RESERVED 1111: Use the ID[1:0] bits (LIN0ID[5:4]) to determine the data length.

22.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

1. The I²C-Bus and How to Use It (including specifications), Philips Semiconductor.
2. The I²C-Bus Specification—Version 2.0, Philips Semiconductor.
3. System Management Bus Specification—Version 1.1, SBS Implementers Forum.

22.2. SMBus Configuration

Figure 22.2 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels. The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pullup resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively.

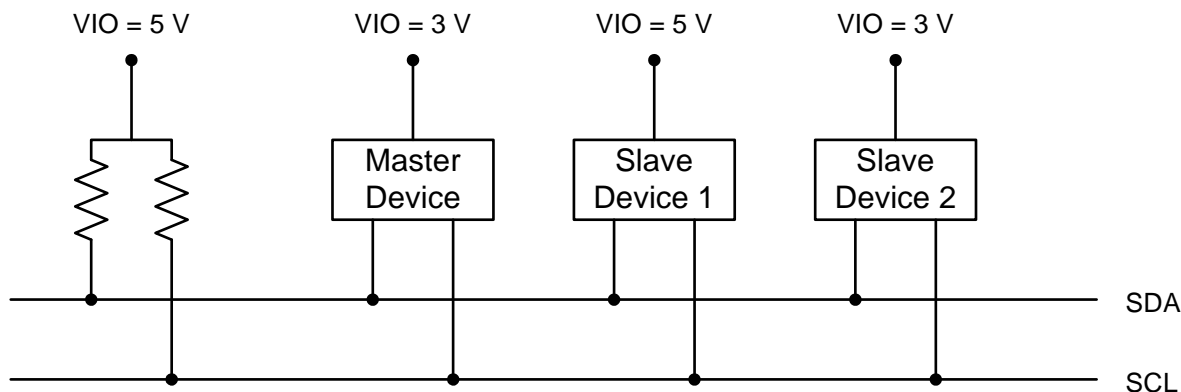


Figure 22.2. Typical SMBus Configuration

22.3. SMBus Operation

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. The SMBus interface may operate as a master or a slave, and multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. It is not necessary to specify one device as the Master in a system; any device who transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Bytes that are received (by a master or slave) are acknowledged (ACK) with a low SDA during a high SCL (see Figure 22.3). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation.

Table 22.4. SMBus Status Decoding

Mode	Values Read				Current SMBus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X	1100
	1100	0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X	1110
						Abort transfer.	0	1	X	—
	0	0	1		A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0DAT.	0	0	X	1100
						End transfer with STOP.	0	1	X	—
						End transfer with STOP and start another transfer.	1	1	X	—
						Send repeated START.	1	0	X	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT).	0	0	X	1000
Master Receiver	1000	1	0	X	A master data byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	1000
						Send NACK to indicate last byte, and send STOP.	0	1	0	—
						Send NACK to indicate last byte, and send STOP followed by START.	1	1	0	1110
						Send ACK followed by repeated START.	1	0	1	1110
						Send NACK to indicate last byte, and send repeated START.	1	0	0	1110
						Send ACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	1	1100
						Send NACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	0	1100

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SFR Definition 25.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3		T3XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = 0x00

Bit	Name	Function
7	TF3H	Timer 3 High Byte Overflow Flag. Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	Timer 3 Low Byte Overflow Flag. Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	Timer 3 Low Byte Interrupt Enable. When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	Timer 3 Capture Mode Enable. 0: Timer 3 Capture Mode is disabled. 1: Timer 3 Capture Mode is enabled.
3	T3SPLIT	Timer 3 Split Mode Enable. When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload. 0: Timer 3 operates in 16-bit auto-reload mode. 1: Timer 3 operates as two 8-bit auto-reload timers.
2	TR3	Timer 3 Run Control. Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1	Unused	Read = 0b; Write = Don't Care
0	T3XCLK	Timer 3 External Clock Select. This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 3 clock is the system clock divided by 12. 1: Timer 3 clock is the external clock divided by 8 (synchronized with SYSCLK).

SFR Definition 26.4. PCA0CPMn: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPM0 = 0xDA, PCA0CPM1 = 0xDB, PCA0CPM2 = 0xDC; PCA0CPM3 = 0xDD, PCA0CPM4 = 0xDE, PCA0CPM5 = 0xDF, SFR Page (all registers) = 0x00

Bit	Name	Function
7	PWM16n	16-bit Pulse Width Modulation Enable. This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOMn	Comparator Function Enable. This bit enables the comparator function for PCA module n when set to 1.
5	CAPPn	Capture Positive Function Enable. This bit enables the positive edge capture for PCA module n when set to 1.
4	CAPNn	Capture Negative Function Enable. This bit enables the negative edge capture for PCA module n when set to 1.
3	MATn	Match Function Enable. This bit enables the match function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
2	TOGn	Toggle Function Enable. This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWMn	Pulse Width Modulation Mode Enable. This bit enables the PWM function for PCA module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8 to 11-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0	ECCFn	Capture/Compare Flag Interrupt Enable. This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt. 0: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set.
Note: When the WDTE bit is set to 1, the PCA0CPM5 register cannot be modified, and module 5 acts as the watchdog timer. To change the contents of the PCA0CPM5 register or the function of module 5, the Watchdog Timer must be disabled.		

SFR Definition 26.7. PCA0CPLn: PCA Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPL0 = 0xFB, PCA0CPL1 = 0xE9, PCA0CPL2 = 0xEB, PCA0CPL3 = 0xED, PCA0CPL4 = 0xFD, PCA0CPL5 = 0xCE; SFR Page (all registers) = 0x00

Bit	Name	Function
7:0	PCA0CPn[7:0]	PCA Capture Module Low Byte. The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n. This register address also allows access to the low byte of the corresponding PCA channel's auto-reload value for 9, 10, or 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will clear the module's ECOMn bit to a 0.		

SFR Definition 26.8. PCA0CPHn: PCA Capture Module High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPH0 = 0xFC, PCA0CPH1 = 0xEA, PCA0CPH2 = 0xEC, PCA0CPH3 = 0xEE, PCA0CPH4 = 0xFE, PCA0CPH5 = 0xCF; SFR Page (all registers) = 0x00

Bit	Name	Function
7:0	PCA0CPn[15:8]	PCA Capture Module High Byte. The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n. This register address also allows access to the high byte of the corresponding PCA channel's auto-reload value for 9, 10, or 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will set the module's ECOMn bit to a 1.		