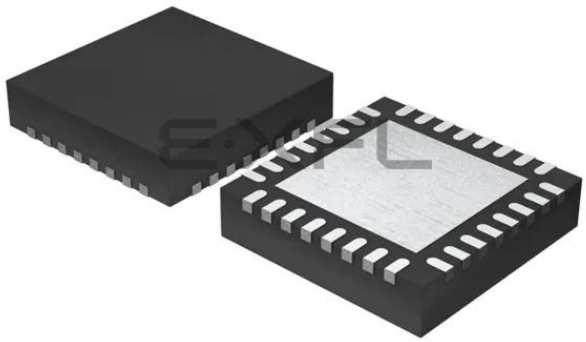

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f562-im

List of Figures

4. Package Specifications

4.1. QFN-40 Package Specifications

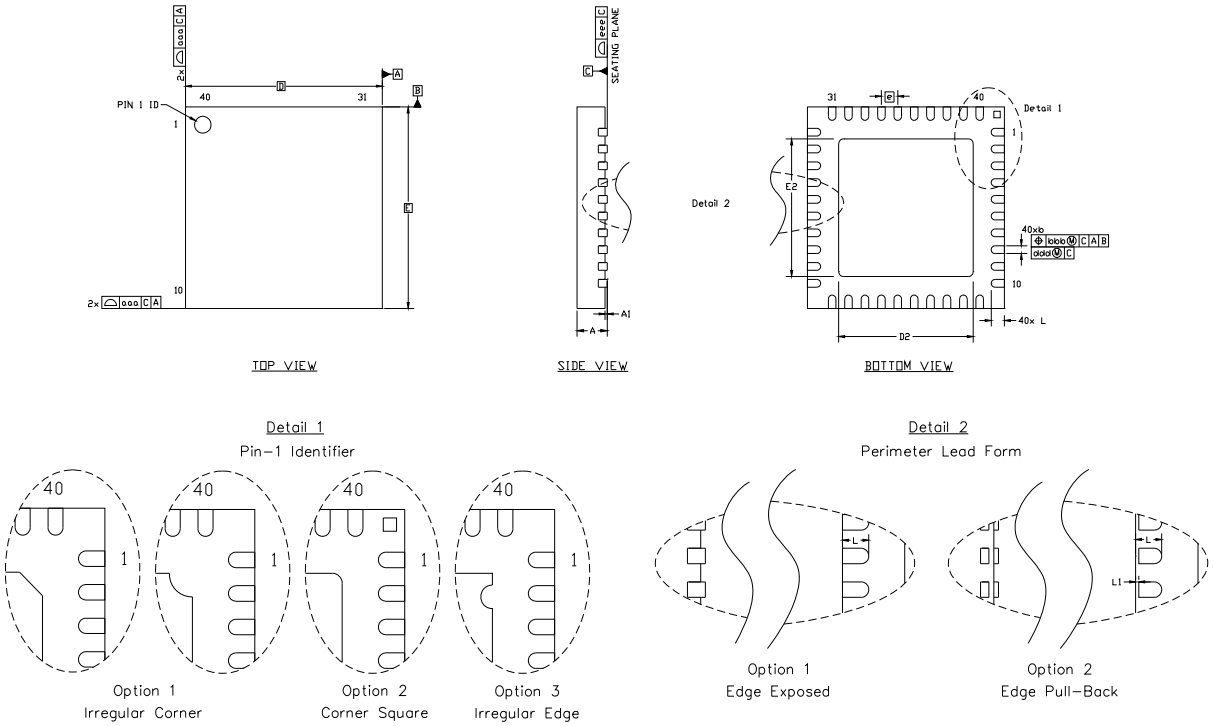

Figure 4.1. QFN-40 Package Drawing

Table 4.1. QFN-40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00		0.05
b	0.18	0.23	0.28
D		6.00 BSC	
D2	4.00	4.10	4.20
e		0.50 BSC	
E		6.00 BSC	

Dimension	Min	Typ	Max
E2	4.00	4.10	4.20
L	0.35	0.40	0.45
L1			0.10
aaa			0.10
bbb			0.10
ddd			0.05
eee			0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VJJD-5, except for features A, D2, and E2 which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

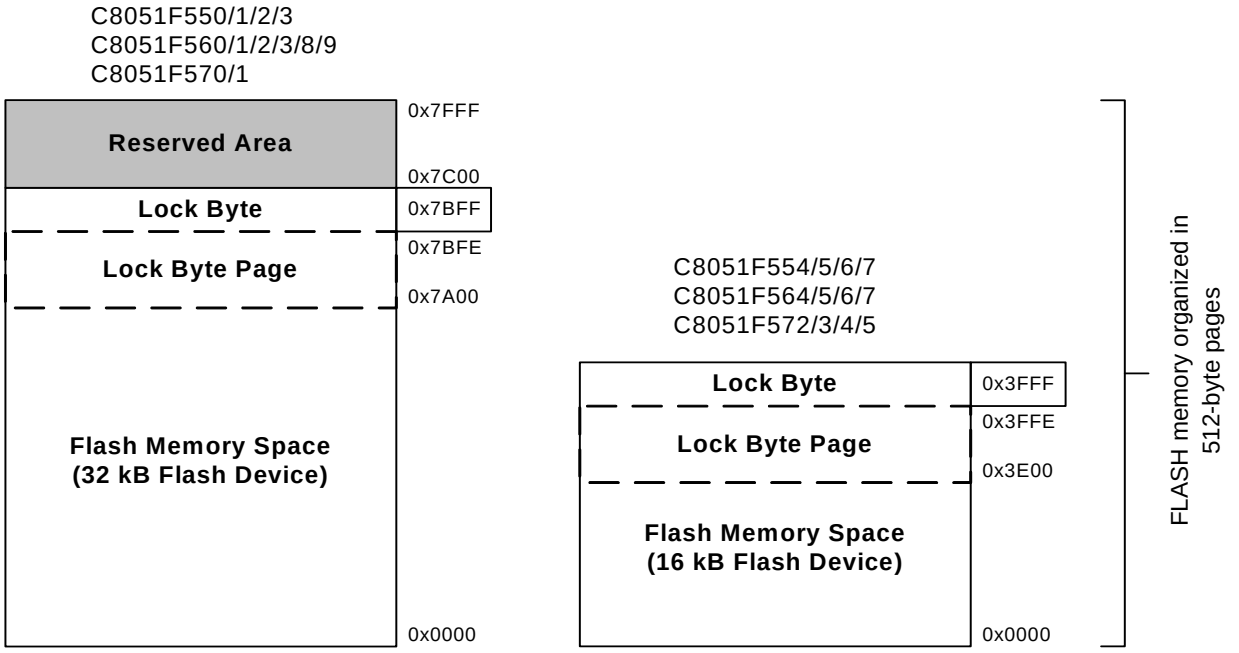

Figure 11.2. Flash Program Memory Map

11.1.1. MOVX Instruction and Program Memory

The MOVX instruction in an 8051 device is typically used to access external data memory. On the C8051F55x/56x/57x devices, the MOVX instruction is normally used to read and write on-chip XRAM, but can be re-configured to write and erase on-chip Flash memory space. MOVC instructions are always used to read Flash memory, while MOVX write instructions are used to erase and write Flash. This Flash access feature provides a mechanism for the C8051F55x/56x/57x to update program code and use the program memory space for non-volatile data storage. Refer to Section “14. Flash Memory” on page 124 for further details.

11.2. Data Memory

The C8051F55x/56x/57x devices include 2304 bytes of RAM data memory. 256 bytes of this memory is mapped into the internal RAM space of the 8051. The other 2048 bytes of this memory is on-chip “external” memory. The data memory map is shown in Figure 11.1 for reference.

11.2.1. Internal RAM

There are 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 11.1 illustrates the data memory organization of the

Table 12.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
SMB0CF	0xC1	SMBus0 Configuration	224
SMB0CN	0xC0	SMBus0 Control	226
SMB0DAT	0xC2	SMBus0 Data	228
SMOD0	0xA9	UART0 Mode	243
SN0	0xF9	Serial Number 0	91
SN1	0xFA	Serial Number 1	91
SN2	0xFB	Serial Number 2	91
SN3	0xFC	Serial Number 3	91
SP	0x81	Stack Pointer	89
SPI0CFG	0xA1	SPI0 Configuration	253
SPI0CKR	0xA2	SPI0 Clock Rate Control	255
SPI0CN	0xF8	SPI0 Control	254
SPI0DAT	0xA3	SPI0 Data	255
TCON	0x88	Timer/Counter Control	265
TH0	0x8C	Timer/Counter 0 High	268
TH1	0x8D	Timer/Counter 1 High	268
TL0	0x8A	Timer/Counter 0 Low	267
TL1	0x8B	Timer/Counter 1 Low	267
TMOD	0x89	Timer/Counter Mode	266
TMR2CN	0xC8	Timer/Counter 2 Control	272
TMR2H	0xCD	Timer/Counter 2 High	274
TMR2L	0xCC	Timer/Counter 2 Low	274
TMR2RLH	0xCB	Timer/Counter 2 Reload High	273
TMR2RLL	0xCA	Timer/Counter 2 Reload Low	273
TMR3CN	0x91	Timer/Counter 3 Control	278
TMR3H	0x95	Timer/Counter 3 High	280
TMR3L	0x94	Timer/Counter 3 Low	280
TMR3RLH	0x93	Timer/Counter 3 Reload High	279
TMR3RLL	0x92	Timer/Counter 3 Reload Low	279
VDM0CN	0xFF	V_{DD} Monitor Control	141
XBR0	0xE1	Port I/O Crossbar Control 0	176
XBR1	0xE2	Port I/O Crossbar Control 1	177
XBR2	0xC7	Port I/O Crossbar Control 2	178

17.4. Multiplexed Mode

The External Memory Interface operates only in a Multiplexed mode. In Multiplexed mode, the Data Bus and the lower 8-bits of the Address Bus share the same Port pins: AD[7:0]. In this mode, an external latch (74HC373 or equivalent logic gate) is used to hold the lower 8-bits of the RAM address. The external latch is controlled by the ALE (Address Latch Enable) signal, which is driven by the External Memory Interface logic. An example of a Multiplexed Configuration is shown in Figure 17.1.

In Multiplexed mode, the external MOVX operation can be broken into two phases delineated by the state of the ALE signal. During the first phase, ALE is high and the lower 8-bits of the Address Bus are presented to AD[7:0]. During this phase, the address latch is configured such that the Q outputs reflect the states of the 'D' inputs. When ALE falls, signaling the beginning of the second phase, the address latch outputs remain fixed and are no longer dependent on the latch inputs. Later in the second phase, the Data Bus controls the state of the AD[7:0] port at the time $\overline{RD}$ or $\overline{WR}$ is asserted.

See Section "17.6.1. Multiplexed Mode" on page 153 for more information.

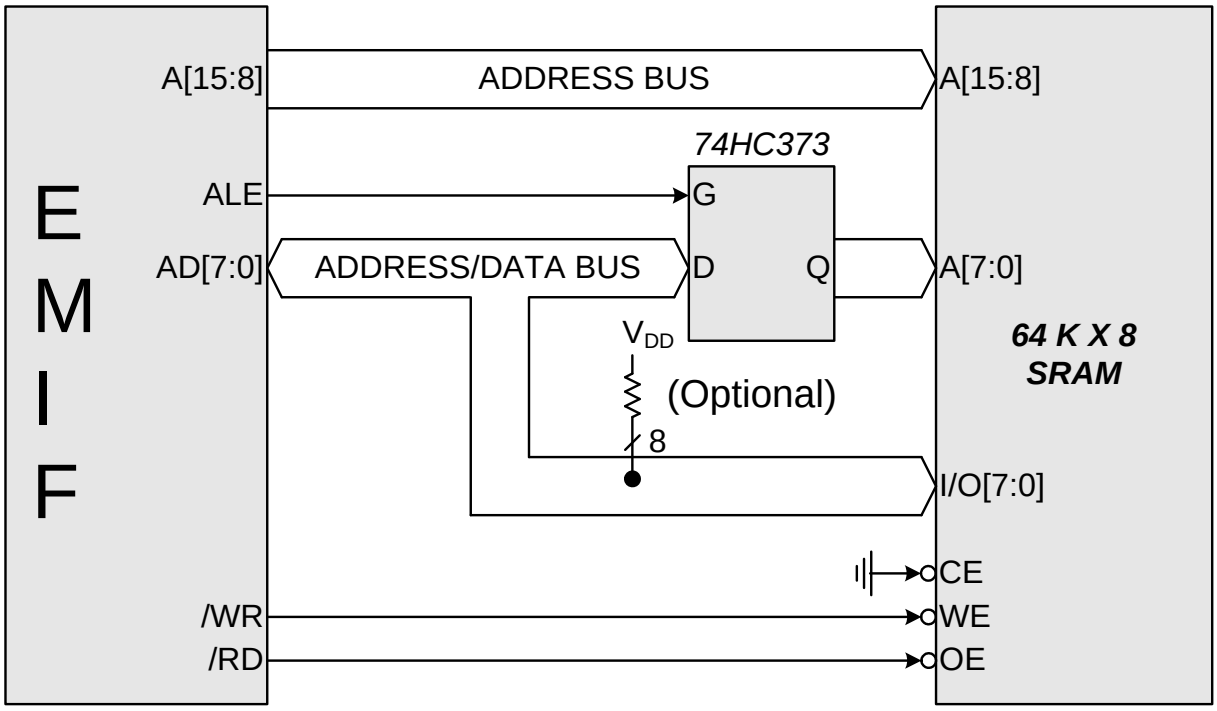

Figure 17.1. Multiplexed Configuration Example

SFR Definition 19.2. XBR1: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	T1E	T0E	ECIE	PCA0ME[2:0]			SYSCKE	Reserved
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE2; SFR Page = 0x0F

Bit	Name	Function
7	T1E	**T1 Enable.** 0: T1 unavailable at Port pin. 1: T1 routed to Port pin.
6	T0E	**T0 Enable.** 0: T0 unavailable at Port pin. 1: T0 routed to Port pin.
5	ECIE	**PCA0 External Counter Input Enable.** 0: ECI unavailable at Port pin. 1: ECI routed to Port pin.
4:2	PCA0ME[2:0]	**PCA Module I/O Enable Bits.** 000: All PCA I/O unavailable at Port pins. 001: CEX0 routed to Port pin. 010: CEX0, CEX1 routed to Port pins. 011: CEX0, CEX1, CEX2 routed to Port pins. 100: CEX0, CEX1, CEX2, CEX3 routed to Port pins. 101: CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins. 110: CEX0, CEX1, CEX2, CEX3, CEX4, CEX5 routed to Port pins. 111: RESERVED
1	SYSCKE	**/SYSCLK Output Enable.** 0: /SYSCLK unavailable at Port pin. 1: /SYSCLK output routed to Port pin.
0	Reserved	Always Write to 0.

19.6. Special Function Registers for Accessing and Configuring Port I/O

All Port I/O are accessed through corresponding special function registers (SFRs) that are both byte addressable and bit addressable, except for P4 which is only byte addressable. When writing to a Port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the Port's input pins are returned regardless of the XBRn settings (i.e., even when the pin is assigned to another signal by the Crossbar, the Port register can always read its corresponding Port I/O pin). The exception to this is the execution of the read-modify-write instructions that target a Port Latch register as the destination. The read-modify-write instructions when operating on a Port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a Port SFR. For these instructions, the value of the latch register (not the pin) is read, modified, and written back to the SFR.

Ports 0–3 have a corresponding PnSKIP register which allows its individual Port pins to be assigned to digital functions or skipped by the Crossbar. All Port pins used for analog functions, GPIO, or dedicated digital functions such as the EMIF should have their PnSKIP bit set to 1.

The Port input mode of the I/O pins is defined using the Port Input Mode registers (PnMDIN). Each Port cell can be configured for analog or digital I/O. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is P4, which can only be used for digital I/O.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the PnMDOUT settings.

SFR Definition 19.12. P0: Port 0

Bit	7	6	5	4	3	2	1	0
Name	P0[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0x80; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P0[7:0]	**Port 0 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P0.n Port pin is logic LOW. 1: P0.n Port pin is logic HIGH.

$$multiplier = \frac{20000}{baud\_rate} - 1$$

$$prescaler = \ln\left[\frac{SYSCLK}{(multiplier + 1) \times baud\_rate \times 200}\right] \times \frac{1}{\ln 2} - 1$$

$$divider = \frac{SYSCLK}{(2^{(prescaler + 1)} \times (multiplier + 1) \times baud\_rate)}$$

In all of these equations, the results must be rounded down to the nearest integer.

The following example shows the steps for calculating the baud rate values for a Master node running at 24 MHz and communicating at 19200 bits/sec. First, calculate the multiplier:

$$multiplier = \frac{20000}{19200} - 1 = 0.0417 \cong 0$$

Next, calculate the prescaler:

$$prescaler = \ln\frac{24000000}{(0 + 1) \times 19200 \times 200} \times \frac{1}{\ln 2} - 1 = 1.644 \cong 1$$

Finally, calculate the divider:

$$divider = \frac{24000000}{2^{(1 + 1)} \times (0 + 1) \times 19200} = 312.5 \cong 312$$

These values lead to the following baud rate:

$$baud\_rate = \frac{24000000}{2^{(1 + 1)} \times (0 + 1) \times 312} \cong 19230.77$$

The following code programs the interface in Master mode, using the Enhanced Checksum and enables the interface to operate at 19230 bits/sec using a 24 MHz system clock.

```
LIN0CF   = 0x80;                        // Activate the interface
LIN0CF  |= 0x40;                        // Set the node as a Master

LIN0ADR  = 0x0D;                        // Point to the LIN0MUL register
// Initialize the register (prescaler, multiplier and bit 8 of divider)
LIN0DAT  = ( 0x01 << 6 ) + ( 0x00 << 1 ) + ( ( 0x138 & 0x0100 ) >> 8 );
LIN0ADR   = 0x0C;                       // Point to the LIN0DIV register
LIN0DAT   = (unsigned char)_0x138;      // Initialize LIN0DIV

LIN0ADR   = 0x0B;                       // Point to the LIN0SIZE register
LIN0DAT  |= 0x80;                       // Initialize the checksum as Enhanced

LIN0ADR   = 0x08;                       // Point to LIN0CTRL register
LIN0DAT   = 0x0C;                       // Reset any error and the interrupt
```

Table 20.2 includes the configuration values required for the typical system clocks and baud rates:

20.7. LIN Registers

The following Special Function Registers (SFRs) and indirect registers are available for the LIN controller.

20.7.1. LIN Direct Access SFR Registers Definitions

SFR Definition 20.1. LIN0ADR: LIN0 Indirect Address Register

Bit	7	6	5	4	3	2	1	0
Name	LIN0ADR[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD3; SFR Page = 0x00

Bit	Name	Function
7:0	LIN0ADR[7:0]	**LIN Indirect Address Register Bits.** This register hold an 8-bit address used to indirectly access the LIN0 core registers. Table 20.4 lists the LIN0 core registers and their indirect addresses. Reads and writes to LIN0DAT will target the register indicated by the LIN0ADR bits.

SFR Definition 20.2. LIN0DAT: LIN0 Indirect Data Register

Bit	7	6	5	4	3	2	1	0
Name	LIN0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD2; SFR Page = 0x00

Bit	Name	Function
7:0	LIN0DAT[7:0]	**LIN Indirect Data Register Bits.** When this register is read, it will read the contents of the LIN0 core register pointed to by LIN0ADR. When this register is written, it will write the value to the LIN0 core register pointed to by LIN0ADR.

LIN Register Definition 20.4. LIN0DTn: LIN0 Data Byte n

Bit	7	6	5	4	3	2	1	0
Name	DATAn[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Indirect Address: LIN0DT1 = 0x00, LIN0DT2 = 0x01, LIN0DT3 = 0x02, LIN0DT4 = 0x03, LIN0DT5 = 0x04, LIN0DT6 = 0x05, LIN0DT7 = 0x06, LIN0DT8 = 0x07

Bit	Name	Function
7:0	DATAn[7:0]	**LIN Data Byte n.** Serial Data Byte that is received or transmitted across the LIN interface.

LIN Register Definition 20.7. LIN0ERR: LIN0 Error Register

Bit	7	6	5	4	3	2	1	0
Name				SYNCH	PRTY	TOUT	CHK	BITERR
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x0A

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care
4	SYNCH	**Synchronization Error Bit (slave mode only).** 0: No error with the SYNCH FIELD has been detected. 1: Edges of the SYNCH FIELD are outside of the maximum tolerance.
3	PRTY	**Parity Error Bit (slave mode only).** 0: No parity error has been detected. 1: A parity error has been detected.
2	TOUT	**Timeout Error Bit.** 0: A timeout error has not been detected. 1: A timeout error has been detected. This error is detected whenever one of the following conditions is met: • The master is expecting data from a slave and the slave does not respond. • The slave is expecting data but no data is transmitted on the bus. • A frame is not finished within the maximum frame length. • The application does not set the DTACK bit (LIN0CTRL.4) or STOP bit (LIN0CTRL.7) until the end of the reception of the first byte after the identifier.
1	CHK	**Checksum Error Bit.** 0: Checksum error has not been detected. 1: Checksum error has been detected.
0	BITERR	**Bit Transmission Error Bit.** 0: No error in transmission has been detected. 1: The bit value monitored during transmission is different than the bit value sent.

Table 21.2. Standard CAN Registers and Reset Values

CAN Addr.	Name	SFR Name (High)	SFR Addr.	SFR Name (Low)	SFR Addr.	16-bit SFR	Reset Value
0x50	IF2 Data A 2	CAN0IF2DA2H	0xFB	CAN0IF2DA2L	0xFA	CAN0IF2DA2	0x0000
0x52	IF2 Data B 1	CAN0IF2DB1H	0xFD	CAN0IF2DB1L	0xFC	CAN0IF2DB1	0x0000
0x54	IF2 Data B 2	CAN0IF2DB2H	0xFF	CAN0IF2DB2L	0xFE	CAN0IF2DB2	0x0000
0x80	Transmission Request 1[1]	CAN0TR1H	0xA3	CAN0TR1L	0xA2	CAN0TR1	0x0000
0x82	Transmission Request 2[1]	CAN0TR2H	0xA5	CAN0TR2L	0xA4	CAN0TR2	0x0000
0x90	New Data 1[1]	CAN0ND1H	0xAB	CAN0ND1L	0xAA	CAN0ND1	0x0000
0x92	New Data 2[1]	CAN0ND2H	0xAD	CAN0ND2L	0xAC	CAN0ND2	0x0000
0xA0	Interrupt Pending 1[1]	CAN0IP1H	0xAF	CAN0IP1L	0xAE	CAN0IP1	0x0000
0xA2	Interrupt Pending 2 [1]	CAN0IP2H	0xB3	CAN0IP2L	0xB2	CAN0IP2	0x0000
0xB0	Message Valid 1[1]	CAN0MV1H	0xBB	CAN0MV1L	0xBA	CAN0MV1	0x0000
0xB2	Message Valid 2[1]	CAN0MV2H	0xBD	CAN0MV2L	0xBC	CAN0MV2	0x0000

Notes:
1. Read-only register.
2. Write-enabled by CCE.
3. The reset value of CAN0TST could also be r0000000b, where r signifies the value of the CAN RX pin.
4. Write-enabled by Test.

Setting the EXTHOLD bit extends the minimum setup and hold times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time that the current SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 22.2 shows the minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is above 10 MHz.

Table 22.2. Minimum SDA Setup and Hold Times

EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time
0	T_{low} – 4 system clocks or 1 system clock + s/w delay*	3 system clocks
1	11 system clocks	12 system clocks

***Note:** Setup Time for ACK bit transmissions and the MSB of all data transfers. When using software acknowledgement, the s/w delay occurs between the time SMB0DAT or ACK is written and when SI is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.

With the SMBTOE bit set, Timer 3 should be configured to overflow after 25 ms in order to detect SCL low timeouts (see Section “22.3.4. SCL Low Timeout” on page 220). The SMBus interface will force Timer 3 to reload while SCL is high, and allow Timer 3 to count when SCL is low. The Timer 3 interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBFTE bit. When this bit is set, the bus will be considered free if SDA and SCL remain high for more than 10 SMBus clock source periods (see Figure 22.4).

23.2. Data Format

UART0 has a number of available options for data formatting. Data transfers begin with a start bit (logic low), followed by the data bits (sent LSB-first), a parity or extra bit (if selected), and end with one or two stop bits (logic high). The data length is variable between 5 and 8 bits. A parity bit can be appended to the data, and automatically generated and detected by hardware for even, odd, mark, or space parity. The stop bit length is selectable between 1 and 2 bit times, and a multi-processor communication mode is available for implementing networked UART buses. All of the data formatting options can be configured using the SMOD0 register, shown in SFR Definition 23.2. Figure 23.2 shows the timing for a UART0 transaction without parity or an extra bit enabled. Figure 23.3 shows the timing for a UART0 transaction with parity enabled (PE0 = 1). Figure 23.4 is an example of a UART0 transaction when the extra bit is enabled (XBE0 = 1). Note that the extra bit feature is not available when parity is enabled, and the second stop bit is only an option for data lengths of 6, 7, or 8 bits.

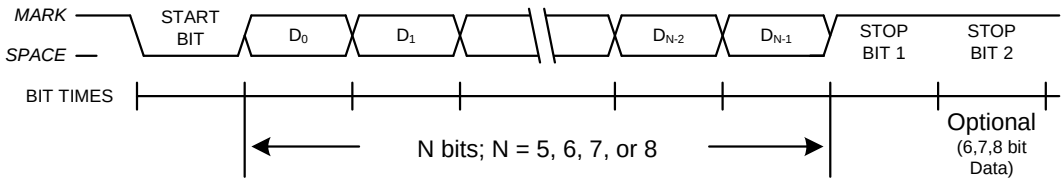

Figure 23.2. UART0 Timing Without Parity or Extra Bit

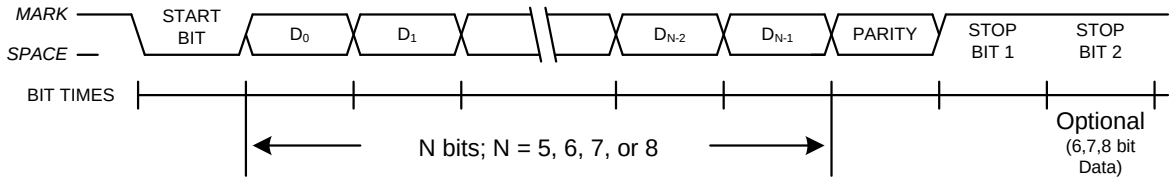

Figure 23.3. UART0 Timing With Parity

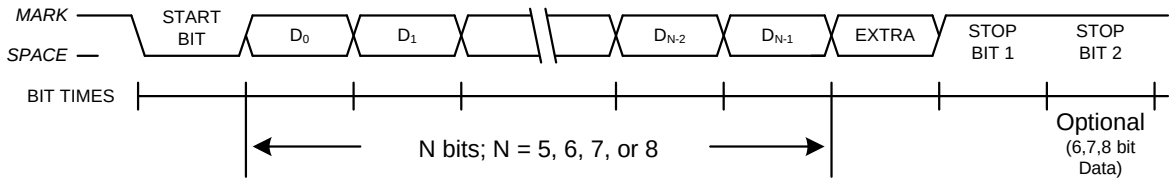

Figure 23.4. UART0 Timing With Extra Bit

SFR Definition 24.1. SPI0CFG: SPI0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Address = 0xA1; SFR Page = 0x00

Bit	Name	Function
7	SPIBSY	**SPI Busy.** This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	**Master Mode Enable.** 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	**SPI0 Clock Phase.** 0: Data centered on first edge of SCK period.* 1: Data centered on second edge of SCK period.*
4	CKPOL	**SPI0 Clock Polarity.** 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	**Slave Selected Flag.** This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	**NSS Instantaneous Pin Input.** This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	**Shift Register Empty (valid in slave mode only).** This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. SRMT = 1 when in Master Mode.
0	RXBMT	**Receive Buffer Empty (valid in slave mode only).** This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. RXBMT = 1 when in Master Mode.

Note: In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 24.1 for timing parameters.

SFR Definition 25.3. TMOD: Timer Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	C/T1	T1M[1:0]		GATE0	C/T0	T0M[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x89; SFR Page = All Pages

Bit	Name	Function
7	GATE1	**Timer 1 Gate Control.** 0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT1}}$ logic level. 1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT1}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 13.7).
6	C/T1	**Counter/Timer 1 Select.** 0: Timer: Timer 1 incremented by clock defined by T1M bit in register CKCON. 1: Counter: Timer 1 incremented by high-to-low transitions on external pin (T1).
5:4	T1M[1:0]	**Timer 1 Mode Select.** These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	**Timer 0 Gate Control.** 0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level. 1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 13.7).
2	C/T0	**Counter/Timer 0 Select.** 0: Timer: Timer 0 incremented by clock defined by T0M bit in register CKCON. 1: Counter: Timer 0 incremented by high-to-low transitions on external pin (T0).
1:0	T0M[1:0]	**Timer 0 Mode Select.** These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

This mode allows software to determine the external oscillator frequency when an RC network or capacitor is used to generate the clock source.

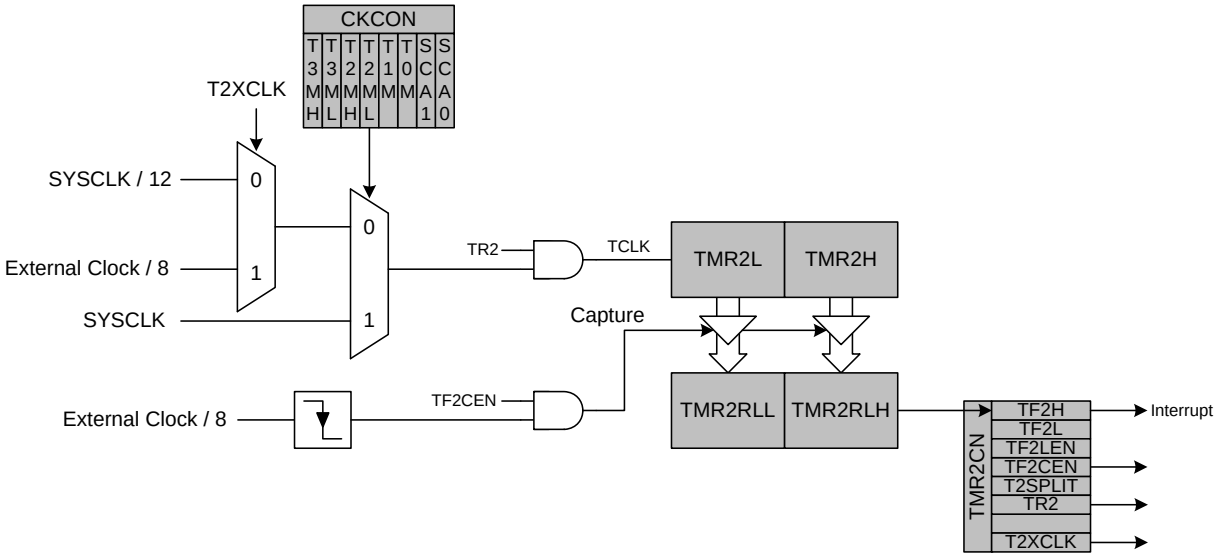

Figure 25.6. Timer 2 External Oscillator Capture Mode Block Diagram

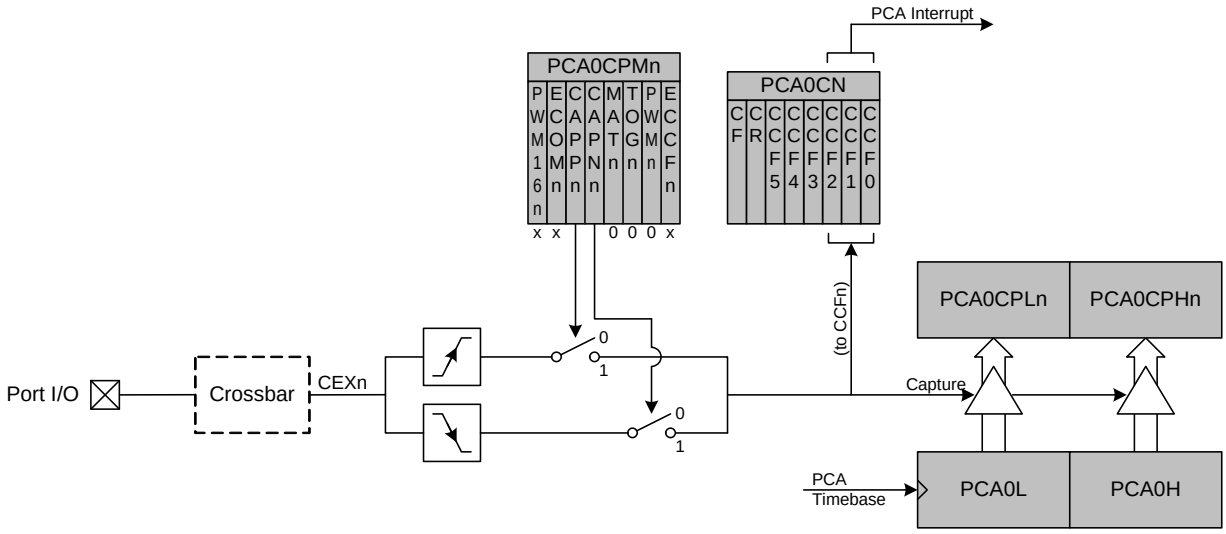

Figure 26.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

26.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

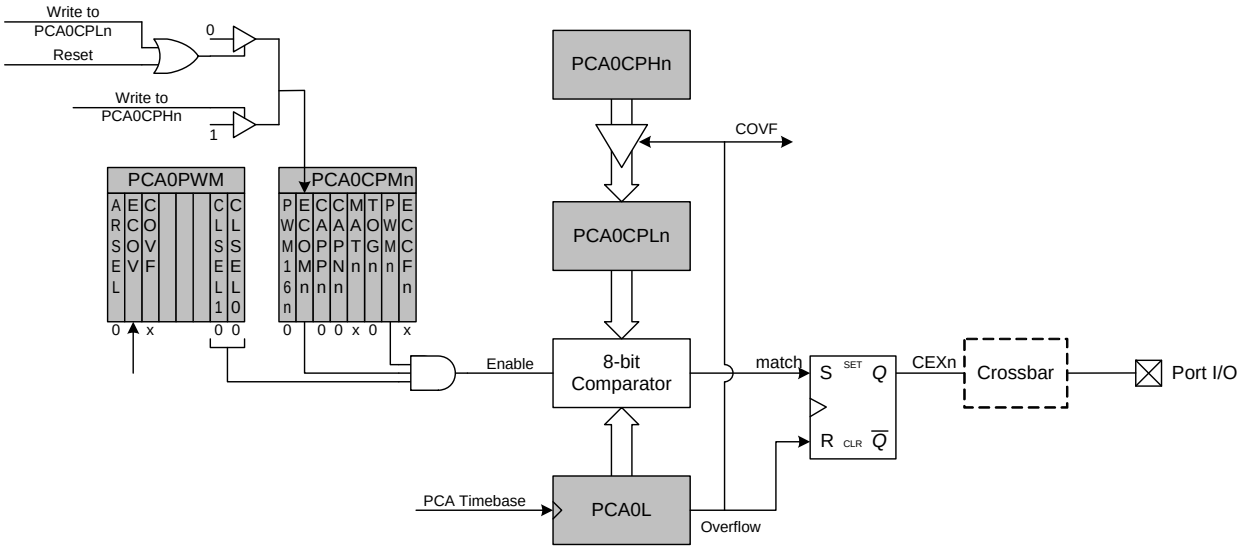

Figure 26.8. PCA 8-Bit PWM Mode Diagram

26.3.5.2. 9/10/11-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 9/10/11-bit PWM mode should be varied by writing to an "Auto-Reload" Register, which is dual-mapped into the PCA0CPHn and PCA0CPLn register locations. The data written to define the duty cycle should be right-justified in the registers. The auto-reload registers are accessed (read or written) when the bit ARSEL in PCA0PWM is set to 1. The capture/compare registers are accessed when ARSEL is set to 0.

When the least-significant N bits of the PCA0 counter match the value in the associated module's capture/compare register (PCA0CPn), the output on CEXn is asserted high. When the counter overflows from the Nth bit, CEXn is asserted low (see Figure 26.9). Upon an overflow from the Nth bit, the COVF flag is set, and the value stored in the module's auto-reload register is loaded into the capture/compare register. The value of N is determined by the CLSEL bits in register PCA0PWM.

The 9, 10 or 11-bit PWM mode is selected by setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to the desired cycle length (other than 8-bits). If the MATn bit is set to 1, the CCFn flag for the module will be set each time a comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 512 (9-bit), 1024 (10-bit) or 2048 (11-bit) PCA clock cycles. The duty cycle for 9/10/11-Bit PWM Mode is given in Equation 26.2, where N is the number of bits in the PWM cycle.

Important Note About PCA0CPHn and PCA0CPLn Registers: When writing a 16-bit value to the PCA0CPn registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(2^N - \text{PCA0CPn})}{2^N}$$

Equation 26.3. 9, 10, and 11-Bit PWM Duty Cycle

A 0% duty cycle may be generated by clearing the ECOMn bit to 0.