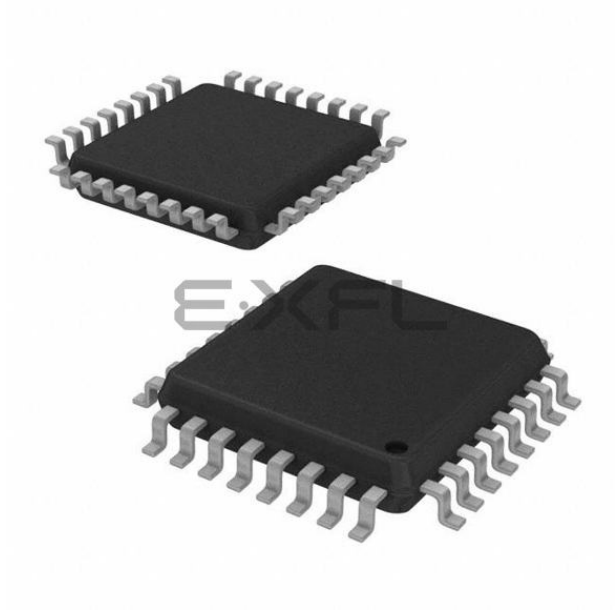

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f562-iqr

Table 5.3. Port I/O DC Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull	V_{IO} – 0.4	—	—	V
	I_{OH} = –10 µA, Port I/O push-pull	V_{IO} – 0.02	—	—	
	I_{OH} = –10 mA, Port I/O push-pull	—	V_{IO} – 0.7	—	
Output Low Voltage	**V_{IO} = 1.8 V:**				
	I_{OL} = 70 µA	—	—	50	
	I_{OL} = 8.5 mA	—	—	750	
	V_{IO} = 2.7 V:				
	I_{OL} = 70 µA	—	—	45	mV
	I_{OL} = 8.5 mA	—	—	550	
	V_{IO} = 5.25 V:				
	I_{OL} = 70 µA	—	—	40	
	I_{OL} = 8.5 mA	—	—	400	
Input High Voltage	V_{REGIN} = 5.25 V	0.7 x VIO	—		V
Input Low Voltage	V_{REGIN} = 2.7 V	—	—	0.3 x VIO	V
Input Leakage Current	Weak Pullup Off	—	—	±2	µA
	Weak Pullup On, V_{IO} = 2.1 V, V_{IN} = 0 V, V_{DD} = 1.8 V	—	7	9	
	Weak Pullup On, V_{IO} = 2.6 V, V_{IN} = 0 V, V_{DD} = 2.6 V	—	17	22	
	Weak Pullup On, V_{IO} = 5.0 V, V_{IN} = 0 V, V_{DD} = 2.6 V	—	49	115	

Table 5.6. Internal High-Frequency Oscillator Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	IFCN = 111b; VDD ≥ VREGMIN[1] IFCN = 111b; VDD < VREGMIN[1]	24 – 0.5% 24 – 1.0%	24[2] 24[2]	24 + 0.5% 24 + 1.0%	MHz
Oscillator Supply Current (from V_{DD})	Internal Oscillator On OSCICN[7:6] = 11b	—	880	1300	µA
Internal Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 1	Temp = 25 °C Temp = 85 °C Temp = 125 °C	—	67 90 130	—	
Wake-up Time From Suspend	OSCICN[7:6] = 00b	—	1	—	µs
Power Supply Sensitivity	Constant Temperature	—	0.11	—	%/V
Temperature Sensitivity[3]	Constant Supply TC_1 TC_2	 — —	 5.0 –0.65	 — —	 ppm/°C ppm/°C[2]

1. VREGMIN is the minimum output of the voltage regulator for its low setting (REG0CN: REG0MD = 0b). See Table 5.8, “Voltage Regulator Electrical Characteristics,” on page 43.
2. This is the average frequency across the operating temperature range
3. Use temperature coefficients TC_1 and TC_2 to calculate the new internal oscillator frequency using the following equation:

$$f(T) = f0 \times (1 + TC_1 \times (T - T0) + TC_2 \times (T - T0)^2)$$

where f0 is the internal oscillator frequency at 25 °C and T0 is 25 °C.

Gain Register Definition 6.1. ADC0GNH: ADC0 Selectable Gain High Byte

Bit	7	6	5	4	3	2	1	0
Name	GAINH[7:0]							
Type	W							
Reset	1	1	1	1	1	1	0	0

Indirect Address = 0x04;

Bit	Name	Function
7:0	GAINH[7:0]	**ADC0 Gain High Byte.** See Section 6.3.1 for details on calculating the value for this register.
Note: This register is accessed indirectly; See Section 6.3.2 for details for writing this register.		

Gain Register Definition 6.2. ADC0GNL: ADC0 Selectable Gain Low Byte

Bit	7	6	5	4	3	2	1	0
Name	GAINL[3:0]				Reserved	Reserved	Reserved	Reserved
Type	W				W	W	W	W
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x07;

Bit	Name	Function
7:4	GAINL[3:0]	**ADC0 Gain Lower 4 Bits.** See Figure 6.3.1 for details for setting this register. This register is only accessed indirectly through the ADC0H and ADC0L register.
3:0	Reserved	Must Write 0000b
Note: This register is accessed indirectly; See Section 6.3.2 for details for writing this register.		

Gain Register Definition 6.3. ADC0GNA: ADC0 Additional Selectable Gain

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GAINADD
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	1

Indirect Address = 0x08;

Bit	Name	Function
7:1	Reserved	Must Write 0000000b.
0	GAINADD	**ADC0 Additional Gain Bit.** Setting this bit add 1/64 (0.016) gain to the gain value in the ADC0GNH and ADC0GNL registers.
Note: This register is accessed indirectly; See Section 6.3.2 for details for writing this register.		

SFR Definition 8.5. CPT0MX: Comparator0 MUX Selection

Bit	7	6	5	4	3	2	1	0
Name	CMX0N[3:0]				CMX0P[3:0]			
Type	R/W				R/W			
Reset	0	1	1	1	0	1	1	1

SFR Address = 0x9C; SFR Page = 0x00

Bit	Name	Function
7:4	CMX0N[3:0]	**Comparator0 Negative Input MUX Selection.** 0000: P0.1 0001: P0.3 0010: P0.5 0011: P0.7 0100: P1.1 0101: P1.3 0110: P1.5 0111: P1.7 1000: P2.1 1001: P2.3 (only available on 40-pin and 32-pin devices) 1010: P2.5 (only available on 40-pin and 32-pin devices) 1011: P2.7 (only available on 40-pin and 32-pin devices) 1100–1111: None
3:0	CMX0P[3:0]	**Comparator0 Positive Input MUX Selection.** 0000: P0.0 0001: P0.2 0010: P0.4 0011: P0.6 0100: P1.0 0101: P1.2 0110: P1.4 0111: P1.6 1000: P2.0 1001: P2.2 (only available on 40-pin and 32-pin devices) 1010: P2.4 (only available on 40-pin and 32-pin devices) 1011: P2.6 (only available on 40-pin and 32-pin devices) 1100–1111: None

12.3. SFR Page Stack Example

The following is an example that shows the operation of the SFR Page Stack during interrupts. In this example, the SFR Control register is left in the default enabled state (i.e., SFRPGEN = 1), and the CIP-51 is executing in-line code that is writing values to SPI Data Register (SFR “SPI0DAT”, located at address 0xA3 on SFR Page 0x00). The device is also using the CAN peripheral (CAN0) and the Programmable Counter Array (PCA0) peripheral to generate a PWM output. The PCA is timing a critical control function in its interrupt service and so its associated ISR that is set to high priority. At this point, the SFR page is set to access the SPI0DAT SFR (SFRPAGE = 0x00). See Figure 12.2.

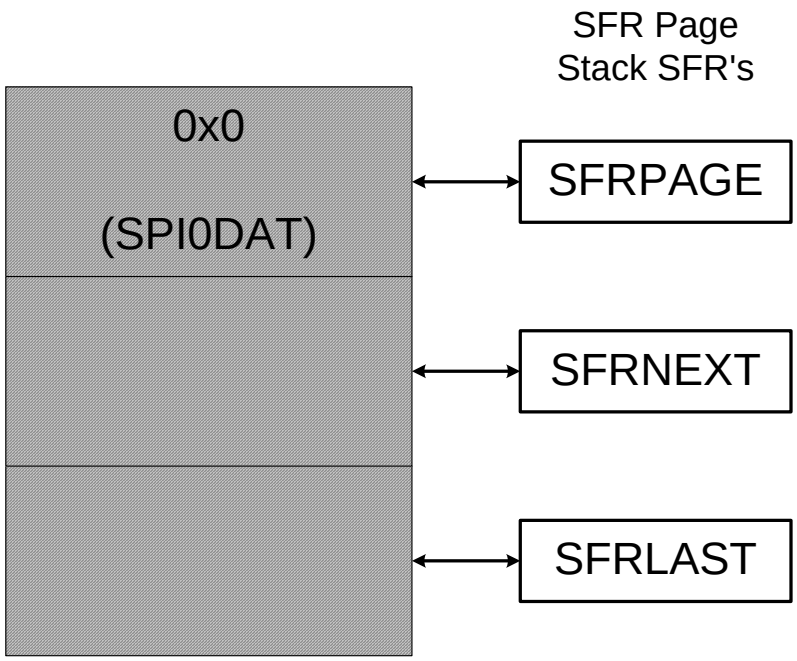

Figure 12.2. SFR Page Stack While Using SFR Page 0x0 To Access SPI0DAT

While in the CAN0 ISR, a PCA interrupt occurs. Recall the PCA interrupt is configured as a high priority interrupt, while the CAN0 interrupt is configured as a *low* priority interrupt. Thus, the CIP-51 will now vector to the high priority PCA ISR. Upon doing so, the CIP-51 will automatically place the SFR page needed to access the PCA's special function registers into the SFRPAGE register, SFR Page 0x00. The value that was in the SFRPAGE register before the PCA interrupt (SFR Page 0x0C for CAN0) is pushed down the stack into SFRNEXT. Likewise, the value that was in the SFRNEXT register before the PCA interrupt (in this case SFR Page 0x00 for SPI0DAT) is pushed down to the SFRLAST register, the "bottom" of the stack. Note that a value stored in SFRLAST (via a previous software write to the SFRLAST register) will be overwritten. See Figure 12.4.

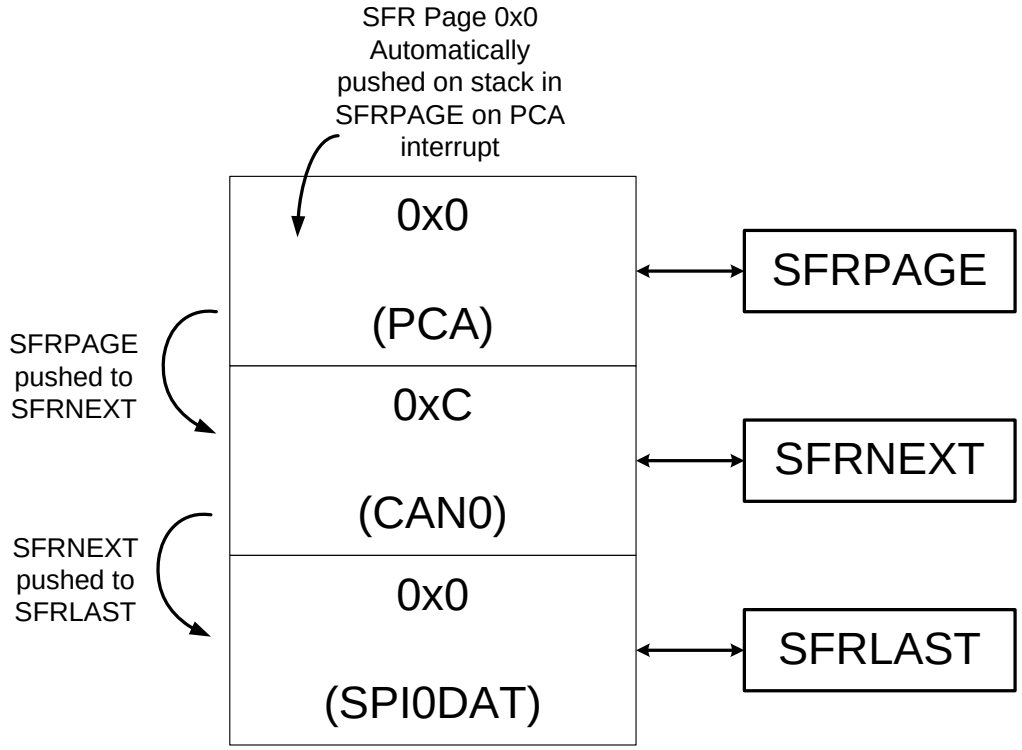

Figure 12.4. SFR Page Stack Upon PCA Interrupt Occurring During a CAN0 ISR

On the execution of the RETI instruction in the CAN0 ISR, the value in SFRPAGE register is overwritten with the contents of SFRNEXT. The CIP-51 may now access the SPI0DAT register as it did prior to the interrupts occurring. See Figure 12.6.

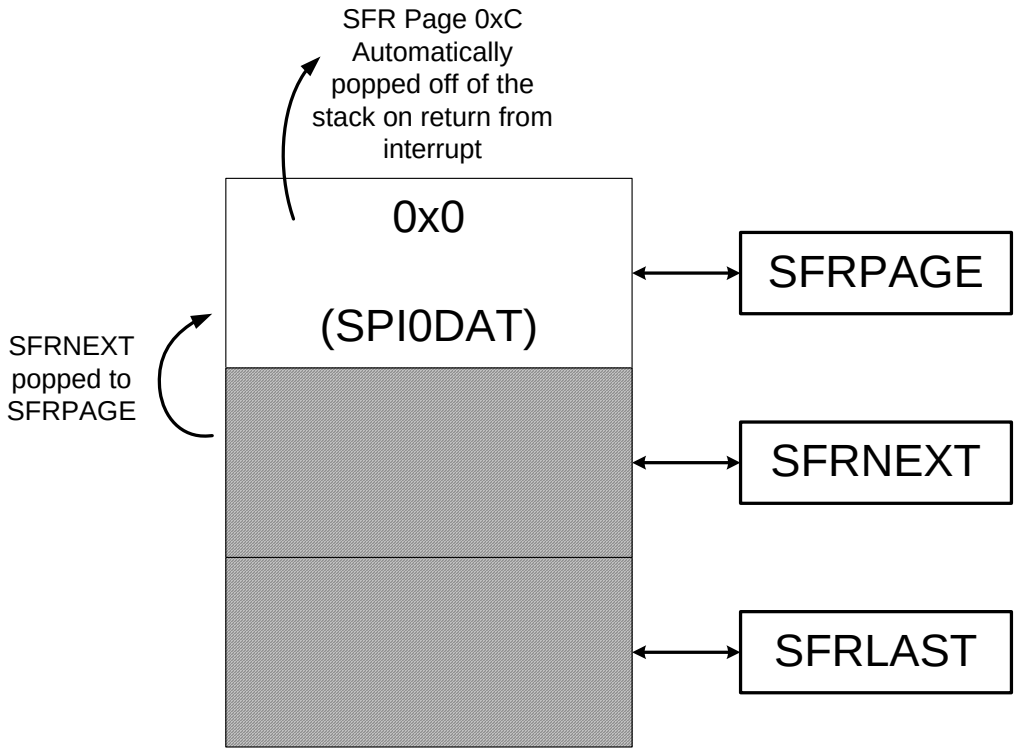

Figure 12.6. SFR Page Stack Upon Return From CAN0 Interrupt

In the example above, all three bytes in the SFR Page Stack are accessible via the SFRPAGE, SFRNEXT, and SFRLAST special function registers. If the stack is altered while servicing an interrupt, it is possible to return to a different SFR Page upon interrupt exit than selected prior to the interrupt call. Direct access to the SFR Page stack can be useful to enable real-time operating systems to control and manage context switching between multiple tasks.

Push operations on the SFR Page Stack only occur on interrupt service, and pop operations only occur on interrupt exit (execution on the RETI instruction). The automatic switching of the SFRPAGE and operation of the SFR Page Stack as described above can be disabled in software by clearing the SFR Automatic Page Enable Bit (SFRPGEN) in the SFR Page Control Register (SFR0CN). See SFR Definition 12.1.

SFR Definition 13.4. EIP1: Extended Interrupt Priority 1

Bit	7	6	5	4	3	2	1	0
Name	PLIN0	PT3	PCP1	PCP0	PPCA0	PADC0	PWADC0	PSMB0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF6; SFR Page = 0x00 and 0x0F

Bit	Name	Function
7	PLIN0	**LIN0 Interrupt Priority Control.** This bit sets the priority of the LIN0 interrupt. 0: LIN0 interrupts set to low priority level. 1: LIN0 interrupts set to high priority level.
6	PT3	**Timer 3 Interrupt Priority Control.** This bit sets the priority of the Timer 3 interrupt. 0: Timer 3 interrupts set to low priority level. 1: Timer 3 interrupts set to high priority level.
5	PCP1	**Comparator0 (CP1) Interrupt Priority Control.** This bit sets the priority of the CP1 interrupt. 0: CP1 interrupt set to low priority level. 1: CP1 interrupt set to high priority level.
4	PCP0	**Comparator0 (CP0) Interrupt Priority Control.** This bit sets the priority of the CP0 interrupt. 0: CP0 interrupt set to low priority level. 1: CP0 interrupt set to high priority level.
3	PPCA0	**Programmable Counter Array (PCA0) Interrupt Priority Control.** This bit sets the priority of the PCA0 interrupt. 0: PCA0 interrupt set to low priority level. 1: PCA0 interrupt set to high priority level.
2	PADC0	**ADC0 Conversion Complete Interrupt Priority Control.** This bit sets the priority of the ADC0 Conversion Complete interrupt. 0: ADC0 Conversion Complete interrupt set to low priority level. 1: ADC0 Conversion Complete interrupt set to high priority level.
1	PWADC0	**ADC0 Window Comparator Interrupt Priority Control.** This bit sets the priority of the ADC0 Window interrupt. 0: ADC0 Window interrupt set to low priority level. 1: ADC0 Window interrupt set to high priority level.
0	PSMB0	**SMBus (SMB0) Interrupt Priority Control.** This bit sets the priority of the SMB0 interrupt. 0: SMB0 interrupt set to low priority level. 1: SMB0 interrupt set to high priority level.

15.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the controller core to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout of 100 µs.

15.3. Suspend Mode

Setting the SUSPEND bit (OSCICN.5) causes the hardware to halt the CPU and the high-frequency internal oscillator, and go into Suspend mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. Most digital peripherals are not active in Suspend mode. The exception to this is the Port Match feature.

Suspend mode can be terminated by three types of events, a port match (described in Section “19.5. Port Match” on page 179), a Comparator low output (if enabled), or a device reset event. When Suspend mode is terminated, the device will continue execution on the instruction following the one that set the SUSPEND bit. If the wake event was configured to generate an interrupt, the interrupt will be serviced upon waking the device. If Suspend mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: Before entering suspend mode, firmware must set the ZTCEN bit in REF0CN (SFR Definition 7.1).

18.4.1. External Crystal Example

If a crystal or ceramic resonator is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 18.1, Option 1. The External Oscillator Frequency Control value (XFCN) should be chosen from the Crystal column of the table in SFR Definition 18.6 (OSCXCN register). For example, an 11.0592 MHz crystal requires an XFCN setting of 111b and a 32.768 kHz Watch Crystal requires an XFCN setting of 001b. After an external 32.768 kHz oscillator is stabilized, the XFCN setting can be switched to 000 to save power. It is recommended to enable the missing clock detector before switching the system clock to any external oscillator source.

When the crystal oscillator is first enabled, the oscillator amplitude detection circuit requires a settling time to achieve proper bias. Introducing a delay of 1 ms between enabling the oscillator and checking the XTLVLD bit will prevent a premature switch to the external oscillator as the system clock. Switching to the external oscillator before the crystal oscillator has stabilized can result in unpredictable behavior. The recommended procedure is:

1. Force XTAL1 and XTAL2 to a high state. This involves enabling the Crossbar and writing 1 to the port pins associated with XTAL1 and XTAL2.
2. Configure XTAL1 and XTAL2 as analog inputs using.
3. Enable the external oscillator.
4. Wait at least 1 ms.
5. Poll for XTLVLD => 1.
6. Enable the Missing Clock Detector.
7. Switch the system clock to the external oscillator.

Important Note on External Crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The desired load capacitance depends upon the crystal and the manufacturer. Refer to the crystal data sheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 18.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 18.3.

SFR Definition 19.6. P1MASK: Port 1 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P1MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF4; SFR Page = 0x00

Bit	Name	Function
7:0	P1MASK[7:0]	**Port 1 Mask Value.** Selects P1 pins to be compared to the corresponding bits in P1MAT. 0: P1.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P1.n pin logic value is compared to P1MAT.n.

SFR Definition 19.7. P1MAT: Port 1 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P1MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF3; SFR Page = 0x00

Bit	Name	Function
7:0	P1MAT[7:0]	**Port 1 Match Value.** Match comparison value used on Port 1 for bits in P1MAT which are set to 1. 0: P1.n pin logic value is compared with logic LOW. 1: P1.n pin logic value is compared with logic HIGH.

Table 20.2. Manual Baud Rate Parameters Examples

	Baud (bits/sec)														
	20 K			19.2 K			9.6 K			4.8 K			1 K		
SYSCLK (MHz)	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.
25	0	1	312	0	1	325	1	1	325	3	1	325	19	1	312
24.5	0	1	306	0	1	319	1	1	319	3	1	319	19	1	306
24	0	1	300	0	1	312	1	1	312	3	1	312	19	1	300
22.1184	0	1	276	0	1	288	1	1	288	3	1	288	19	1	276
16	0	1	200	0	1	208	1	1	208	3	1	208	19	1	200
12.25	0	0	306	0	0	319	1	0	319	3	0	319	19	0	306
12	0	0	300	0	0	312	1	0	312	3	0	312	19	0	300
11.0592	0	0	276	0	0	288	1	0	288	3	0	288	19	0	276
8	0	0	200	0	0	208	1	0	208	3	0	208	19	0	200

20.2.4. Baud Rate Calculations—Automatic Mode

If the LIN controller is configured for slave mode, only the prescaler and divider need to be calculated:

$$\text{prescaler} = \ln\left[\frac{\text{SYSCLK}}{4000000}\right] \times \frac{1}{\ln 2} - 1$$

$$\text{divider} = \frac{\text{SYSCLK}}{2^{(\text{prescaler}+1)} \times 20000}$$

The following example calculates the values of these variables for a 24 MHz system clock:

$$\text{prescaler} = \ln\left[\frac{24000000}{4000000}\right] \times \frac{1}{\ln 2} - 1 = 1.585 \cong 1$$

$$\text{divider} = \frac{24000000}{2^{(1+1)} \times 20000} = 300$$

Table 20.3 presents some typical values of system clock and baud rate along with their factors.

SFR Definition 23.3. SBUF0: Serial (UART0) Port Data Buffer

Bit	7	6	5	4	3	2	1	0
Name	SBUF0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x99; SFR Page = 0x00

Bit	Name	Function
7:0	SBUF0[7:0]	**Serial Data Buffer Bits 7–0 (MSB–LSB).** This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF0, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF0 initiates the transmission. A read of SBUF0 returns the contents of the receive latch.

SFR Definition 23.4. SBCON0: UART0 Baud Rate Generator Control

Bit	7	6	5	4	3	2	1	0
Name	Reserved	SB0RUN	Reserved	Reserved	Reserved	Reserved	SB0PS[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAB; SFR Page = 0x0F

Bit	Name	Function
7	Reserved	Read = 0b; Must Write 0b;
6	SB0RUN	**Baud Rate Generator Enable.** 0: Baud Rate Generator disabled. UART0 will not function. 1: Baud Rate Generator enabled.
5:2	Reserved	Read = 0000b; Must Write = 0000b;
1:0	SB0PS[1:0]	**Baud Rate Prescaler Select.** 00: Prescaler = 12. 01: Prescaler = 4. 10: Prescaler = 48. 11: Prescaler = 1.

SFR Definition 25.9. TMR2RLL: Timer 2 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCA; SFR Page = 0x00

Bit	Name	Function
7:0	TMR2RLL[7:0]	**Timer 2 Reload Register Low Byte.** TMR2RLL holds the low byte of the reload value for Timer 2.

SFR Definition 25.10. TMR2RLH: Timer 2 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCB; SFR Page = 0x00

Bit	Name	Function
7:0	TMR2RLH[7:0]	**Timer 2 Reload Register High Byte.** TMR2RLH holds the high byte of the reload value for Timer 2.

T3MH	T3XCLK	TMR3H Clock Source
0	0	SYSCLK/12
0	1	External Clock/8
1	X	SYSCLK

T3ML	T3XCLK	TMR3L Clock Source
0	0	SYSCLK/12
0	1	External Clock/8
1	X	SYSCLK

The TF3H bit is set when TMR3H overflows from 0xFF to 0x00; the TF3L bit is set when TMR3L overflows from 0xFF to 0x00. When Timer 3 interrupts are enabled, an interrupt is generated each time TMR3H overflows. If Timer 3 interrupts are enabled and TF3LEN (TMR3CN.5) is set, an interrupt is generated each time either TMR3L or TMR3H overflows. When TF3LEN is enabled, software must check the TF3H and TF3L flags to determine the source of the Timer 3 interrupt. The TF3H and TF3L interrupt flags are not cleared by hardware and must be manually cleared by software.

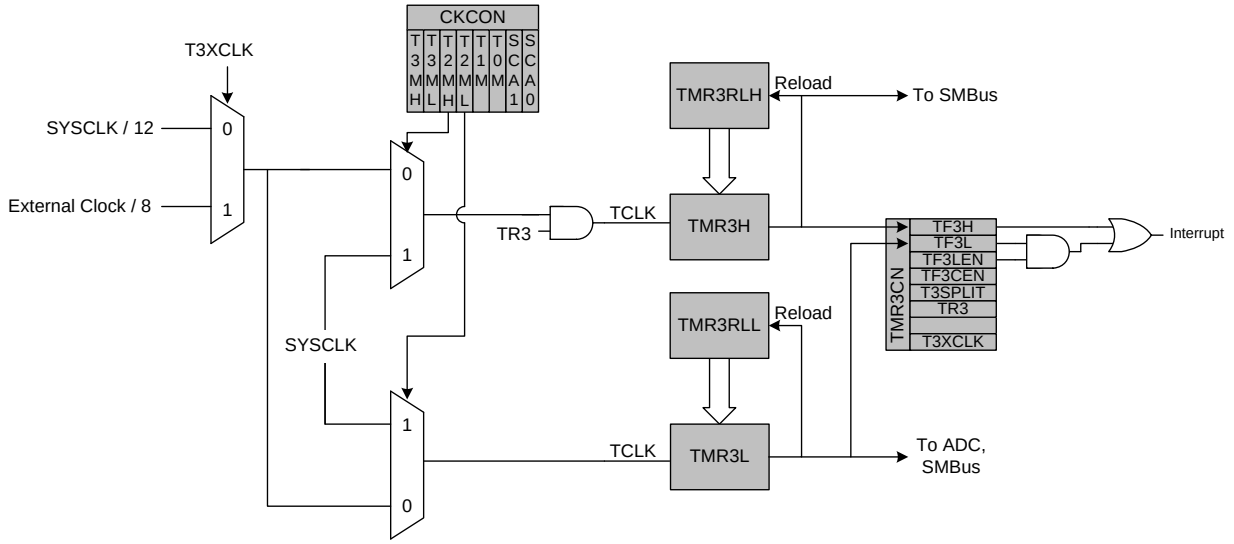

Figure 25.8. Timer 3 8-Bit Mode Block Diagram

25.3.3. External Oscillator Capture Mode

Capture Mode allows the external oscillator to be measured against the system clock. Timer 3 can be clocked from the system clock, or the system clock divided by 12, depending on the T3ML (CKCON.6), and T3XCLK bits. When a capture event is generated, the contents of Timer 3 (TMR3H:TMR3L) are loaded into the Timer 3 reload registers (TMR3RLH:TMR3RLL) and the TF3H flag is set. A capture event is generated by the falling edge of the clock source being measured, which is the external oscillator/8. By recording the difference between two successive timer capture values, the external oscillator frequency can be determined with respect to the Timer 3 clock. The Timer 3 clock should be much faster than the capture clock to achieve an accurate reading. Timer 3 should be in 16-bit auto-reload mode when using Capture Mode.

If the SYSCLK is 24 MHz and the difference between two successive captures is 5861, then the external clock frequency is as follows:

24 MHz/(5861/8) = 0.032754 MHz or 32.754 kHz

This mode allows software to determine the external oscillator frequency when an RC network or capacitor is used to generate the clock source.

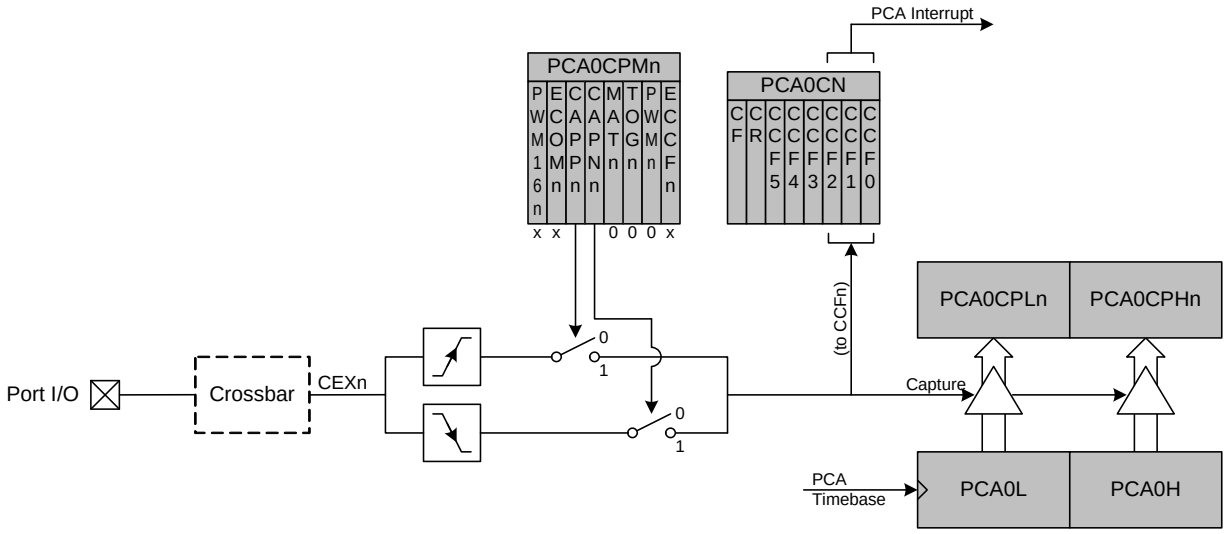

Figure 26.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

26.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

27. C2 Interface

C8051F55x/56x/57x devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

27.1. C2 Interface Registers

The following describes the C2 registers necessary to perform Flash programming through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 27.1. C2ADD: C2 Address

Bit	7	6	5	4	3	2	1	0
Name	C2ADD[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function	
7:0	C2ADD[7:0]	**C2 Address.** The C2ADD register is accessed via the C2 interface to select the target Data register for C2 Data Read and Data Write commands.	
		Address	**Description**
		0x00	Selects the Device ID register for Data Read instructions
		0x01	Selects the Revision ID register for Data Read instructions
		0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions
		0xB4	Selects the C2 Flash Programming Data register for Data Read/Write instructions