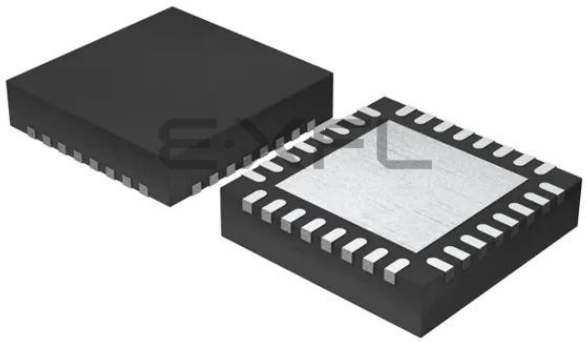

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), CANbus, LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f564-im

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F55x/56x/57x

Name	Pin 40-pin packages	Pin 32-pin packages	Pin 24-pin packages	Type	Description
VDD	4	4	3		Digital Supply Voltage. Must be connected.
GND	6	6	4		Digital Ground. Must be connected.
VDDA	5	5	—		Analog Supply Voltage. Must be connected.
GNDA	7	7	5		Analog Ground. Must be connected.
VREGIN	3	3	2		Voltage Regulator Input
VIO	2	2	1		Port I/O Supply Voltage. Must be connected.
$\overline{\text{RST}}$/ C2CK	10	10	8	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} Monitor. Clock signal for the C2 Debug Interface.
P4.0/ C2D	9	—	—	D I/O or A In D I/O	Port 4.0. See SFR Definition 19.28. Bi-directional data signal for the C2 Debug Interface.
P3.0/ C2D		9	—	D I/O or A In D I/O	Port 3.0. See SFR Definition 19.24. Bi-directional data signal for the C2 Debug Interface.
P2.1/ C2D		—	7	D I/O or A In D I/O	Port 2.1. See SFR Definition 19.20. Bi-directional data signal for the C2 Debug Interface.
P0.0	8	8	6	D I/O or A In	Port 0.0. See SFR Definition 19.12.
P0.1	1	1	24	D I/O or A In	Port 0.1
P0.2	40	32	23	D I/O or A In	Port 0.2
P0.3	39	31	22	D I/O or A In	Port 0.3
P0.4	38	30	21	D I/O or A In	Port 0.4
P0.5	37	29	20	D I/O or A In	Port 0.5
P0.6	36	28	19	D I/O or A In	Port 0.6
P0.7	35	27	18	D I/O or A In	Port 0.7

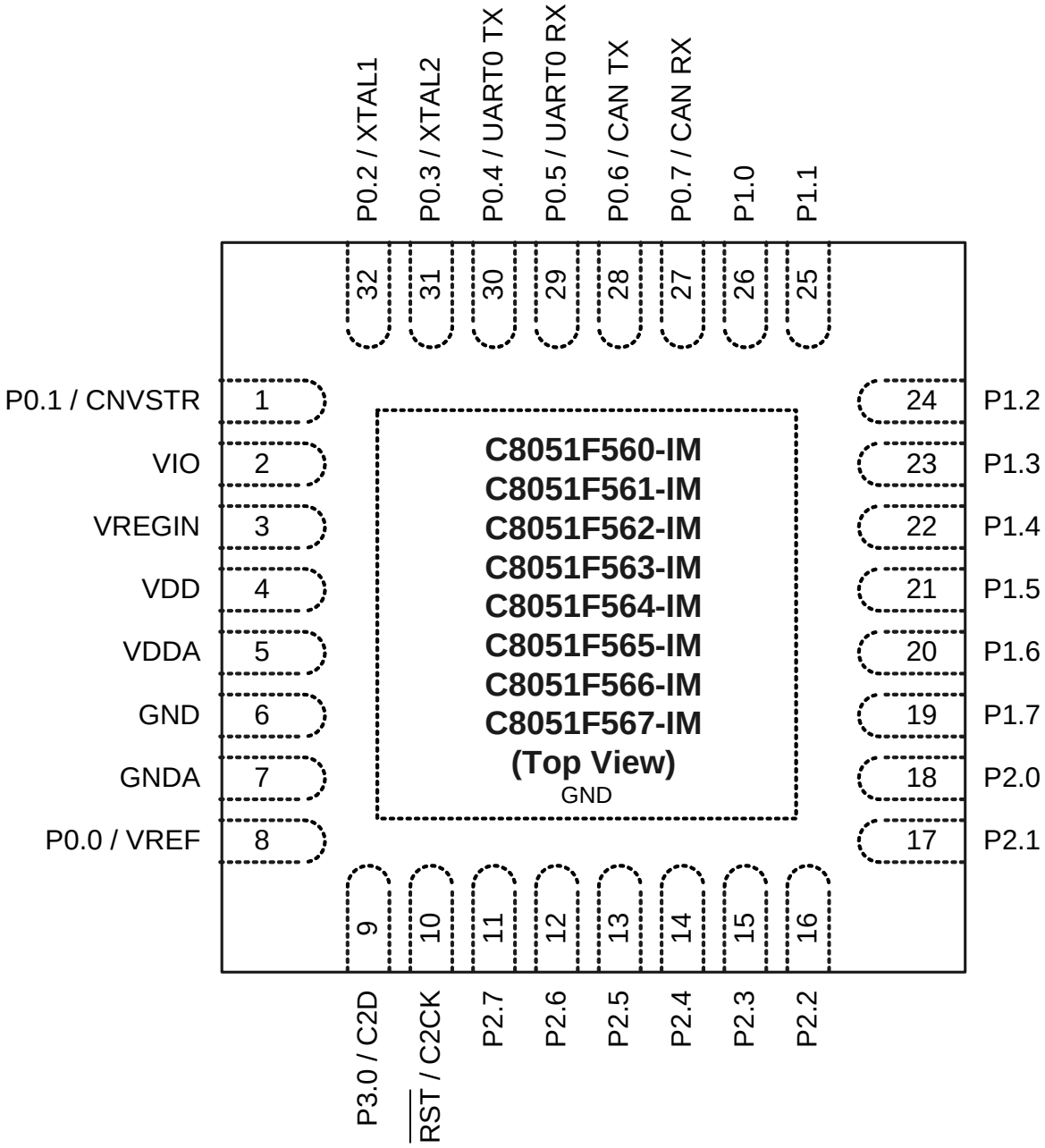

Figure 3.3. QFN-32 Pinout Diagram (Top View)

Table 5.4. Reset Electrical Characteristics

–40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{RST}$ Output Low Voltage	VIO = 5 V; IOL = 70 µA	—	—	40	mV
$\overline{RST}$ Input High Voltage		0.7 x V_{IO}	—	—	
$\overline{RST}$ Input Low Voltage		—	—	0.3 x V_{IO}	
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 0.0 V, VIO = 5 V	—	49	115	µA
V_{DD} RST Threshold ($V_{RST-LOW}$)		1.65	1.75	1.80	V
V_{DD} RST Threshold ($V_{RST-HIGH}$)		2.25	2.30	2.45	V
V_{REGIN} Ramp Time for Power On	V_{REGIN} Ramp 0–1.8 V	—	—	1	ms
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation V_{DD} = 2.1 V V_{DD} = 2.5 V	 200 200	 340 250	 600 600	µs
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	155	175	µs
Minimum $\overline{RST}$ Low Time to Generate a System Reset		6	—	—	µs
V_{DD} Monitor Turn-on Time		—	60	100	µs
V_{DD} Monitor Supply Current		—	1	2	µA

Table 5.5. Flash Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F550-3, ‘F560-3, ‘F568-9, and ‘F570-1	32768[1]			Bytes
	C8051F554-7, ‘F564-7, and ‘F572-5	16384			
Endurance		20 k	150 k	—	Erase/Write
Retention	125 °C	10	—	—	Years
Erase Cycle Time	25 MHz System Clock	28	30	45	ms
Write Cycle Time	25 MHz System Clock	79	84	125	µs
V_{DD}	Write/Erase operations	$V_{RST-HIGH}$[2]	—	—	V
Temperature during Programming Operations	–I Devices –A Devices	0 –40	— —	+125 +125	°C

1. On the 32 kB Flash devices, 1024 bytes at addresses 0x7C00 to 0x7FFF are reserved.
2. See Table 5.4 for the $V_{RST-HIGH}$ specification.

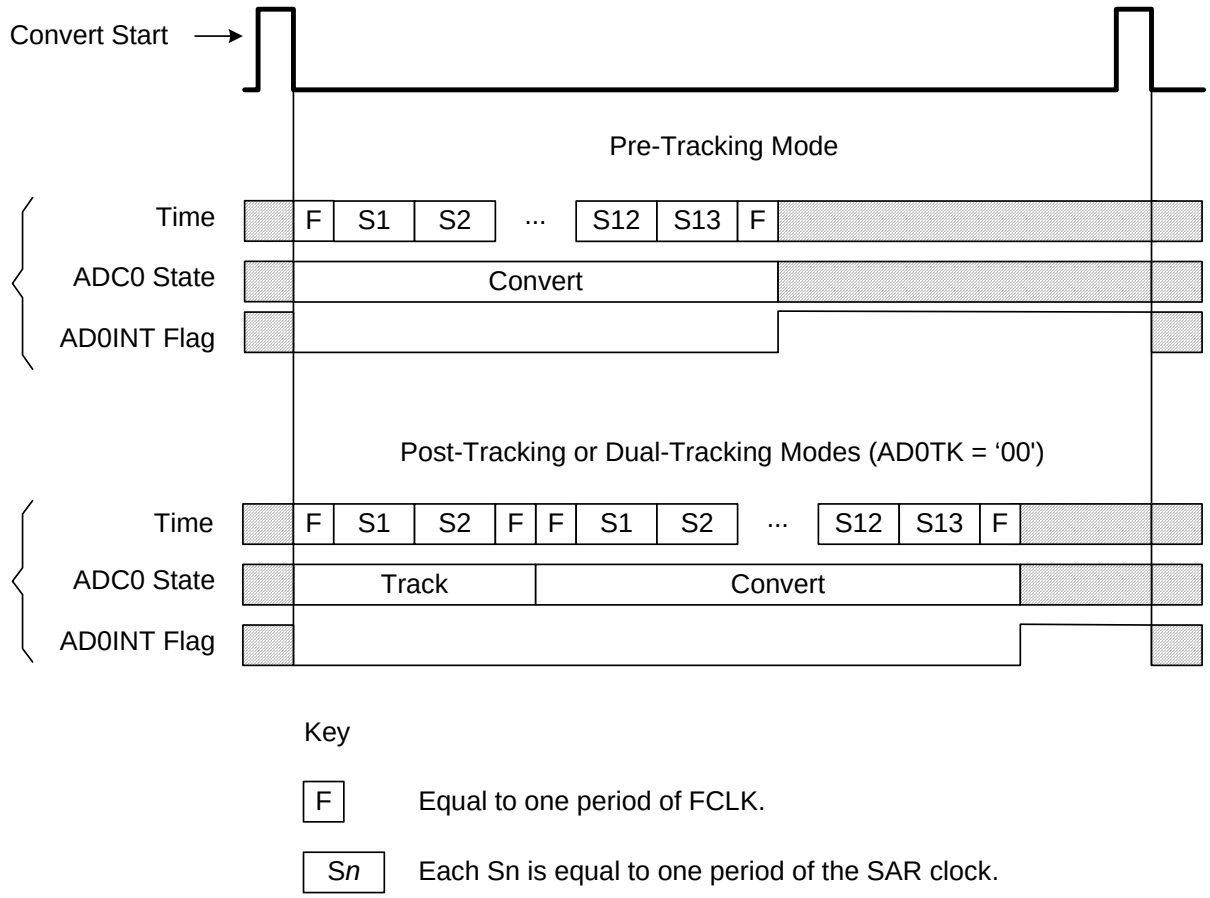

Figure 6.3. 12-Bit ADC Tracking Mode Example

6.1.4. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a very low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a very low power state, accumulates 1, 4, 8, or 16 samples using an internal Burst Mode clock (approximately 25 MHz), then re-enters a very low power state. Since the Burst Mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a very low power state within a single system clock cycle, even if the system clock is slow (e.g., 32.768 kHz), or suspended.

Burst Mode is enabled by setting BURSTEN to logic 1. When in Burst Mode, AD0EN controls the ADC0 idle power state (i.e. the state ADC0 enters when not tracking or performing conversions). If AD0EN is set to logic 0, ADC0 is powered down after each burst. If AD0EN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If ADC0 is powered down, it will automatically power up and wait the programmable Power-up Time controlled by the AD0PWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 6.4 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

Important Note: When Burst Mode is enabled, only Post-Tracking and Dual-Tracking modes can be used.

When Burst Mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When Burst Mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (AD0INT) will be set after “repeat count” conversions have

Gain Register Definition 6.1. ADC0GNH: ADC0 Selectable Gain High Byte

Bit	7	6	5	4	3	2	1	0
Name	GAINH[7:0]							
Type	W							
Reset	1	1	1	1	1	1	0	0

Indirect Address = 0x04;

Bit	Name	Function
7:0	GAINH[7:0]	**ADC0 Gain High Byte.** See Section 6.3.1 for details on calculating the value for this register.
Note: This register is accessed indirectly; See Section 6.3.2 for details for writing this register.		

Gain Register Definition 6.2. ADC0GNL: ADC0 Selectable Gain Low Byte

Bit	7	6	5	4	3	2	1	0
Name	GAINL[3:0]				Reserved	Reserved	Reserved	Reserved
Type	W				W	W	W	W
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x07;

Bit	Name	Function
7:4	GAINL[3:0]	**ADC0 Gain Lower 4 Bits.** See Figure 6.3.1 for details for setting this register. This register is only accessed indirectly through the ADC0H and ADC0L register.
3:0	Reserved	Must Write 0000b
Note: This register is accessed indirectly; See Section 6.3.2 for details for writing this register.		

6.5. ADC0 Analog Multiplexer

ADC0 includes an analog multiplexer to enable multiple analog input sources. Any of the following may be selected as an input: P0.0–P3.7, the on-chip temperature sensor, the core power supply (V_{DD}), or ground (GND). **ADC0 is single-ended and all signals measured are with respect to GND.** The ADC0 input channels are selected using the ADC0MX register as described in SFR Definition 6.13.

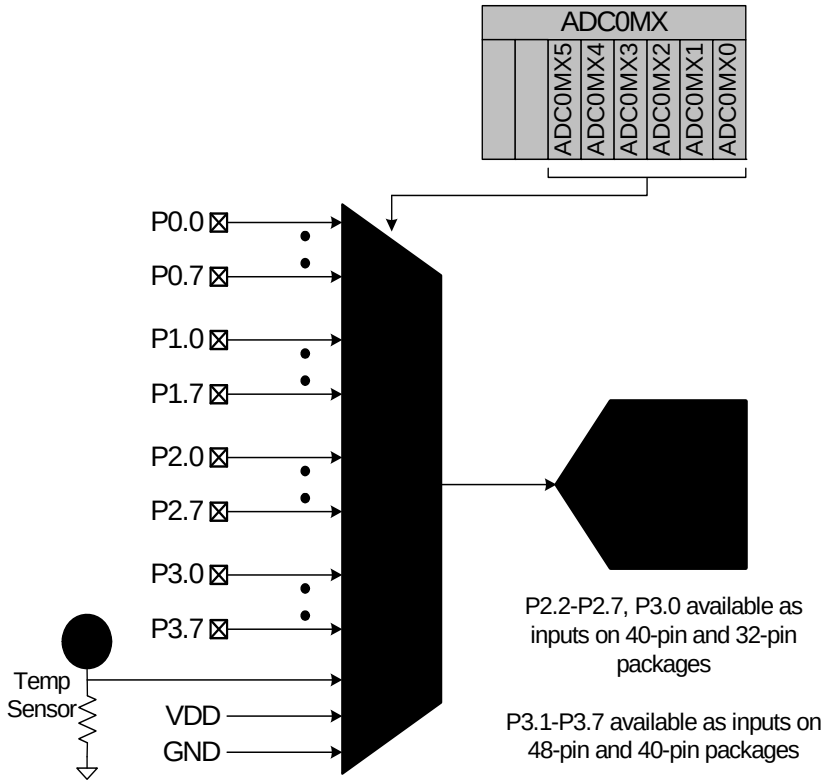

Figure 6.8. ADC0 Multiplexer Block Diagram

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN. To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP. See Section “19. Port Input/Output” on page 169 for more Port I/O configuration details.

On the execution of the RETI instruction in the CAN0 ISR, the value in SFRPAGE register is overwritten with the contents of SFRNEXT. The CIP-51 may now access the SPI0DAT register as it did prior to the interrupts occurring. See Figure 12.6.

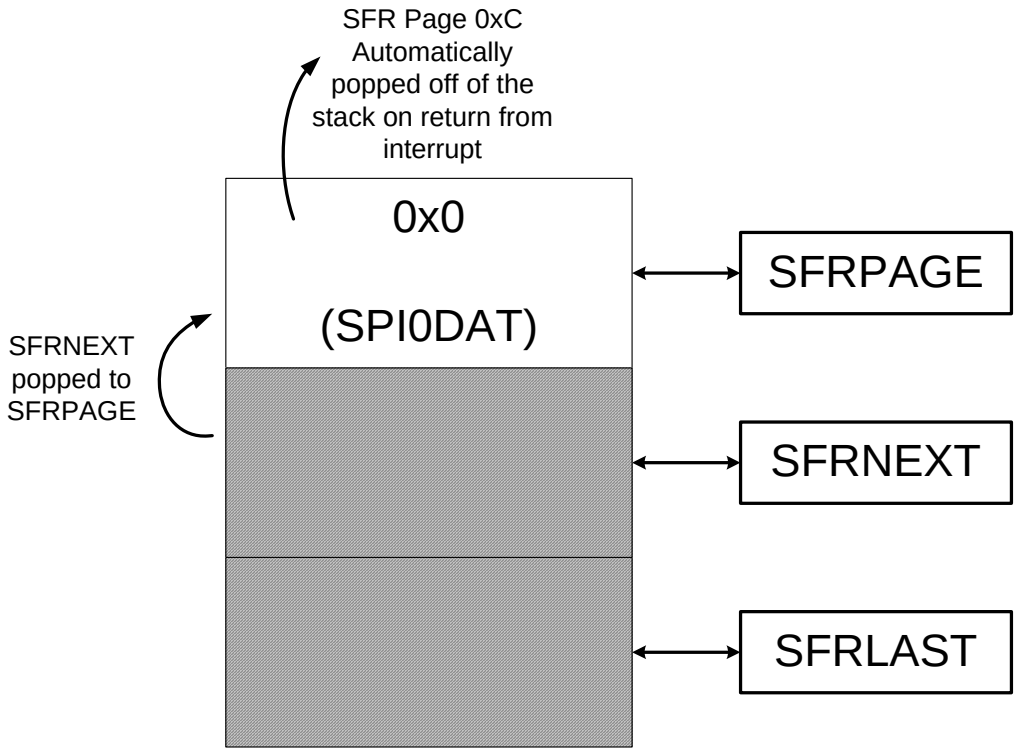

Figure 12.6. SFR Page Stack Upon Return From CAN0 Interrupt

In the example above, all three bytes in the SFR Page Stack are accessible via the SFRPAGE, SFRNEXT, and SFRLAST special function registers. If the stack is altered while servicing an interrupt, it is possible to return to a different SFR Page upon interrupt exit than selected prior to the interrupt call. Direct access to the SFR Page stack can be useful to enable real-time operating systems to control and manage context switching between multiple tasks.

Push operations on the SFR Page Stack only occur on interrupt service, and pop operations only occur on interrupt exit (execution on the RETI instruction). The automatic switching of the SFRPAGE and operation of the SFR Page Stack as described above can be disabled in software by clearing the SFR Automatic Page Enable Bit (SFRPGEN) in the SFR Page Control Register (SFR0CN). See SFR Definition 12.1.

Table 12.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
IT01CF	0xE4	INT0/INT1 Configuration	123
LIN0ADR	0xD3	LIN0 Address	200
LIN0CF	0xC9	LIN0 Configuration	200
LIN0DAT	0xD2	LIN0 Data	201
OSCICN	0xA1	Internal Oscillator Control	160
OSCICRS	0xA2	Internal Oscillator Coarse Control	161
OSCIFIN	0x9E	Internal Oscillator Fine Calibration	161
OSCXCN	0x9F	External Oscillator Control	165
P0	0x80	Port 0 Latch	183
P0MASK	0xF2	Port 0 Mask Configuration	179
P0MAT	0xF1	Port 0 Match Configuration	179
P0MDIN	0xF1	Port 0 Input Mode Configuration	184
P0MDOUT	0xA4	Port 0 Output Mode Configuration	184
P0SKIP	0xD4	Port 0 Skip	185
P1	0x90	Port 1 Latch	185
P1MASK	0xF4	Port 1 Mask Configuration	180
P1MAT	0xF3	Port 1 Match Configuration	180
P1MDIN	0xF2	Port 1 Input Mode Configuration	186
P1MDOUT	0xA5	Port 1 Output Mode Configuration	186
P1SKIP	0xD5	Port 1 Skip	187
P2	0xA0	Port 2 Latch	187
P2MASK	0xB2	Port 2 Mask Configuration	181
P2MAT	0xB1	Port 2 Match Configuration	181
P2MDIN	0xF3	Port 2 Input Mode Configuration	188
P2MDOUT	0xA6	Port 2 Output Mode Configuration	188
P2SKIP	0xD6	Port 2 Skip	189
P3	0xB0	Port 3 Latch	189
P3MASK	0xAF	Port 3 Mask Configuration	182
P3MAT	0xAE	Port 3 Match Configuration	182
P3MDIN	0xF4	Port 3 Input Mode Configuration	190
P3MDOUT	0xAE	Port 3 Output Mode Configuration	190
P3SKIP	0xD7	Port 3 Skip	191
P4	0xB5	Port 4 Latch	191
P4MDOUT	0xAF	Port 4 Output Mode Configuration	192
PCA0CN	0xD8	PCA Control	294
PCA0CPH0	0xFC	PCA Capture 0 High	299

SFR Definition 14.1. PSCTL: Program Store R/W Control

Bit	7	6	5	4	3	2	1	0
Name							PSEE	PSWE
Type	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8F; SFR Page = 0x00

Bit	Name	Function
7:2	Unused	Read = 000000b, Write = don't care.
1	PSEE	**Program Store Erase Enable.** Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter. 0: Flash program memory erasure disabled. 1: Flash program memory erasure enabled.
0	PSWE	**Program Store Write Enable.** Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data. 0: Writes to Flash program memory disabled. 1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

18.2. Programmable Internal Oscillator

All C8051F55x/56x/57x devices include a programmable internal high-frequency oscillator that defaults as the system clock after a system reset. The internal oscillator period can be adjusted via the OSCICRS and OSCIFIN registers defined in SFR Definition 18.3 and SFR Definition 18.4. On C8051F55x/56x/57x devices, OSCICRS and OSCIFIN are factory calibrated to obtain a 24 MHz base frequency. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, 8, 16, 32, 64, or 128, as defined by the IFCN bits in register OSCICN. The divide value defaults to 128 following a reset.

18.2.1. Internal Oscillator Suspend Mode

When software writes a logic 1 to SUSPEND (OSCICN.5), the internal oscillator is suspended. If the system clock is derived from the internal oscillator, the input clock to the peripheral or CIP-51 will be stopped until one of the following events occur:

- Port 0 Match Event.
- Port 1 Match Event.
- Port 2 Match Event.
- Port 3 Match Event.
- Comparator 0 enabled and output is logic 0.

When one of the oscillator awakening events occur, the internal oscillator, CIP-51, and affected peripherals resume normal operation, regardless of whether the event also causes an interrupt. The CPU resumes execution at the instruction following the write to SUSPEND.

Note: Before entering suspend mode, firmware must set the ZTCEN bit in REF0CN (SFR Definition 7.1).

SFR Definition 19.3. XBR2: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	WEAKPUD	XBARE	Reserved					LIN0E
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC7; SFR Page = 0x0F

Bit	Name	Function
7	WEAKPUD	**Port I/O Weak Pullup Disable.** 0: Weak Pullups enabled (except for Ports whose I/O are configured for analog mode). 1: Weak Pullups disabled.
6	XBARE	**Crossbar Enable.** 0: Crossbar disabled. 1: Crossbar enabled.
5:1	Reserved	Always Write to 00000b.
0	LIN0E	**LIN I/O Output Enable.** 0: LIN I/O unavailable at Port pin. 1: LIN_TX, LIN_RX routed to Port pins.

SFR Definition 19.8. P2MASK: Port 2 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P2MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB2; SFR Page = 0x00

Bit	Name	Function
7:0	P2MASK[7:0]	**Port 2 Mask Value.** Selects P2 pins to be compared to the corresponding bits in P2MAT. 0: P2.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P2.n pin logic value is compared to P2MAT.n.
Note: P2.2–P2.7 are available on 40-pin and 32-pin packages.		

SFR Definition 19.9. P2MAT: Port 2 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P2MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xB1; SFR Page = 0x00

Bit	Name	Function
7:0	P2MAT[7:0]	**Port 2 Match Value.** Match comparison value used on Port 2 for bits in P2MAT which are set to 1. 0: P2.n pin logic value is compared with logic LOW. 1: P2.n pin logic value is compared with logic HIGH.
Note: P2.2–P2.7 are available on 40-pin and 32-pin packages.		

SFR Definition 19.25. P3MDIN: Port 3 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P3MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF4; SFR Page = 0x0F

Bit	Name	Function
7:0	P3MDIN[7:0]	**Analog Configuration Bits for P3.7–P3.0 (respectively).** Port pins configured for analog mode have their weak pull-up and digital receiver disabled. For analog mode, the pin also needs to be configured for open-drain mode in the P3MDOUT register. 0: Corresponding P3.n pin is configured for analog mode. 1: Corresponding P3.n pin is not configured for analog mode.
Note: P3.0 is available on 40-pin and 32-pin packages. P3.1-P3.7 are available on 40-pin packages		

SFR Definition 19.26. P3MDOUT: Port 3 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P3MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAE; SFR Page = 0x0F

Bit	Name	Function
7:0	P3MDOUT[7:0]	**Output Configuration Bits for P3.7–P3.0 (respectively).** These bits are ignored if the corresponding bit in register P3MDIN is logic 0. 0: Corresponding P3.n Output is open-drain. 1: Corresponding P3.n Output is push-pull.
Note: P3.0 is available on 40-pin and 32-pin packages. P3.1-P3.7 are available on 40-pin packages		

21.2.4. CAN Register Assignment

The standard Bosch CAN registers are mapped to SFR space as shown below and their full definitions are available in the CAN User's Guide. The name shown in the Name column matches what is provided in the CAN User's Guide. One additional SFR which is not a standard Bosch CAN register, CAN0CFG, is provided to configure the CAN clock. All CAN registers are located on SFR Page 0x0C.

Table 21.2. Standard CAN Registers and Reset Values

CAN Addr.	Name	SFR Name (High)	SFR Addr.	SFR Name (Low)	SFR Addr.	16-bit SFR	Reset Value
0x00	CAN Control Register	—	—	CAN0CN	0xC0	—	0x01
0x02	Status Register	—	—	CAN0STAT	0x94	—	0x00
0x04	Error Counter[1]	CAN0ERRH	0x97	CAN0ERRL	0x96	CAN0ERR	0x0000
0x06	Bit Timing Register[2]	CAN0BTH	0x9B	CAN0BTL	0x9A	CAN0BT	0x2301
0x08	Interrupt Register[1]	CAN0IIDH	0x9D	CAN0IIDL	0x9C	CAN0IID	0x0000
0x0A	Test Register	—	—	CAN0TST	0x9E	—	0x00[3,4]
0x0C	BRP Extension Register[2]	—	—	CAN0BRPE	0xA1	—	0x00
0x10	IF1 Command Request	CAN0IF1CRH	0xBF	CAN0IF1CRL	0xBE	CAN0IF1CR	0x0001
0x12	IF1 Command Mask	CAN0IF1CMH	0xC3	CAN0IF1CML	0xC2	CAN0IF1CM	0x0000
0x14	IF1 Mask 1	CAN0IF1M1H	0xC5	CAN0IF1M1L	0xC4	CAN0IF1M1	0xFFFF
0x16	IF1 Mask 2	CAN0IF1M2H	0xC7	CAN0IF1M2L	0xC6	CAN0IF1M2	0xFFFF
0x18	IF1 Arbitration 1	CAN0IF1A1H	0xCB	CAN0IF1A1L	0xCA	CAN0IF1A1	0x0000
0x1A	IF1 Arbitration 2	CAN0IF1A2H	0xCD	CAN0IF1A2L	0xCC	CAN0IF1A2	0x0000
0x1C	IF1 Message Control	CAN0IF1MCH	0xD3	CAN0IF1MCL	0xD2	CAN0IF1MC	0x0000
0x1E	IF1 Data A 1	CAN0IF1DA1H	0xD5	CAN0IF1DA1L	0xD4	CAN0IF1DA1	0x0000
0x20	IF1 Data A 2	CAN0IF1DA2H	0xD7	CAN0IF1DA2L	0xD6	CAN0IF1DA2	0x0000
0x22	IF1 Data B 1	CAN0IF1DB1H	0xDB	CAN0IF1DB1L	0xDA	CAN0IF1DB1	0x0000
0x24	IF1 Data B 2	CAN0IF1DB2H	0xDD	CAN0IF1DB2L	0xDC	CAN0IF1DB2	0x0000
0x40	IF2 Command Request	CAN0IF2CRH	0xDF	CAN0IF2CRL	0xDE	CAN0IF2CR	0x0001
0x42	IF2 Command Mask	CAN0IF2CMH	0xE3	CAN0IF2CML	0xE2	CAN0IF2CM	0x0000
0x44	IF2 Mask 1	CAN0IF2M1H	0xEB	CAN0IF2M1L	0xEA	CAN0IF2M1	0xFFFF
0x46	IF2 Mask 2	CAN0IF2M2H	0xED	CAN0IF2M2L	0xEC	CAN0IF2M2	0xFFFF
0x48	IF2 Arbitration 1	CAN0IF2A1H	0xEF	CAN0IF2A1L	0xEE	CAN0IF2A1	0x0000
0x4A	IF2 Arbitration 2	CAN0IF2A2H	0xF3	CAN0IF2A2L	0xF2	CAN0IF2A2	0x0000
0x4C	IF2 Message Control	CAN0IF2MCH	0xCF	CAN0IF2MCL	0xCE	CAN0IF2MC	0x0000
0x4E	IF2 Data A 1	CAN0IF2DA1H	0xF7	CAN0IF2DA1L	0xF6	CAN0IF2DA1	0x0000

Notes:
1. Read-only register.
2. Write-enabled by CCE.
3. The reset value of CAN0TST could also be r0000000b, where r signifies the value of the CAN RX pin.
4. Write-enabled by Test.

23.2. Data Format

UART0 has a number of available options for data formatting. Data transfers begin with a start bit (logic low), followed by the data bits (sent LSB-first), a parity or extra bit (if selected), and end with one or two stop bits (logic high). The data length is variable between 5 and 8 bits. A parity bit can be appended to the data, and automatically generated and detected by hardware for even, odd, mark, or space parity. The stop bit length is selectable between 1 and 2 bit times, and a multi-processor communication mode is available for implementing networked UART buses. All of the data formatting options can be configured using the SMOD0 register, shown in SFR Definition 23.2. Figure 23.2 shows the timing for a UART0 transaction without parity or an extra bit enabled. Figure 23.3 shows the timing for a UART0 transaction with parity enabled (PE0 = 1). Figure 23.4 is an example of a UART0 transaction when the extra bit is enabled (XBE0 = 1). Note that the extra bit feature is not available when parity is enabled, and the second stop bit is only an option for data lengths of 6, 7, or 8 bits.

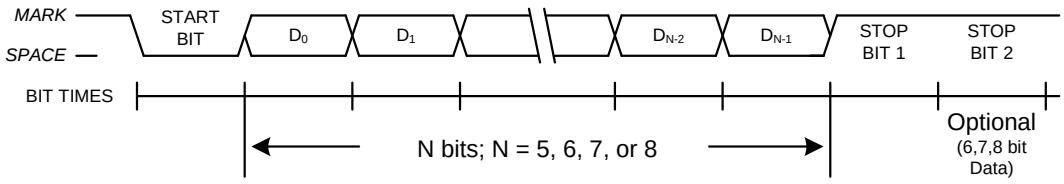

Figure 23.2. UART0 Timing Without Parity or Extra Bit

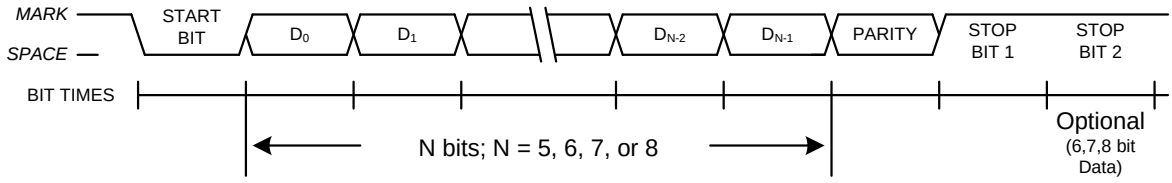

Figure 23.3. UART0 Timing With Parity

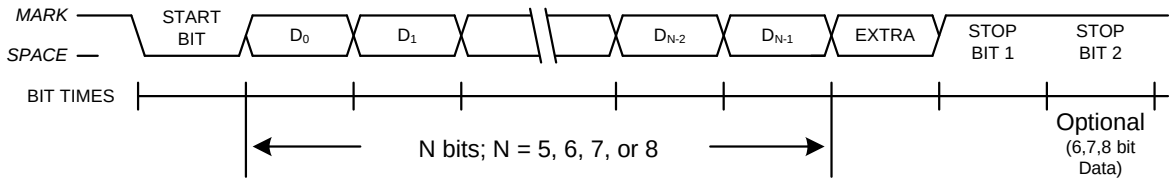

Figure 23.4. UART0 Timing With Extra Bit

the RI0 flag will be set. Note: when MCE0 = 1, RI0 will only be set if the extra bit was equal to 1. Data can be read from the receive FIFO by reading the SBUF0 register. The SBUF0 register represents the oldest byte in the FIFO. After SBUF0 is read, the next byte in the FIFO is immediately loaded into SBUF0, and space is made available in the FIFO for another incoming byte. If enabled, an interrupt will occur when RI0 is set. RI0 can only be cleared to '0' by software when there is no more information in the FIFO. The recommended procedure to empty the FIFO contents is as follows:

1. Clear RI0 to 0.
2. Read SBUF0.
3. Check RI0, and repeat at step 1 if RI0 is set to 1.

If the extra bit function is enabled (XBE0 = 1) and the parity function is disabled (PE0 = 0), the extra bit for the oldest byte in the FIFO can be read from the RBX0 bit (SCON0.2). If the extra bit function is not enabled, the value of the stop bit for the oldest FIFO byte will be presented in RBX0. When the parity function is enabled (PE0 = 1), hardware will check the received parity bit against the selected parity type (selected with S0PT[1:0]) when receiving data. If a byte with parity error is received, the PERR0 flag will be set to 1. This flag must be cleared by software. Note: when parity is enabled, the extra bit function is not available.

Note: The UART Receive FIFO pointer can be corrupted if the UART receives a byte and firmware reads a byte from the FIFO at the same time. When this occurs, firmware will lose the received byte and the FIFO receive overrun flag (OVR0) will also be set to 1. Systems using the UART Receive FIFO should ensure that the FIFO isn't accessed by hardware and firmware at the same time. In other words, firmware should ensure to read the FIFO before the next byte is received.

24. Enhanced Serial Peripheral Interface (SPI0)

The Enhanced Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

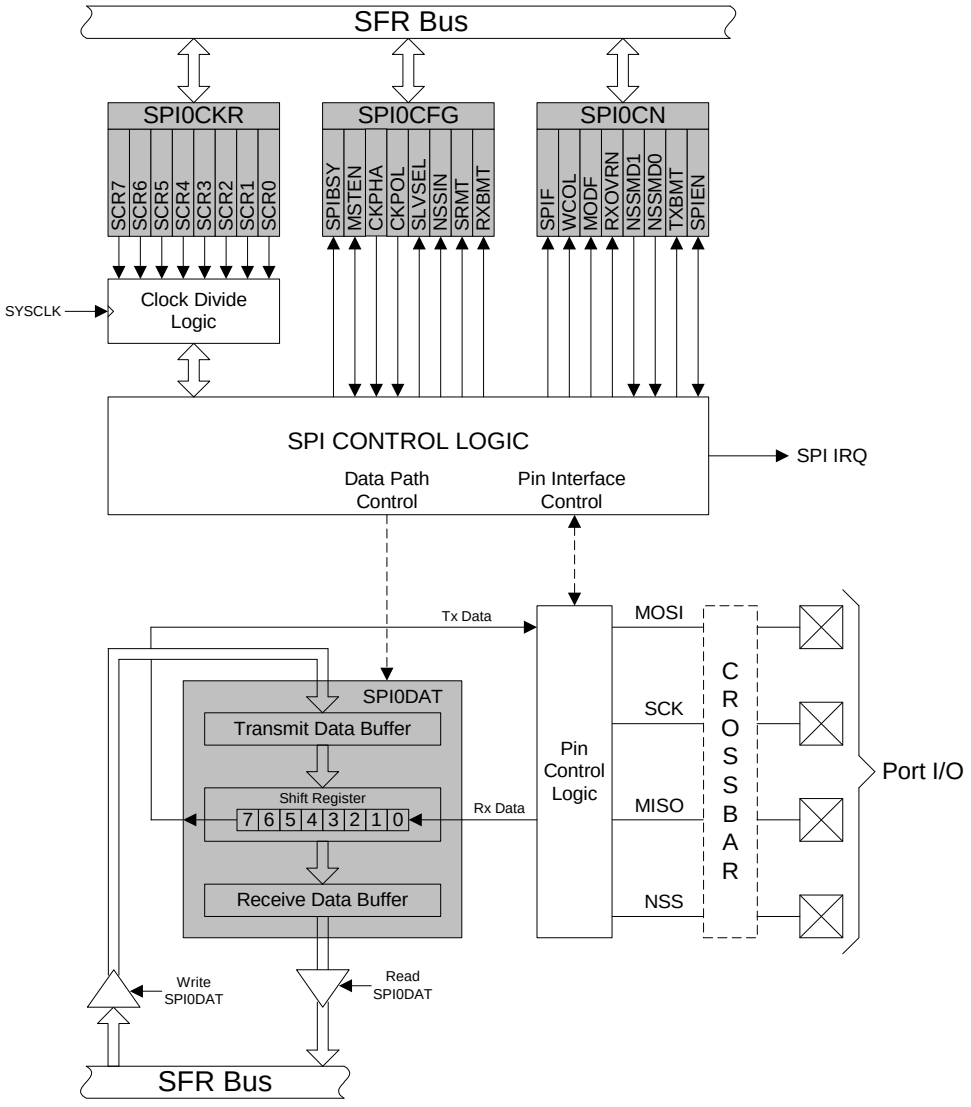

Figure 24.1. SPI Block Diagram

26.5. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of the PCA.

SFR Definition 26.1. PCA0CN: PCA Control

Bit	7	6	5	4	3	2	1	0
Name	CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD8; Bit-Addressable; SFR Page = 0x00

Bit	Name	Function
7	CF	**PCA Counter/Timer Overflow Flag.** Set by hardware when the PCA Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
6	CR	**PCA Counter/Timer Run Control.** This bit enables/disables the PCA Counter/Timer. 0: PCA Counter/Timer disabled. 1: PCA Counter/Timer enabled.
5	CCF5	**PCA Module 5 Capture/Compare Flag.** This bit is set by hardware when a match or capture occurs. When the CCF5 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
4	CCF4	**PCA Module 4 Capture/Compare Flag.** This bit is set by hardware when a match or capture occurs. When the CCF4 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
3	CCF3	**PCA Module 3 Capture/Compare Flag.** This bit is set by hardware when a match or capture occurs. When the CCF3 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
2	CCF2	**PCA Module 2 Capture/Compare Flag.** This bit is set by hardware when a match or capture occurs. When the CCF2 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
1	CCF1	**PCA Module 1 Capture/Compare Flag.** This bit is set by hardware when a match or capture occurs. When the CCF1 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.
0	CCF0	**PCA Module 0 Capture/Compare Flag.** This bit is set by hardware when a match or capture occurs. When the CCF0 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

SFR Definition 26.5. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF9; SFR Page = 0x00

Bit	Name	Function
7:0	PCA0[7:0]	**PCA Counter/Timer Low Byte.** The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.

Note: When the WDTE bit is set to 1, the PCA0L register cannot be modified by software. To change the contents of the PCA0L register, the Watchdog Timer must first be disabled.

SFR Definition 26.6. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFA; SFR Page = 0x00

Bit	Name	Function
7:0	PCA0[15:8]	**PCA Counter/Timer High Byte.** The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a “snapshot” register, whose contents are updated only when the contents of PCA0L are read (see Section 26.1).

Note: When the WDTE bit is set to 1, the PCA0H register cannot be modified by software. To change the contents of the PCA0H register, the Watchdog Timer must first be disabled.

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 1.0

- Updated “2. Ordering Information” to include -A (Automotive) devices and automotive qualification information.
- Updated Figure 4.8 on page 35.
- Updated supply current related specifications throughout “5. Electrical Characteristics” .
- Updated SFR Definition 7.1 to change VREF high setting to 2.20 V from 2.25 V.
- Updated Figure 8.1 to indicate that Comparators are powered from V_{IO} and not V_{DDA}.
- Updated the Gain Table in “6.3.1. Calculating the Gain Value” to fix the ADC0GNH Value in the last row.
- Updated Table 10.1 with correct timing for all branch instructions, MOVC, and CPL A.
- Updated “14.2. Non-volatile Data Storage” to clarify behavior of 8-bit MOVX instructions and when writing/erasing Flash.
- Updated SFR Definition 14.3 (FLSCL) to include FLEWT bit definition. This bit must be set before writing or erasing Flash. Also updated Table 5.5 to reflect new Flash Write and Erase timing.
- Updated “16.7. Flash Error Reset” with an additional cause of a Flash Error reset.
- Updated “19.1.3. Interfacing Port I/O in a Multi-Voltage System” to remove note regarding interfacing to voltages above VIO.
- Updated “22. SMBus” to remove all hardware ACK features, including SMB0ADM and SMB0ADR SFRs.
- Updated SFR Definition 23.1 (SCON0) to correct SFR Page to 0x00 from All Pages.
- All items from the C8051F55x-F56x-57x Errata dated November 5th, 2009 are incorporated into this data sheet.

Revision 1.0 to Revision 1.1

- Updated “1. System Overview” with a voltage range specification for the internal oscillator.
- Updated Table 5.6, “Internal High-Frequency Oscillator Electrical Characteristics,” on page 42 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated “5. Electrical Characteristics” to remove the internal oscillator curve across temperature diagram.
- Updated Figure 6.4 on Page 51 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 7.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Fixed incorrect cross references in “8. Comparators” .
- Updated SFR Definition 9.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Update “15.3. Suspend Mode” with note regarding ZTCEN.
- Added Port 2 Event and Port 3 Events to wake-up sources in “18.2.1. Internal Oscillator Suspend Mode”
- Updated “20. Local Interconnect Network (LIN0)” with a voltage range specification for the internal oscillator.
- Updated LIN Register Definitions 20.9 and 20.10 with correct reset values.
- Updated “21. Controller Area Network (CAN0)” with a voltage range specification for the internal oscillator.
- Updated C2 Register Definitions 27.2 and 27.3 with correct C2 and SFR Addresses.