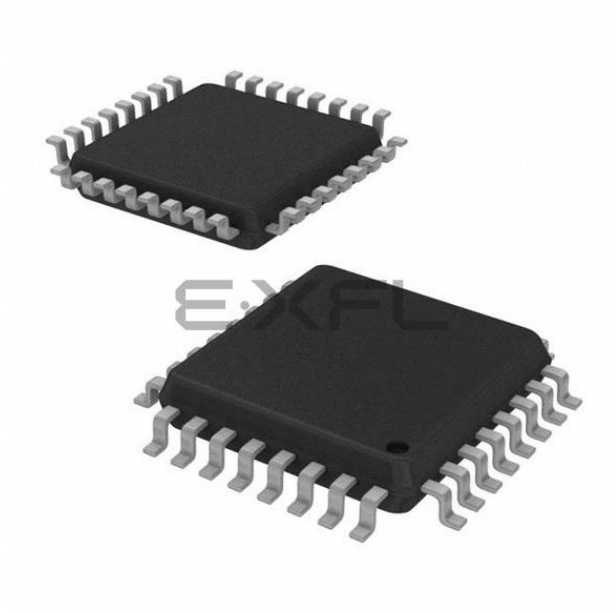

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), CANbus, LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f564-iqr

1. System Overview

C8051F55x/56x/57x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Controller Area Network (CAN 2.0B) Controller with 32 message objects, each with its own indentifier mask (C8051F550/1/4/5, ‘F560/1/4/5/8/9, and ‘F572/3)
- LIN 2.1 peripheral (fully backwards compatible, master and slave modes) (C8051F550/2/4/6, ‘F560/2/4/6/8, and ‘F570/2/4)
- True 12-bit 200 ksps 32-channel single-ended ADC with analog multiplexer
- Precision programmable 24 MHz internal oscillator that is within ±0.5% across the temperature range and for VDD voltages greater than or equal to the on-chip voltage regulator minimum output at the low setting. The oscillator is within ±1.0% for VDD voltages below this minimum output setting.
- On-chip Clock Multiplier to reach up to 50 MHz
- 32 kB (C8051F550-3, ‘F560-3, ‘F568-9, and ‘F570-1) or 16 kB (C8051F554-7, ‘F564-7, and ‘F572-5) of on-chip Flash memory
- 2304 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- External Data Memory Interface (C8051F568-9 and ‘F570-5) with 64 kB address space
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Voltage Regulator
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- 33, 25, or 18 Port I/O (5 V push-pull)

With on-chip Voltage Regulator, Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F55x/56x/57x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

The devices are specified for 1.8 V to 5.25 V operation over the automotive temperature range (–40 to +125 °C). The C8051F568-9 and ‘F570-5 are available in 40-pin QFN packages, the C8051F560-7 devices are available in 32-pin QFP and QFN packages, and the C8051F550-7 are available in 24-pin QFN packages. All package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1, Figure 1.2, and Figure 1.3.

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F55x/56x/57x

Name	Pin 40-pin packages	Pin 32-pin packages	Pin 24-pin packages	Type	Description
VDD	4	4	3		Digital Supply Voltage. Must be connected.
GND	6	6	4		Digital Ground. Must be connected.
VDDA	5	5	—		Analog Supply Voltage. Must be connected.
GNDA	7	7	5		Analog Ground. Must be connected.
VREGIN	3	3	2		Voltage Regulator Input
VIO	2	2	1		Port I/O Supply Voltage. Must be connected.
$\overline{\text{RST}}$/ C2CK	10	10	8	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} Monitor. Clock signal for the C2 Debug Interface.
P4.0/ C2D	9	—	—	D I/O or A In D I/O	Port 4.0. See SFR Definition 19.28. Bi-directional data signal for the C2 Debug Interface.
P3.0/ C2D		9	—	D I/O or A In D I/O	Port 3.0. See SFR Definition 19.24. Bi-directional data signal for the C2 Debug Interface.
P2.1/ C2D		—	7	D I/O or A In D I/O	Port 2.1. See SFR Definition 19.20. Bi-directional data signal for the C2 Debug Interface.
P0.0	8	8	6	D I/O or A In	Port 0.0. See SFR Definition 19.12.
P0.1	1	1	24	D I/O or A In	Port 0.1
P0.2	40	32	23	D I/O or A In	Port 0.2
P0.3	39	31	22	D I/O or A In	Port 0.3
P0.4	38	30	21	D I/O or A In	Port 0.4
P0.5	37	29	20	D I/O or A In	Port 0.5
P0.6	36	28	19	D I/O or A In	Port 0.6
P0.7	35	27	18	D I/O or A In	Port 0.7

Table 5.4. Reset Electrical Characteristics

–40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{RST}$ Output Low Voltage	VIO = 5 V; IOL = 70 µA	—	—	40	mV
$\overline{RST}$ Input High Voltage		0.7 x V_{IO}	—	—	
$\overline{RST}$ Input Low Voltage		—	—	0.3 x V_{IO}	
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 0.0 V, VIO = 5 V	—	49	115	µA
V_{DD} RST Threshold ($V_{RST-LOW}$)		1.65	1.75	1.80	V
V_{DD} RST Threshold ($V_{RST-HIGH}$)		2.25	2.30	2.45	V
V_{REGIN} Ramp Time for Power On	V_{REGIN} Ramp 0–1.8 V	—	—	1	ms
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation V_{DD} = 2.1 V V_{DD} = 2.5 V	 200 200	 340 250	 600 600	µs
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	155	175	µs
Minimum $\overline{RST}$ Low Time to Generate a System Reset		6	—	—	µs
V_{DD} Monitor Turn-on Time		—	60	100	µs
V_{DD} Monitor Supply Current		—	1	2	µA

Table 5.5. Flash Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F550-3, ‘F560-3, ‘F568-9, and ‘F570-1	32768[1]			Bytes
	C8051F554-7, ‘F564-7, and ‘F572-5	16384			
Endurance		20 k	150 k	—	Erase/Write
Retention	125 °C	10	—	—	Years
Erase Cycle Time	25 MHz System Clock	28	30	45	ms
Write Cycle Time	25 MHz System Clock	79	84	125	µs
V_{DD}	Write/Erase operations	$V_{RST-HIGH}$[2]	—	—	V
Temperature during Programming Operations	–I Devices –A Devices	0 –40	— —	+125 +125	°C

1. On the 32 kB Flash devices, 1024 bytes at addresses 0x7C00 to 0x7FFF are reserved.
2. See Table 5.4 for the $V_{RST-HIGH}$ specification.

Table 5.12. Comparator 0 and Comparator 1 Electrical Characteristics
VIO = 1.8 to 5.25 V, –40 to +125 °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Response Time: Mode 0, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	330	—	ns
	CPn+ – CPn– = –100 mV	—	390	—	ns
Response Time: Mode 1, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	490	—	ns
	CPn+ – CPn– = –100 mV	—	610	—	ns
Response Time: Mode 2, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	590	—	ns
	CP0+ – CP0– = –100 mV	—	750	—	ns
Response Time: Mode 3, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	2300	—	ns
	CPn+ – CPn– = –100 mV	—	3100	—	ns
Common-Mode Rejection Ratio		—	2.1	13	mV/V
Positive Hysteresis 1	CPnHYP1–0 = 00	-2	0	2	mV
Positive Hysteresis 2	CPnHYP1–0 = 01	2	6	10	mV
Positive Hysteresis 3	CPnHYP1–0 = 10	5	11	20	mV
Positive Hysteresis 4	CPnHYP1–0 = 11	13	21	40	mV
Negative Hysteresis 1	CPnHYN1–0 = 00	-2	0	2	mV
Negative Hysteresis 2	CPnHYN1–0 = 01	2	5	10	mV
Negative Hysteresis 3	CPnHYN1–0 = 10	5	11	20	mV
Negative Hysteresis 4	CPnHYN1–0 = 11	13	21	40	mV
Inverting or Non-Inverting Input Voltage Range		–0.25	—	V_{IO} + 0.25	V
Input Capacitance		—	8	—	pF
Input Offset Voltage		–10	—	+10	mV
Power Supply					
Power Supply Rejection		—	0.18	—	mV/V
Power-up Time		—	3	—	µs
Supply Current at DC	Mode 0	—	6.3	20	µA
	Mode 1	—	3.4	10	µA
	Mode 2	—	2.6	7.5	µA
	Mode 3	—	0.6	3	µA

***Note:** Vcm is the common-mode voltage on CP0+ and CP0–.

Post-Tracking Mode is selected when AD0TM is set to 01b. A programmable tracking time based on AD0TK is started immediately following the convert start signal. Conversions are started after the programmed tracking time ends. After a conversion is complete, ADC0 does not track the input. Rather, the sampling capacitor remains disconnected from the input making the input pin high-impedance until the next convert start signal.

Dual-Tracking Mode is selected when AD0TM is set to 11b. A programmable tracking time based on AD0TK is started immediately following the convert start signal. Conversions are started after the programmed tracking time ends. After a conversion is complete, ADC0 tracks continuously until the next conversion is started.

Depending on the output connected to the ADC input, additional tracking time, more than is specified in Table 5.9, may be required after changing MUX settings. See the settling time requirements described in Section “6.2.1. Settling Time Requirements” on page 52.

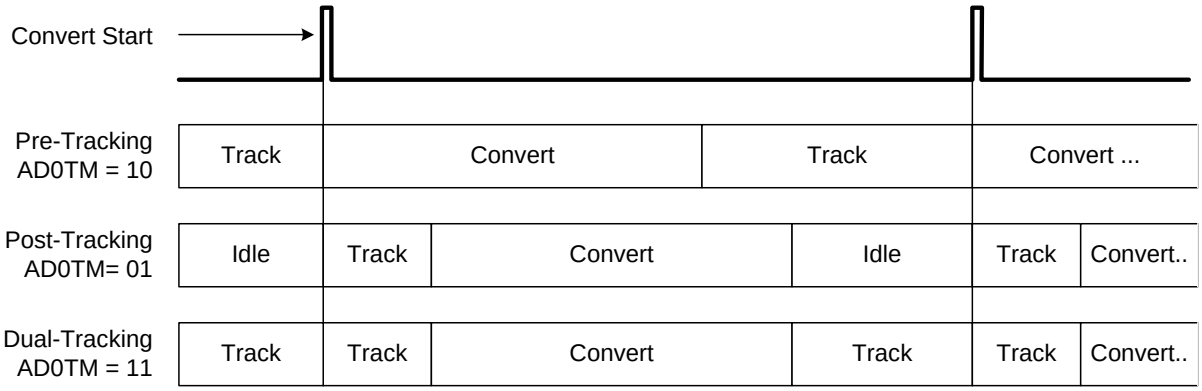

Figure 6.2. ADC0 Tracking Modes

6.1.3. Timing

ADC0 has a maximum conversion speed specified in Table 5.9. ADC0 is clocked from the ADC0 Subsystem Clock (FCLK). The source of FCLK is selected based on the BURSTEN bit. When BURSTEN is logic 0, FCLK is derived from the current system clock. When BURSTEN is logic 1, FCLK is derived from the Burst Mode Oscillator, an independent clock source with a maximum frequency of 25 MHz.

When ADC0 is performing a conversion, it requires a clock source that is typically slower than FCLK. The ADC0 SAR conversion clock (SAR clock) is a divided version of FCLK. The divide ratio can be configured using the AD0SC bits in the ADC0CF register. The maximum SAR clock frequency is listed in Table 5.9.

ADC0 can be in one of three states at any given time: tracking, converting, or idle. Tracking time depends on the tracking mode selected. For Pre-Tracking Mode, tracking is managed by software and ADC0 starts conversions immediately following the convert start signal. For Post-Tracking and Dual-Tracking Modes, the tracking time after the convert start signal is equal to the value determined by the AD0TK bits plus 2 FCLK cycles. Tracking is immediately followed by a conversion. The ADC0 conversion time is always 13 SAR clock cycles plus an additional 2 FCLK cycles to start and complete a conversion. Figure 6.3 shows timing diagrams for a conversion in Pre-Tracking Mode and tracking plus conversion in Post-Tracking or Dual-Tracking Mode. In this example, repeat count is set to one.

SFR Definition 6.9. ADC0GTH: ADC0 Greater-Than Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTH[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC4; SFR Page = 0x00

Bit	Name	Function
7:0	ADC0GTH[7:0]	**ADC0 Greater-Than Data Word High-Order Bits.**

SFR Definition 6.10. ADC0GTL: ADC0 Greater-Than Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC3; SFR Page = 0x00

Bit	Name	Function
7:0	ADC0GTL[7:0]	**ADC0 Greater-Than Data Word Low-Order Bits.**

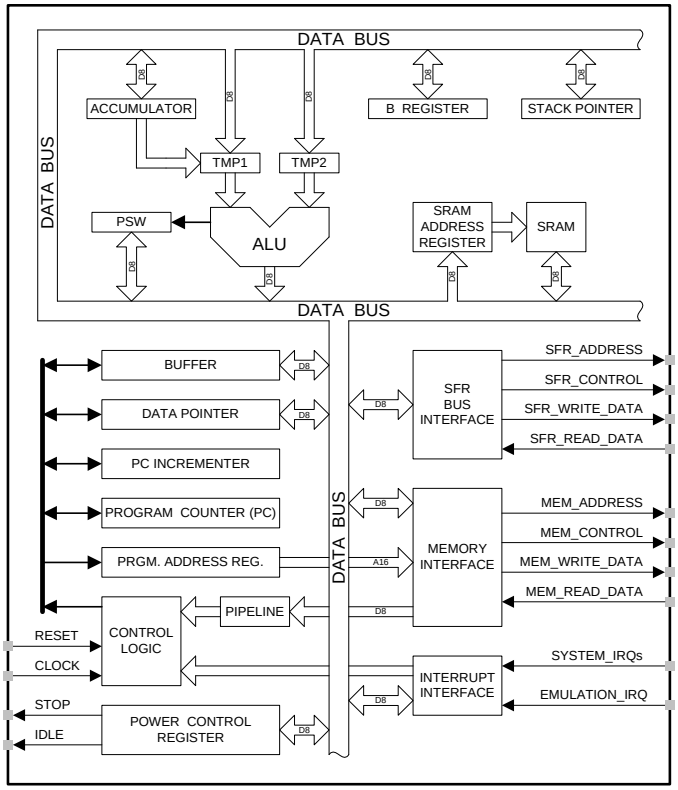

Figure 10.1. CIP-51 Block Diagram

With the CIP-51's maximum system clock at 50 MHz, it has a peak throughput of 50 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

Programming and Debugging Support

In-system programming of the Flash program memory and communication with on-chip debug support logic is accomplished via the Silicon Labs 2-Wire Development Interface (C2).

The on-chip debug support logic facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive, requiring no RAM, Stack, timers, or other on-chip resources. C2 details can be found in Section “27. C2 Interface” on page 300.

The CIP-51 is supported by development tools from Silicon Labs and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via the C2 interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

Table 10.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/(4-6)*
JNC rel	Jump if Carry is not set	2	2/(4-6)*
JB bit, rel	Jump if direct bit is set	3	3/(5-7)*
JNB bit, rel	Jump if direct bit is not set	3	3/(5-7)*
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/(5-7)*
Program Branching			
ACALL addr11	Absolute subroutine call	2	4-6*
LCALL addr16	Long subroutine call	3	5-7*
RET	Return from subroutine	1	6-8*
RETI	Return from interrupt	1	6-8*
AJMP addr11	Absolute jump	2	4-6*
LJMP addr16	Long jump	3	5-7*
SJMP rel	Short jump (relative address)	2	4-6*
JMP @A+DPTR	Jump indirect relative to DPTR	1	3-5*
JZ rel	Jump if A equals zero	2	2/(4-6)*
JNZ rel	Jump if A does not equal zero	2	2/(4-6)*
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	4/(6-8)*
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/(6-8)*
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/(5-7)*
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/(6-8)*
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/(4-6)*
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/(5-7)*
NOP	No operation	1	1

Note: Certain instructions take a variable number of clock cycles to execute depending on instruction alignment and the FLRT setting (SFR Definition 14.3).

12. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the C8051F55x/56x/57x's resources and peripherals. The CIP-51 controller core duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the C8051F55x/56x/57x. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 12.3 lists the SFRs implemented in the C8051F55x/56x/57x device family.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g., P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing unoccupied addresses in the SFR space will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 12.3, for a detailed description of each register.

12.1. SFR Paging

The CIP-51 features SFR paging, allowing the device to map many SFRs into the 0x80 to 0xFF memory address space. The SFR memory space has 256 *pages*. In this way, each memory location from 0x80 to 0xFF can access up to 256 SFRs. The C8051F55x/56x/57x family of devices utilizes three SFR pages: 0x00, 0x0C, and 0x0F. SFR pages are selected using the Special Function Register Page Selection register, SFRPAGE (see SFR Definition 11.3). The procedure for reading and writing an SFR is as follows:

1. Select the appropriate SFR page number using the SFRPAGE register.
2. Use direct accessing mode to read or write the special function register (MOV instruction).

12.2. Interrupts and SFR Paging

When an interrupt occurs, the SFR Page Register will automatically switch to the SFR page containing the flag bit that caused the interrupt. The automatic SFR Page switch function conveniently removes the burden of switching SFR pages from the interrupt service routine. Upon execution of the RETI instruction, the SFR page is automatically restored to the SFR Page in use prior to the interrupt. This is accomplished via a three-byte *SFR Page Stack*. The top byte of the stack is SFRPAGE, the current SFR Page. The second byte of the SFR Page Stack is SFRNEXT. The third, or bottom byte of the SFR Page Stack is SFRLAST. Upon an interrupt, the current SFRPAGE value is pushed to the SFRNEXT byte, and the value of SFRNEXT is pushed to SFRLAST. Hardware then loads SFRPAGE with the SFR Page containing the flag bit associated with the interrupt. On a return from interrupt, the SFR Page Stack is popped resulting in the value of SFRNEXT returning to the SFRPAGE register, thereby restoring the SFR page context without software intervention. The value in SFRLAST (0x00 if there is no SFR Page value in the bottom of the stack) of the stack is placed in SFRNEXT register. If desired, the values stored in SFRNEXT and SFRLAST may be modified during an interrupt, enabling the CPU to return to a different SFR Page upon execution of the RETI instruction (on interrupt exit). Modifying registers in the SFR Page Stack does not cause a push or pop of the stack. Only interrupt calls and returns will cause push/pop operations on the SFR Page Stack.

On the C8051F55x/56x/57x devices, vectoring to an interrupt will switch SFRPAGE to page 0x00, except for the CAN0 interrupt which will switch SFRPAGE to page 0x0C.

While in the CAN0 ISR, a PCA interrupt occurs. Recall the PCA interrupt is configured as a high priority interrupt, while the CAN0 interrupt is configured as a *low* priority interrupt. Thus, the CIP-51 will now vector to the high priority PCA ISR. Upon doing so, the CIP-51 will automatically place the SFR page needed to access the PCA's special function registers into the SFRPAGE register, SFR Page 0x00. The value that was in the SFRPAGE register before the PCA interrupt (SFR Page 0x0C for CAN0) is pushed down the stack into SFRNEXT. Likewise, the value that was in the SFRNEXT register before the PCA interrupt (in this case SFR Page 0x00 for SPI0DAT) is pushed down to the SFRLAST register, the "bottom" of the stack. Note that a value stored in SFRLAST (via a previous software write to the SFRLAST register) will be overwritten. See Figure 12.4.

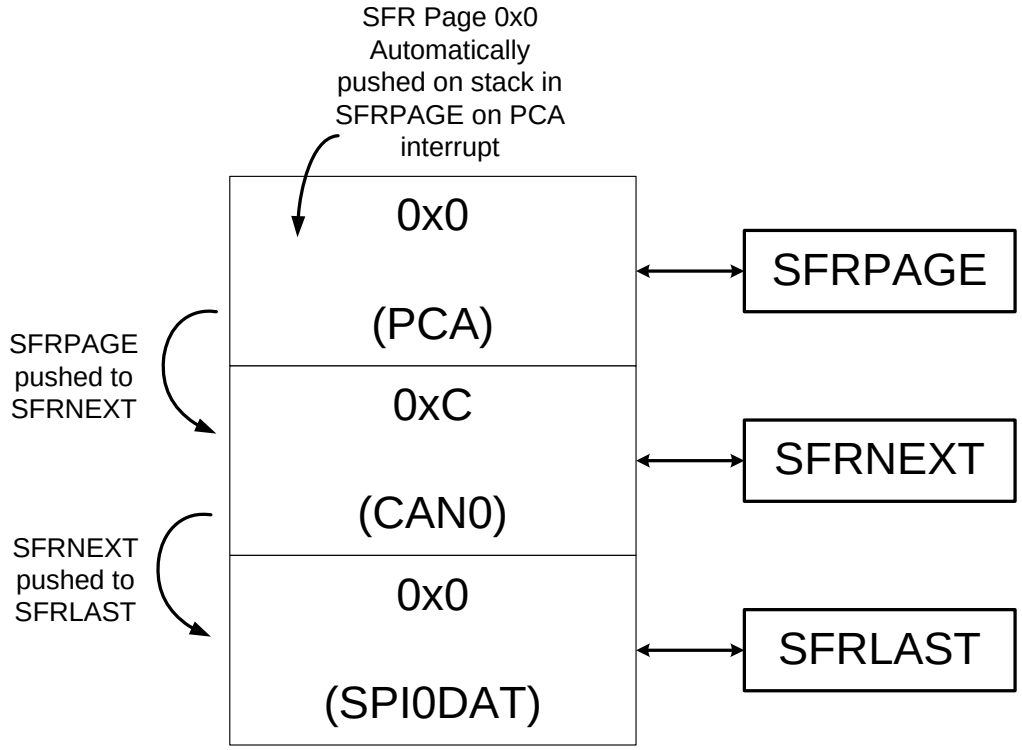

Figure 12.4. SFR Page Stack Upon PCA Interrupt Occurring During a CAN0 ISR

SFR Definition 15.1. PCON: Power Control

Bit	7	6	5	4	3	2	1	0
Name	GF[5:0]						STOP	IDLE
Type	R/W						R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x87; SFR Page = All Pages

Bit	Name	Function
7:2	GF[5:0]	**General Purpose Flags 5–0.** These are general purpose flags for use under software control.
1	STOP	**Stop Mode Select.** Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0. 1: CPU goes into Stop mode (internal oscillator stopped).
0	IDLE	**IDLE: Idle Mode Select.** Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0. 1: CPU goes into Idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)

SFR Definition 16.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name		FERROR	C0RSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Type	R	R	R/W	R/W	R	R/W	R/W	R
Reset	0	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xEF; SFR Page = 0x00

Bit	Name	Description	Write	Read
7	Unused	**Unused.**	Don't care.	0
6	FERROR	**Flash Error Reset Flag.**	N/A	Set to 1 if Flash read/write/erase error caused the last reset.
5	C0RSEF	**Comparator0 Reset Enable and Flag.**	Writing a 1 enables Comparator0 as a reset source (active-low).	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	**Software Reset Force and Flag.**	Writing a 1 forces a system reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	**Watchdog Timer Reset Flag.**	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	**Missing Clock Detector Enable and Flag.**	Writing a 1 enables the Missing Clock Detector. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	**Power-On/V_{DD} Monitor Reset Flag, and V_{DD} monitor Reset Enable.**	Writing a 1 enables the V_{DD} monitor as a reset source. **Writing 1 to this bit before the V_{DD} monitor is enabled and stabilized may cause a system reset.**	Set to 1 anytime a power-on or V_{DD} monitor reset occurs. **When set to 1 all other RSTSRC flags are indeterminate.**
0	PINRSF	**HW Pin Reset Flag.**	N/A	Set to 1 if $\overline{\text{RST}}$ pin caused the last reset.

Note: Do not use read-modify-write operations on this register

17.5. Memory Mode Selection

The external data memory space can be configured in one of four modes, shown in Figure 17.2, based on the EMIF Mode bits in the EMI0CF register (SFR Definition 17.2). These modes are summarized below. More information about the different modes can be found in Section “17.6. Timing” on page 151.

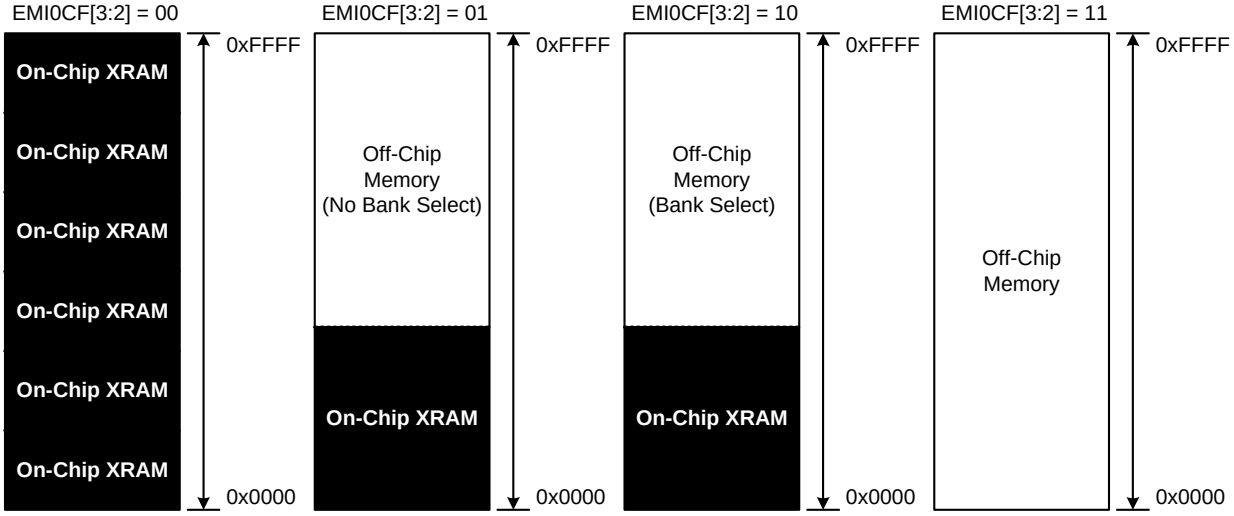

Figure 17.2. EMIF Operating Modes

17.5.1. Internal XRAM Only

When bits EMI0CF[3:2] are set to 00, all MOVX instructions will target the internal XRAM space on the device. Memory accesses to addresses beyond the populated space will wrap on 2 kB boundaries. As an example, the addresses 0x800 and 0x1000 both evaluate to address 0x0000 in on-chip XRAM space.

- 8-bit MOVX operations use the contents of EMI0CN to determine the high-byte of the effective address and R0 or R1 to determine the low-byte of the effective address.
- 16-bit MOVX operations use the contents of the 16-bit DPTR to determine the effective address.

17.5.2. Split Mode without Bank Select

When bit EMI0CF.[3:2] are set to 01, the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the internal XRAM size boundary will access on-chip XRAM space.
- Effective addresses above the internal XRAM size boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. However, in the “No Bank Select” mode, an 8-bit MOVX operation will not drive the upper 8-bits A[15:8] of the Address Bus during an off-chip access. This allows the user to manipulate the upper address bits at will by setting the Port state directly via the port latches. This behavior is in contrast with “Split Mode with Bank Select” described below. The lower 8-bits of the Address Bus A[7:0] are driven, determined by R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and unlike 8-bit MOVX operations, the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

17.6.1.2. 8-bit MOVX without Bank Select: EMI0CF[4:2] = 001 or 011

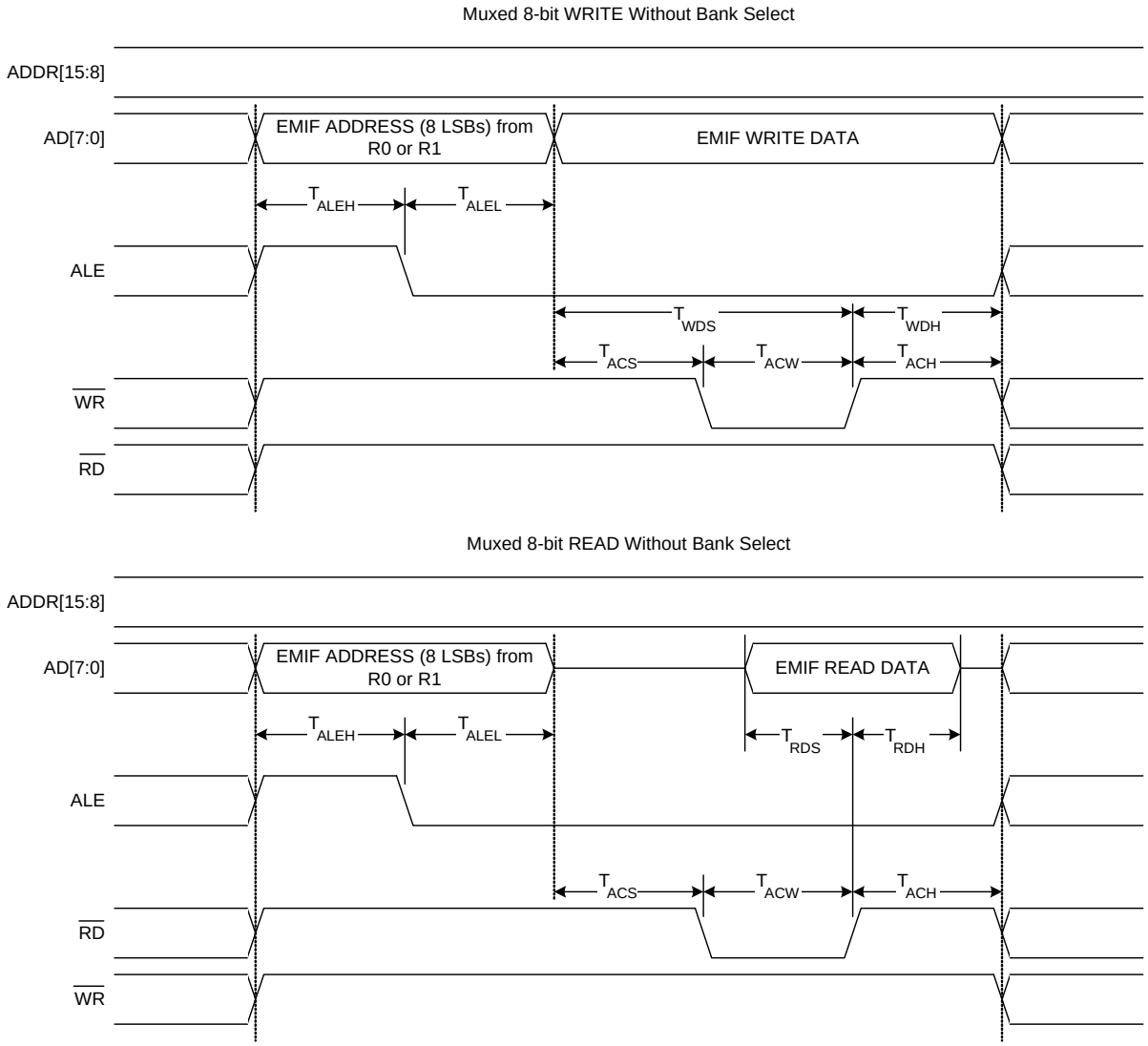

Figure 17.4. Multiplexed 8-bit MOVX without Bank Select Timing

18. Oscillators and Clock Selection

C8051F55x/56x/57x devices include a programmable internal high-frequency oscillator, an external oscillator drive circuit, and a clock multiplier. The internal oscillator can be enabled/disabled and calibrated using the OSCICN, OSCICRS, and OSCIFIN registers, as shown in Figure 18.1. The system clock can be sourced by the external oscillator circuit or the internal oscillator. The clock multiplier can produce three possible base outputs which can be scaled by a programmable factor of 1, 2/3, 2/4 (or 1/2), 2/5, 2/6 (or 1/3), or 2/7: Internal Oscillator x 2, Internal Oscillator x 4, External Oscillator x 2, or External Oscillator x 4.

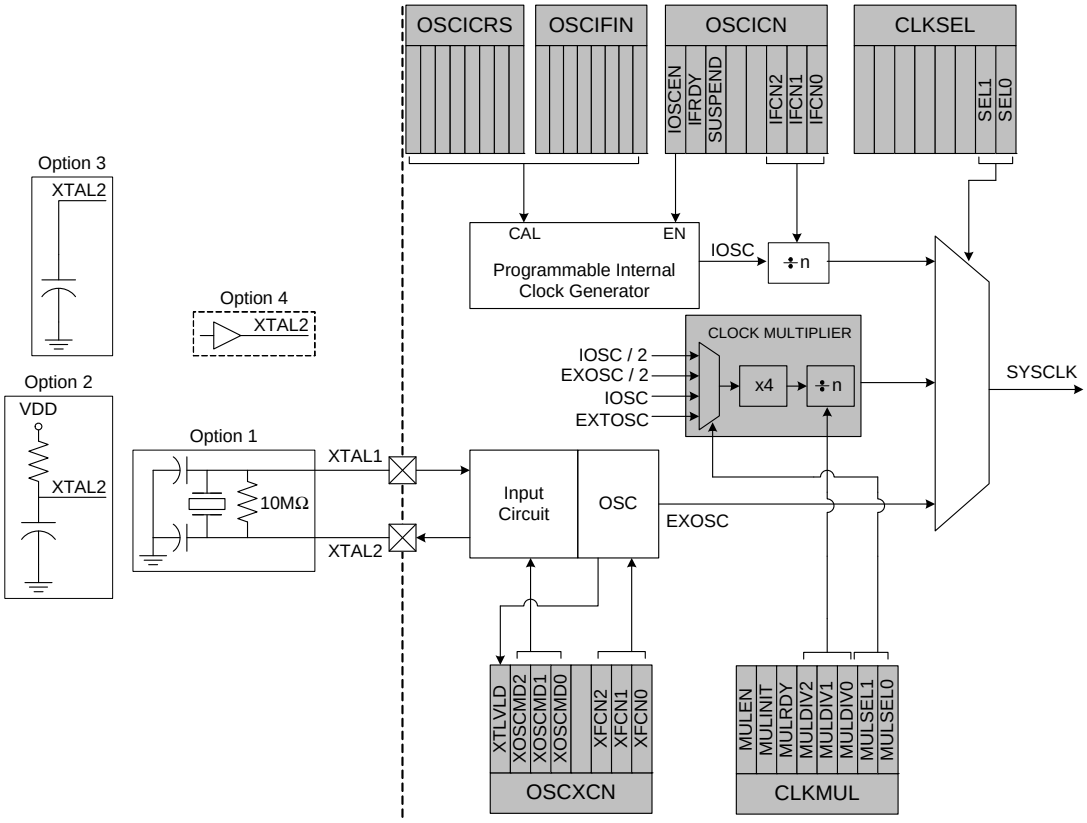

Figure 18.1. Oscillator Options

18.1. System Clock Selection

The CLKSL[1:0] bits in register CLKSEL select which oscillator source is used as the system clock. CLKSL[1:0] must be set to 01b for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA) when the internal oscillator is selected as the system clock. The system clock may be switched on-the-fly between the internal oscillator, external oscillator, and Clock Multiplier so long as the selected clock source is enabled and has settled.

The internal oscillator requires little start-up time and may be selected as the system clock immediately following the register write which enables the oscillator. The external RC and C modes also typically require no startup time.

External crystals and ceramic resonators however, typically require a start-up time before they are settled and ready for use. The Crystal Valid Flag (XTLVLD in register OSCXCN) is set to 1 by hardware when the external crystal or ceramic resonator is settled. **In crystal mode, to avoid reading a false XTLVLD, software should delay at least 1 ms between enabling the external oscillator and checking XTLVLD.**

When a digital I/O cell is placed in the high impedance state, a weak pull-up transistor pulls the Port pad to the VIO supply voltage to ensure the digital input is at a defined logic state. Weak pull-ups are disabled when the I/O cell is driven to GND to minimize power consumption and may be globally disabled by setting WEAKPUD to 1. The user should ensure that digital I/O are always internally or externally pulled or driven to a valid logic state to minimize power consumption. Port pins configured for digital I/O always read back the logic state of the Port pad, regardless of the output logic value of the Port pin.

19.1.3. Interfacing Port I/O in a Multi-Voltage System

All Port I/O are capable of interfacing to digital logic operating at a supply voltage higher than VDD and less than 5.25 V. Connect the VIO pin to the voltage source of the interface logic.

19.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins P0.0–P3.7 can be assigned to various analog, digital, and external interrupt functions. P4.0 can be assigned to only digital functions. The Port pins assigned to analog functions should be configured for analog I/O, and Port pins assigned to digital or external interrupt functions should be configured for digital I/O.

19.2.1. Assigning Port I/O Pins to Analog Functions

Table 19.1 shows all available analog functions that require Port I/O assignments. **Port pins selected for these analog functions should have their corresponding bit in PnSKIP set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the Crossbar. Table 19.1 shows the potential mapping of Port I/O to each analog function.

Table 19.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P3.7[1]	ADC0MX, PnSKIP
Comparator0 or Compartor1 Input	P0.0–P2.7[1]	CPT0MX, CPT1MX, PnSKIP
Voltage Reference (VREF0)[2]	P0.0	REF0CN, PnSKIP
External Oscillator in Crystal Mode (XTAL1)	P0.2	OSCXCN, PnSKIP
External Oscillator in RC, C, or Crystal Mode (XTAL2)	P0.3	OSCXCN, PnSKIP

Notes:
1. P3.1–P3.7 are available on the 40-pin packages. P2.2-P3.0 are available 40-pin and 32-pin packages.
2. If VDD is selected as the voltage reference in the REF0CN register and the ADC is enabled in the ADC0CN register, the P0.0/VREF pin cannot operate as a general purpose I/O pin in open-drain mode. With the above settings, this pin can operate in push-pull output mode or as an analog input.

19.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the Crossbar for pin assignment; however, some digital functions bypass the Crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in PnSKIP set to 1.** Table 19.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

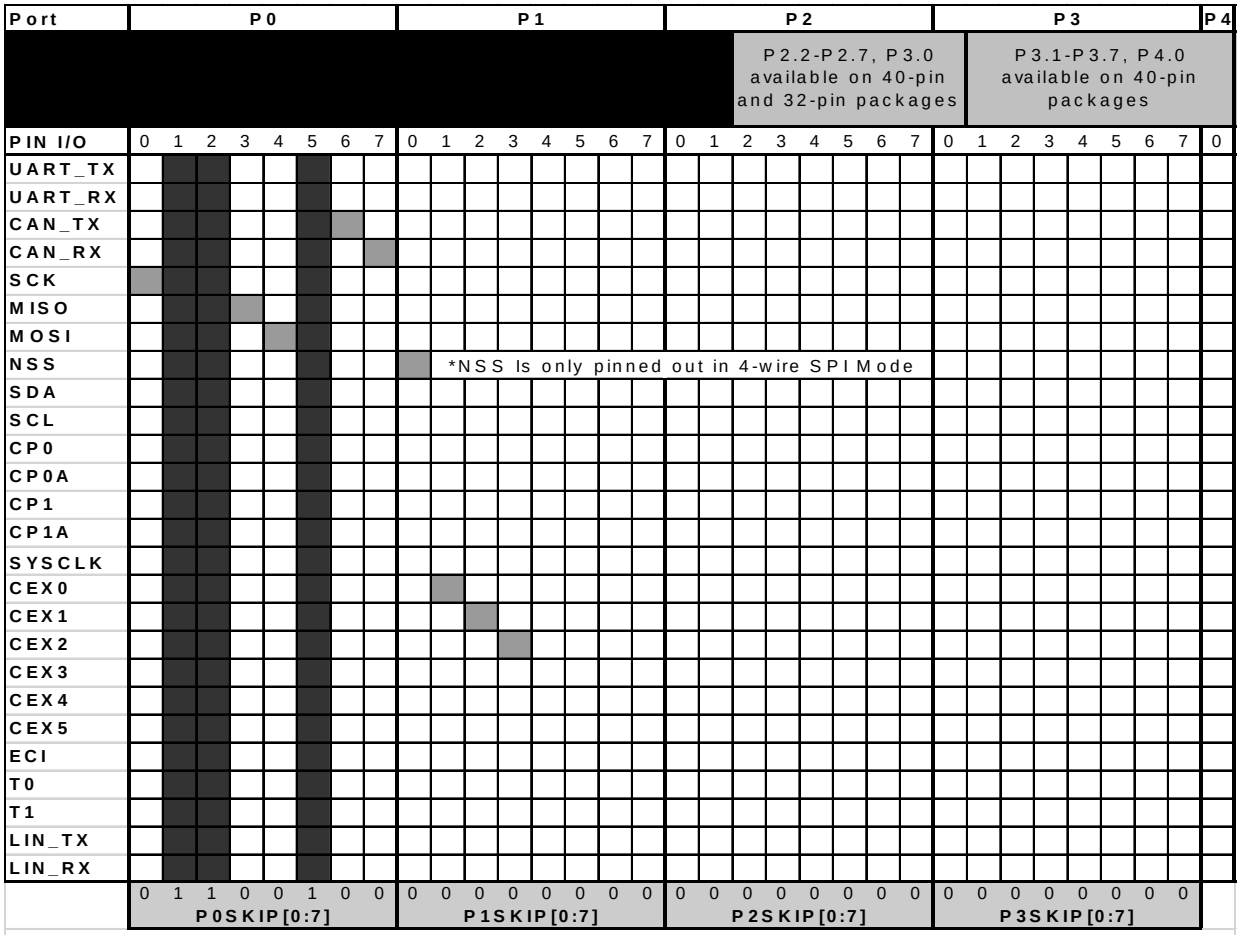

Figure 19.4. Crossbar Priority Decoder in Example Configuration

19.4. Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all Port pins, using the Port Input Mode register (PnMDIN).
2. Select the output mode (open-drain or push-pull) for all Port pins, using the Port Output Mode register (PnMDOUT).
3. Select any pins to be skipped by the I/O Crossbar using the Port Skip registers (PnSKIP).
4. Assign Port pins to desired peripherals.
5. Enable the Crossbar (XBARE = 1).

All Port pins must be configured as either analog or digital inputs. Port 4 C8051F568-9 and ‘F570-5 is a digital-only Port. Any pins to be used as Comparator or ADC inputs should be configured as an analog inputs. When a pin is configured as an analog input, its weak pullup, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however this practice is not recommended.

Additionally, all analog input pins should be configured to be skipped by the Crossbar (accomplished by setting the associated bits in PnSKIP). Port input mode is set in the PnMDIN register, where a 1 indicates a digital input, and a 0 indicates an analog input. All pins default to digital inputs on reset. See SFR Definition 19.13 for the PnMDIN register details.

SFR Definition 19.17. P1MDIN: Port 1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF2; SFR Page = 0x0F

Bit	Name	Function
7:0	P1MDIN[7:0]	**Analog Configuration Bits for P1.7–P1.0 (respectively).** Port pins configured for analog mode have their weak pull-up and digital receiver disabled. For analog mode, the pin also needs to be configured for open-drain mode in the P1MDOUT register. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.

SFR Definition 19.18. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA5; SFR Page = 0x0F

Bit	Name	Function
7:0	P1MDOUT[7:0]	**Output Configuration Bits for P1.7–P1.0 (respectively).** These bits are ignored if the corresponding bit in register P1MDIN is logic 0. 0: Corresponding P1.n Output is open-drain. 1: Corresponding P1.n Output is push-pull.

Table 22.4. SMBus Status Decoding

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X	1100
	1100	0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X	1110
						Abort transfer.	0	1	X	—
		0	0	1	A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0DAT.	0	0	X	1100
						End transfer with STOP.	0	1	X	—
						End transfer with STOP and start another transfer.	1	1	X	—
						Send repeated START.	1	0	X	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT).	0	0	X	1000
Master Receiver	1000	1	0	X	A master data byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	1000
						Send NACK to indicate last byte, and send STOP.	0	1	0	—
						Send NACK to indicate last byte, and send STOP followed by START.	1	1	0	1110
						Send ACK followed by repeated START.	1	0	1	1110
						Send NACK to indicate last byte, and send repeated START.	1	0	0	1110
						Send ACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	1	1100
						Send NACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	0	1100