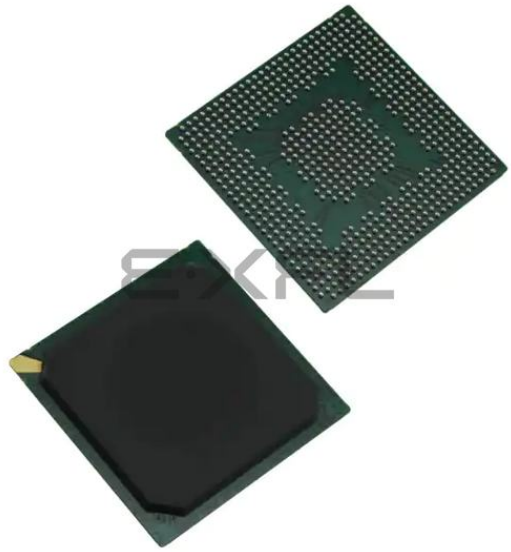

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8343czqagd

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications.*

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8343EA.

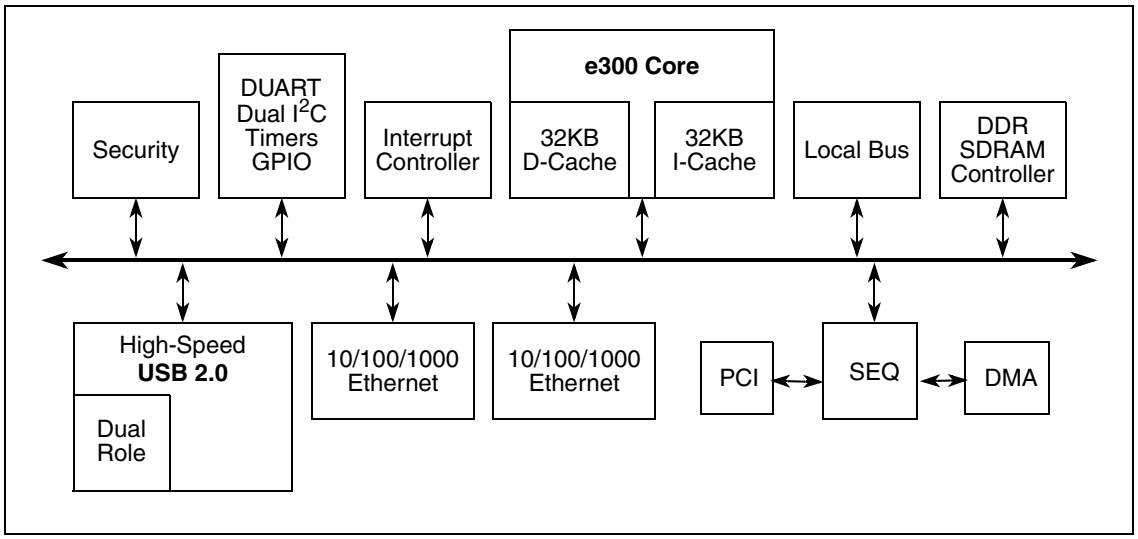


Figure 1. MPC8343EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 400 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- bit data interface, up to 266 MHz data rate

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI

- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - Public key execution unit (PKEU) :
    - RSA and Diffie-Hellman algorithms
    - Programmable field size up to 2048 bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511 bits
  - Data encryption standard (DES) execution unit (DEU)
    - DES and 3DES algorithms
    - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric-key cipher
    - Key lengths of 128, 192, and 256 bits
    - ECB, CBC, CCM, and counter (CTR) modes
  - XOR parity generation accelerator for RAID applications
  - ARC four execution unit (AFEU)
    - Stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - Message digest execution unit (MDEU)
    - SHA with 160-, 224-, or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Random number generator (RNG)
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Static and/or dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality
  - Complies with USB specification Rev. 2.0
  - Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8343EA.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8343EA.

Table 9. RESET Pins DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage[2]	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

Table 13 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 13. DDR2 SDRAM Capacitance for $GV_{DD}(typ) = 1.8$ V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. $GV_{DD} = 1.8$ V ± 0.090 V, f = 1 MHz, $T_A = 25°C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5$ V.

Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5$ V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current ($V_{OUT} = 1.95$ V)	I_{OH}	–15.2	—	mA	—
Output low current ($V_{OUT} = 0.35$ V)	I_{OL}	15.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 \text{ V} \le V_{OUT} \le GV_{DD}$.

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5$ V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. $GV_{DD} = 2.5$ V ± 0.125 V, f = 1 MHz, $T_A = 25°C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz		–600	600		3
333 MHz		–750	750		—

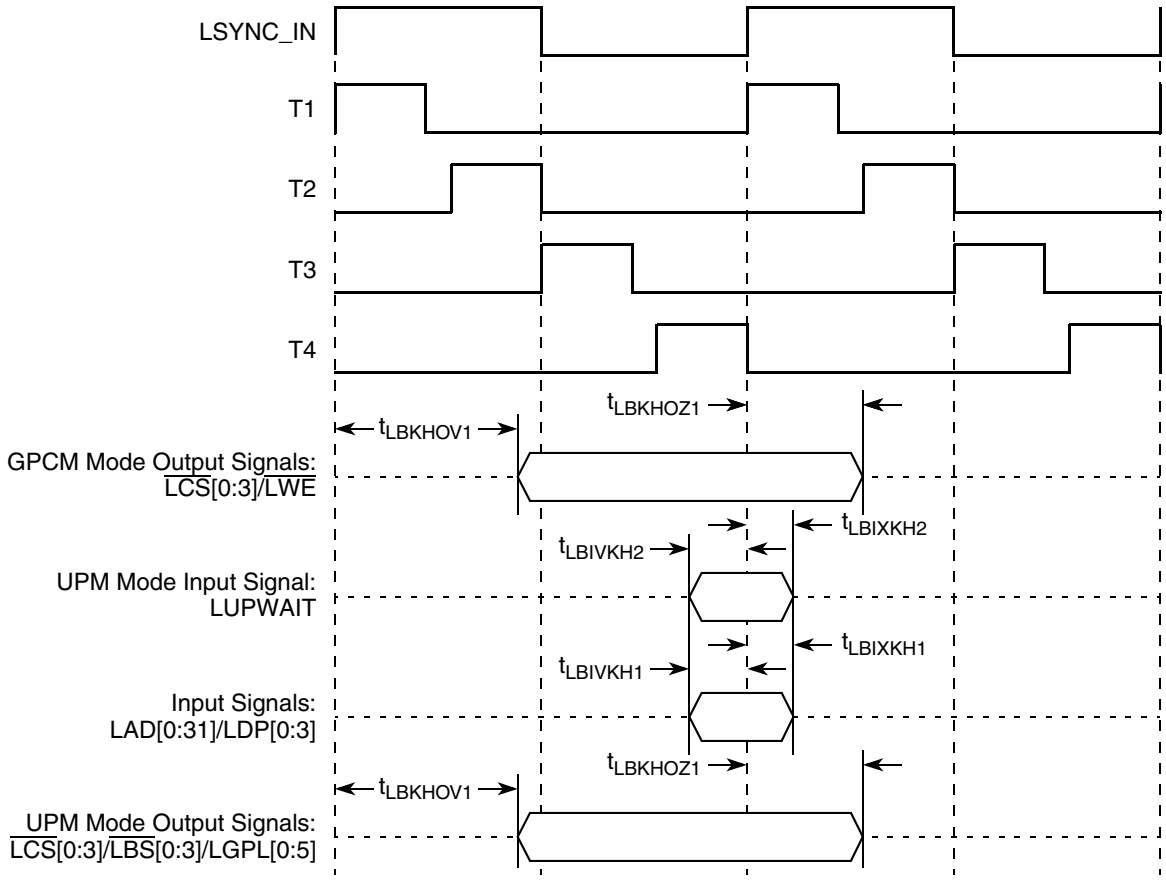


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

11.1 JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

Table 36. JTAG Interface DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	OV_{DD} – 0.3	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V

Table 36. JTAG Interface DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA. Table 37 provides the JTAG AC timing specifications as defined in Figure 24 through Figure 27.

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 23 provides the AC test load for TDO and the boundary-scan outputs of the MPC8343EA.

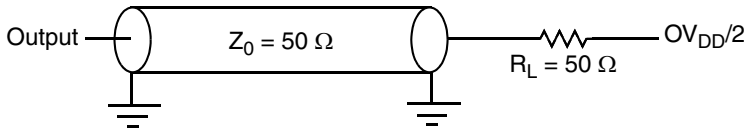


Figure 23. AC Test Load for the JTAG Interface

Figure 24 provides the JTAG clock input timing diagram.

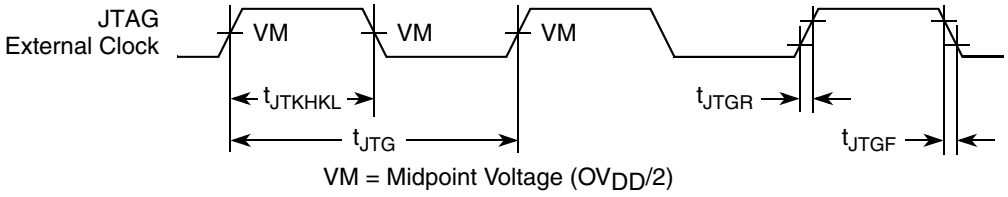


Figure 24. JTAG Clock Input Timing Diagram

Figure 25 provides the $\overline{\text{TRST}}$ timing diagram.

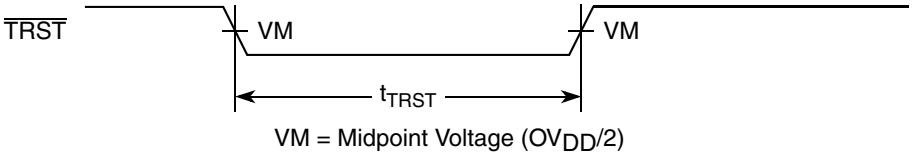


Figure 25. $\overline{\text{TRST}}$ Timing Diagram

Figure 26 provides the boundary-scan timing diagram.

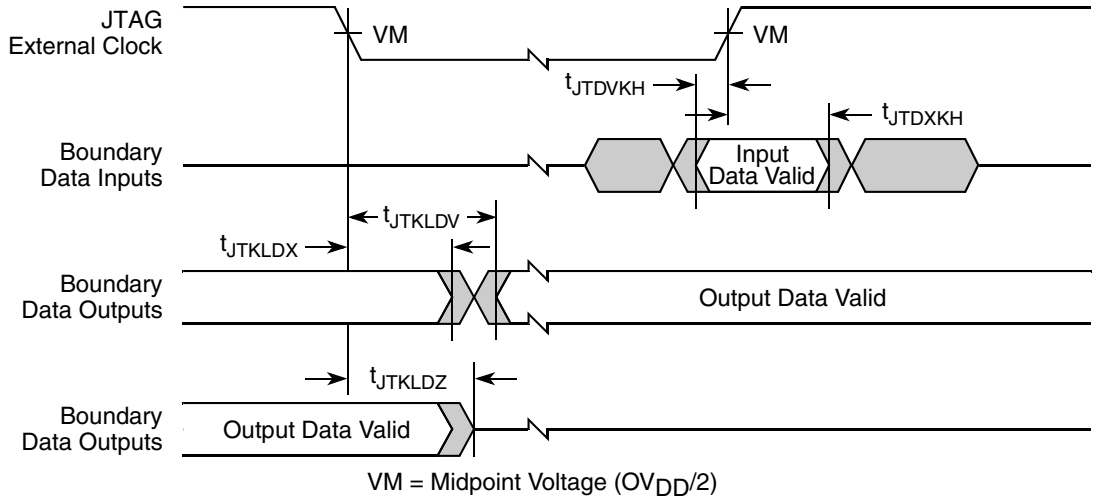


Figure 26. Boundary-Scan Timing Diagram

Figure 27 provides the test access port timing diagram.

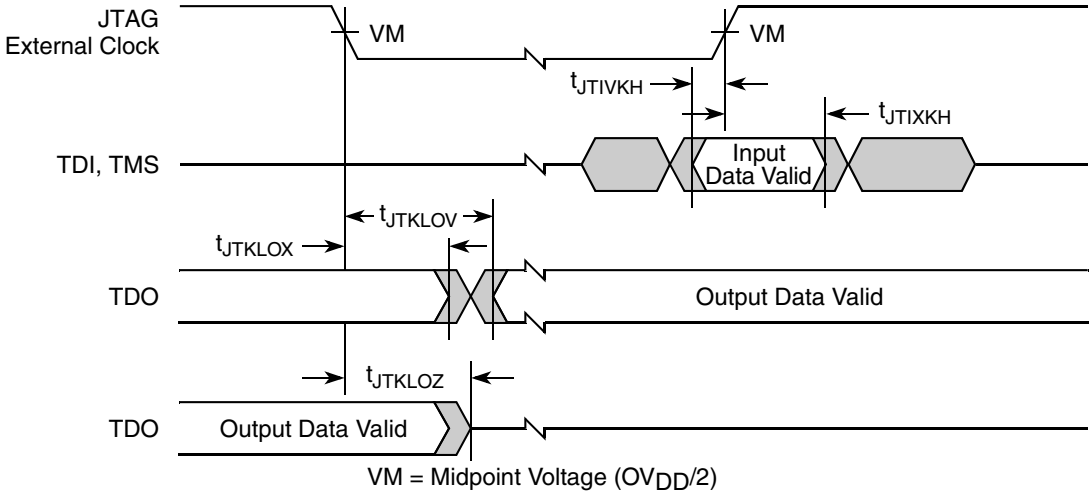


Figure 27. Test Access Port Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8343EA.

13.1 PCI DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the PCI interface of the MPC8343EA.

Table 40. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN}[1]= 0 V or $V_{IN} = OV_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8343EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 41 provides the PCI AC timing specifications at 66 MHz.

Table 41. PCI AC Timing Specifications at 66 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

Figure 31 shows the PCI input AC timing diagram.

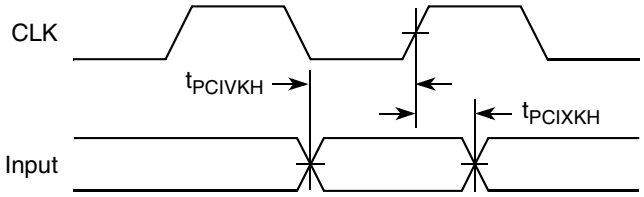


Figure 31. PCI Input AC Timing Diagram

Figure 32 shows the PCI output AC timing diagram.

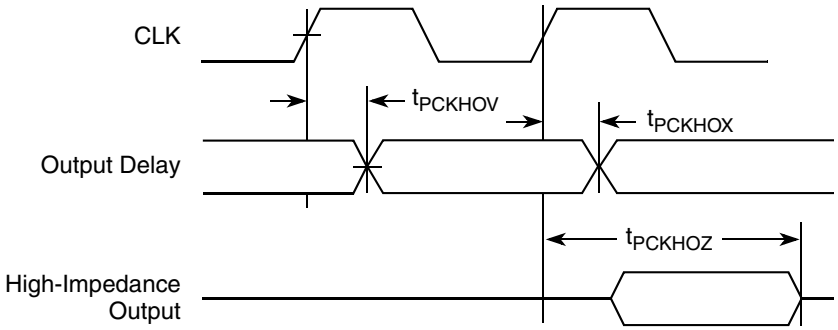


Figure 32. PCI Output AC Timing Diagram

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the MPC8343EA timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 43. Timer DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

Table 44. Timers Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8343EA GPIO.

Table 45. GPIO DC Electrical Characteristics

PArameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 46 provides the GPIO input and output AC timing specifications.

Table 46. GPIO Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

Table 49. SPI DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 50 provides the SPI input and output AC timing specifications.

Table 50. SPI AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the SPI.

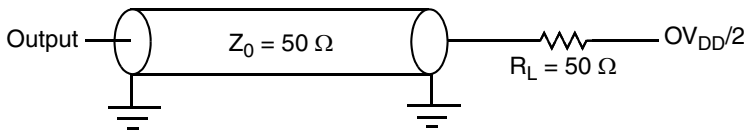
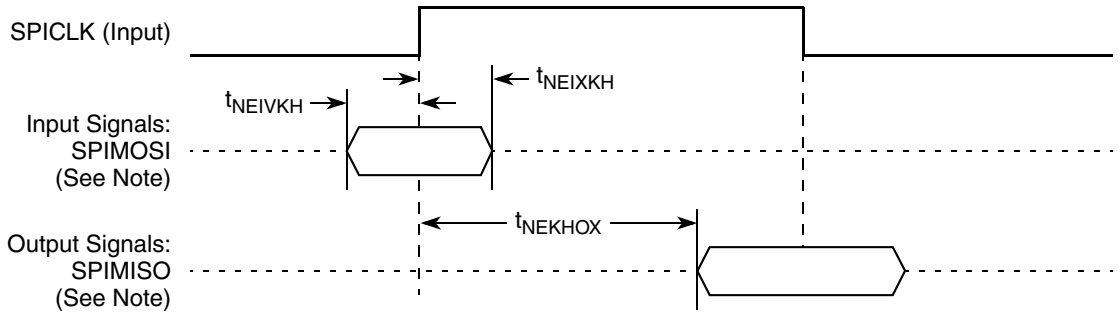


Figure 33. SPI AC Test Load

Figure 34 and Figure 35 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

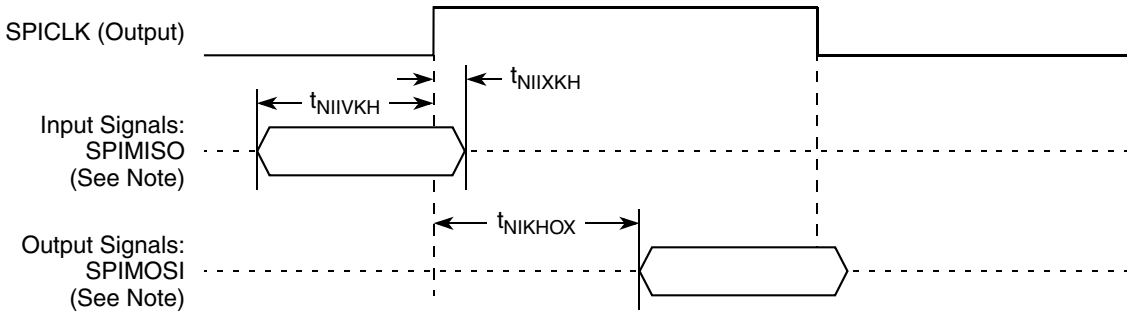
Figure 34 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 35 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8343EA is available in a plastic ball grid array (PBGA). See Section 18.1, "Package Parameters for the MPC8343EA PBGA," and Section 18.2, "Mechanical Dimensions for the MPC8343EA PBGA."

18.1 Package Parameters for the MPC8343EA PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USB				
DR_D0_ENABLEN	C28	I/O	OV_{DD}	—
DR_D1_SER_TXD	F25	I/O	OV_{DD}	—
DR_D2_VMO_SE0	B28	I/O	OV_{DD}	—
DR_D3_SPEED	C27	I/O	OV_{DD}	—
DR_D4_DP	D26	I/O	OV_{DD}	—
DR_D5_DM	E25	I/O	OV_{DD}	—
DR_D6_SER_RCV	C26	I/O	OV_{DD}	—
DR_D7_DRVVBUS	D25	I/O	OV_{DD}	—
DR_SESS_VLD_NXT	B26	I	OV_{DD}	—
DR_XCVR_SEL_DPPULLUP	E24	I/O	OV_{DD}	—
DR_STP_SUSPEND	A27	O	OV_{DD}	—
DR_RX_ERROR_PWRFAULT	C25	I	OV_{DD}	—
DR_TX_VALID_PCTL0	A26	O	OV_{DD}	—
DR_TX_VALIDH_PCTL1	B25	O	OV_{DD}	—
DR_CLK	A25	I	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E8	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	J28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV_{DD}	—
Ethernet Management Interface				
EC_MDC	Y24	O	LV_{DD1}	—
EC_MDIO	Y25	I/O	LV_{DD1}	11
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV_{DD1}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV_{DD}	—
TSEC1_CRS/GPIO2[21]	U25	I/O	LV_{DD1}	—
TSEC1_GTX_CLK	V24	O	LV_{DD1}	3
TSEC1_RX_CLK	U26	I	LV_{DD1}	—

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
OV_{DD}	B27, D3, D11, D19, E15, E23, F5, F8, F11, F14, F17, F20, G24, H23, H24, J6, J14, J17, J18, K4, L9, L20, L23, L25, M6, M9, M20, P5, P20, P23, R6, R9, R24, U23, V4, V6	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	—
MVREF1	AF19	I	DDR reference voltage	—
MVREF2	AE10	I	DDR reference voltage	—
No Connection				
NC	A22, A23, A24, B22, B23, B24, C21, C22, C23, C24, D21, D22, D23, D24, E21, M27, M28, N26, N27, N28, P25, P26, P27, R28, T24, T25, T26, T27, T28, U27, U28, Y3, Y4, Y5, AA1, AA2, AA3, AA4, AB1, AB2, AB3, AB4, AC1, AC2, AC3, AC4, AD1, AD2, AD3, AD5, AD7, AD11, AD12, AE4, AE6, AE8, AE9, AE23, AF1, AF5, AF6, AF8, AF24, AG1, AG3, AG4, AG7, AG8, AG9, AG10, AH2, AH3, AH5, AH8, AH9, V5, V2, V1	—	—	—

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must be always be tied to GND.
7. This pin must always be pulled up to OV_{DD}.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
11. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to LV_{DD1}.
12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pull up on LGPL4 is required.

Table 55. CSB Frequency Options for Host Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

1 CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Table 56. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266

Table 58. Suggested PLL Configurations (continued)

Ref No.[1]	RCWL		266 MHz Device			333 MHz Device			400 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
326	**0011**	**0100110**	—			33	100	300	33	100	300
623	**0110**	**0100011**	—			33	200	300	33	200	300
922	**1001**	**0100010**	—			33	300	300	33	300	300
425	**0100**	**0100101**	—			33	133	333	33	133	333
524	**0101**	**0100100**	—			33	166	333	33	166	333
A22	**1010**	**0100010**	—			33	333	333	33	333	333
723	**0111**	**0100011**	—			—			33	233	350
604	**0110**	**0000100**	—			—			33	200	400
624	**0110**	**0100100**	—			—			33	200	400
823	1000	0100011	—			—			33	266	400
66 MHz CLKIN/PCI_CLK Options											
242	**0010**	**1000010**	66	133	133	66	133	133	66	133	133
322	**0011**	**0100010**	66	200	200	66	200	200	66	200	200
224	**0010**	**0100100**	66	133	266	66	133	266	66	133	266
422	**0100**	**0100010**	66	266	266	66	266	266	66	266	266
323	**0011**	**0100011**	—			66	200	300	66	200	300
223	**0010**	**0100101**	—			66	133	333	66	133	333
522	**0101**	**0100010**	—			66	333	333	66	333	333
304	**0011**	**0000100**	—			—			66	200	400
324	**0011**	**0100100**	—			—			66	200	400
403	**0100**	**0000011**	—			—			66	266	400
423	**0100**	**0100011**	—			—			66	266	400

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so

parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 62. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature[1] Range**	**Package[2]**	**Processor Frequency[3]**	**Platform Frequency**	**Revision Level**
MPC	8343	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400	D = 266	B = 3.1

Notes:
1. For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266 and up to with a platform frequency of 333
2. See Section 18, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

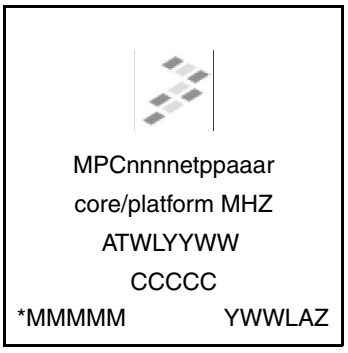
Table 63 shows the SVR settings by device and package type.

Table 63. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8343EA	PBGA	8056_0030
MPC8343A	PBGA	8057_0030

22.2 Part Marking

Parts are marked as in the example shown in Figure 40.



PBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 40. Freescale Part Marking for PBGA Devices