
**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (3) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 620-BBGA Exposed Pad |
| Supplier Device Package | 620-HBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8343czqagdb |

**NOTE**

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

# 1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8343EA.

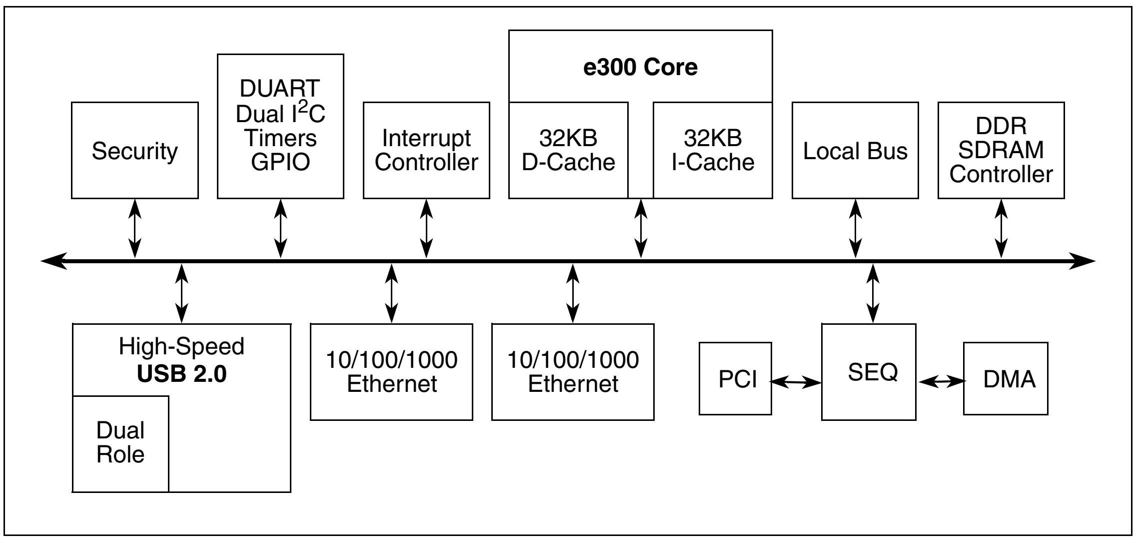



**Figure 1. MPC8343EA Block Diagram**

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 400 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- bit data interface, up to 266 MHz data rate

- — Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- — DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
- — Full error checking and correction (ECC) support
- — Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- — Contiguous or discontiguous memory mapping
- — Read-modify-write support
- — Sleep-mode support for SDRAM self refresh
- — Auto refresh
- — On-the-fly power management using CKE
- — Registered DIMM support
- — 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2

- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - — Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - — Ethernet physical interfaces:
    - – 1000 Mbps IEEE Std. 802.3 RGMII, IEEE Std. 802.3z RTBI, full-duplex
    - – 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - — Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - — 9.6-Kbyte jumbo frame support
  - — RMON statistics support
  - — Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - — MII management interface for control and status
  - — Programmable CRC generation and checking
- PCI interface
  - — Designed to comply with *PCI Specification Revision 2.3*
  - — Data bus width:
    - – 32-bit data PCI interface operating at up to 66 MHz
  - — PCI 3.3-V compatible
  - — PCI host bridge capabilities
  - — PCI agent mode on PCI interface
  - — PCI-to-memory and memory-to-PCI streaming
  - — Memory prefetching of PCI read accesses and support for delayed read transactions
  - — Posting of processor-to-PCI and PCI-to-memory writes
  - — On-chip arbitration supporting five masters on PCI
  - — Accesses to all PCI address spaces
  - — Parity supported
  - — Selectable hardware-enforced coherency

- Can operate as a stand-alone USB host controller
  - USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
  - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)

- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects for eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard I$^2$C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I$^2$C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I$^2$C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters

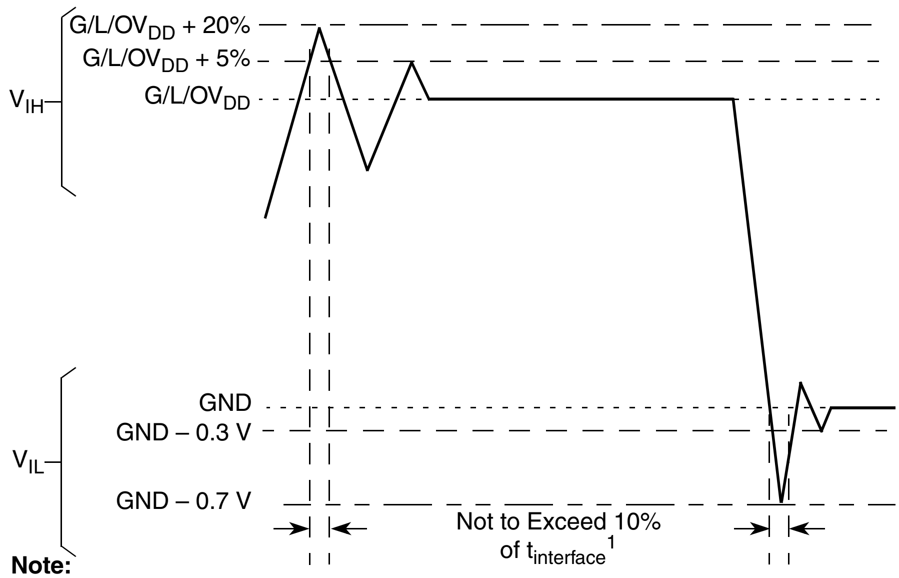
**Table 2. Recommended Operating Conditions (continued)**

| Parameter | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | $OV_{DD}$ | 3.3 V ± 330 mV | V | — |

**Note:**

1 $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, $AV_{DD}$, and $V_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8343EA.




**Note:**

1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

**Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}$/$OV_{DD}$/$LV_{DD}$**

## 5.2 RESET AC Electrical Characteristics

Table 10 provides the reset initialization AC timing specifications of the MPC8343EA.

**Table 10. RESET Initialization Timing Specifications**

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of HRESET or SRESET (input) to activate reset flow | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Required assertion time of PORESET with stable clock applied to CLKIN when the MPC8343EA is in PCI host mode | 32 | — | $t_{CLKIN}$ | 2 |
| Required assertion time of PORESET with stable clock applied to PCI_SYNC_IN when the MPC8343EA is in PCI agent mode | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| HRESET/SRESET assertion (output) | 512 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| HRESET negation to SRESET negation (output) | 16 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8343EA is in PCI host mode | 4 | — | $t_{CLKIN}$ | 2 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8343EA is in PCI agent mode | 4 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input hold time for POR configuration signals with respect to negation of HRESET | 0 | — | ns | — |
| Time for the MPC8343EA to turn off POR configuration signals with respect to the assertion of HRESET | — | 4 | ns | 3 |
| Time for the MPC8343EA to turn on POR configuration signals with respect to the negation of HRESET | 1 | — | $t_{PCI\_SYNC\_IN}$ | 1, 3 |

**Notes:**
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
2. $t_{CLKIN}$ is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

**Table 11. PLL and DLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| PLL lock times | — | 100 | µs | — |
| DLL lock times | 7680 | 122,880 | csb_clk cycles | 1, 2 |

**Notes:**
1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, “Clocking.”

# 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8343EA. Note that DDR SDRAM is $GV_{DD}$(typ) = 2.5 V and DDR2 SDRAM is $GV_{DD}$(typ) = 1.8 V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

**NOTE**

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

## 6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8343EA when $GV_{DD}$(typ) = 1.8 V.

**Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.71 | 1.89 | V | 1 |
| I/O reference voltage | $MV_{REF}$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF}$ – 0.04 | $MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.125 | $GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF}$ – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –9.9 | 9.9 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**

1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to equal 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ cannot exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal $MV_{REF}$. This rail should track variations in the DC level of $MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

Table 13 provides the DDR2 capacitance when $GV_{DD}$(typ) = 1.8 V.

**Table 13. DDR2 SDRAM Capacitance for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.090 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}$(typ) = 2.5 V.

**Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 2.5 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 2.375 | 2.625 | V | 1 |
| I/O reference voltage | $MV_{REF}$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF}$ – 0.04 | $MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.18 | $GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF}$ – 0.18 | V | — |
| Output leakage current | $I_{OZ}$ | –9.9 | –9.9 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.95 V) | $I_{OH}$ | –15.2 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.35 V) | $I_{OL}$ | 15.2 | — | mA | — |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MV_{REF}$. This rail should track variations in the DC level of $MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

Table 15 provides the DDR capacitance when $GV_{DD}$(typ) = 2.5 V.

**Table 15. DDR SDRAM Capacitance for $GV_{DD}$(typ) = 2.5 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 2.5 V ± 0.125 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.

Figure 7 shows the DDR SDRAM output timing diagram.

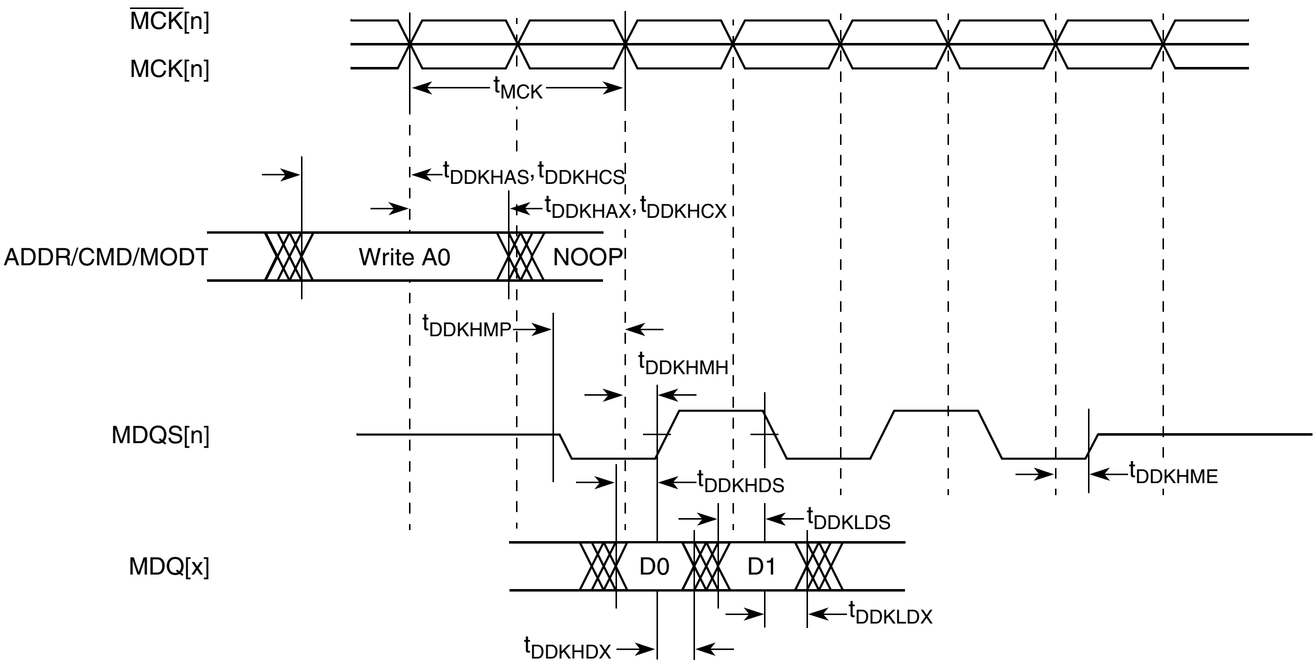



**Figure 7. DDR SDRAM Output Timing Diagram**

Figure 8 provides the AC test load for the DDR bus.

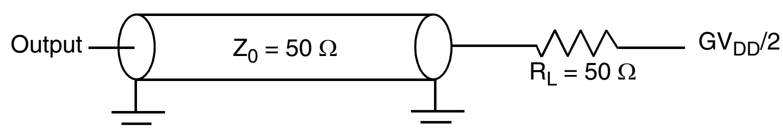



**Figure 8. DDR AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8343EA.

## 7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface of the MPC8343EA.

**Table 21. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current (0.8 V ≤ $V_{IN}$ ≤ 2 V) | $I_{IN}$ | — | ±5 | μA |

**Table 21. DUART DC Electrical Characteristics (continued)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

## 7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8343EA.

**Table 22. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | 256 | baud | — |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

**Notes:**

1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8$^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16$^{th}$ sample.

# 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

## 8.1 Three-Speed Ethernet Controller (TSEC)—MII/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII interface is defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, “Ethernet Management Interface Electrical Characteristics.”

### 8.2.1.2 MII Receive AC Timing Specifications

Table 26 provides the MII receive AC timing specifications.

**Table 26. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise (20%–80%) | $t_{MRXR}$ | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%–20%) | $t_{MRXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 provides the AC test load for TSEC.

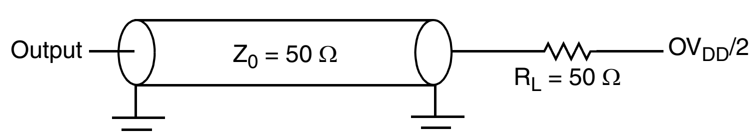



**Figure 10. TSEC AC Test Load**

Figure 11 shows the MII receive AC timing diagram.

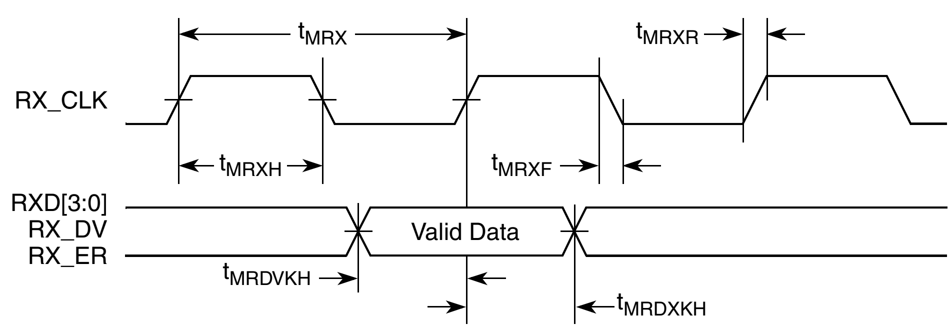



**Figure 11. MII Receive AC Timing Diagram**

# 9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8343EA.

## 9.1 USB DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the USB interface.

**Table 31. USB DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

## 9.2 USB AC Electrical Specifications

Table 32 describes the general timing parameters of the USB interface of the MPC8343EA.

**Table 32. USB General Timing Parameters (ULPI Mode Only)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| USB clock cycle time | $t_{USCK}$ | 15 | — | ns | 2–5 |
| Input setup to USB clock—all inputs | $t_{USIVKH}$ | 4 | — | ns | 2–5 |
| Input hold to USB clock—all inputs | $t_{USIXKH}$ | 1 | — | ns | 2–5 |
| USB clock to output valid—all outputs | $t_{USKHOV}$ | — | 7 | ns | 2–5 |
| Output hold from USB clock—all outputs | $t_{USKHOX}$ | 2 | — | ns | 2–5 |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{USIXKH}$ symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, $t_{USKHOX}$ symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}$/2 of the rising edge of the USB clock to 0.4 × $OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

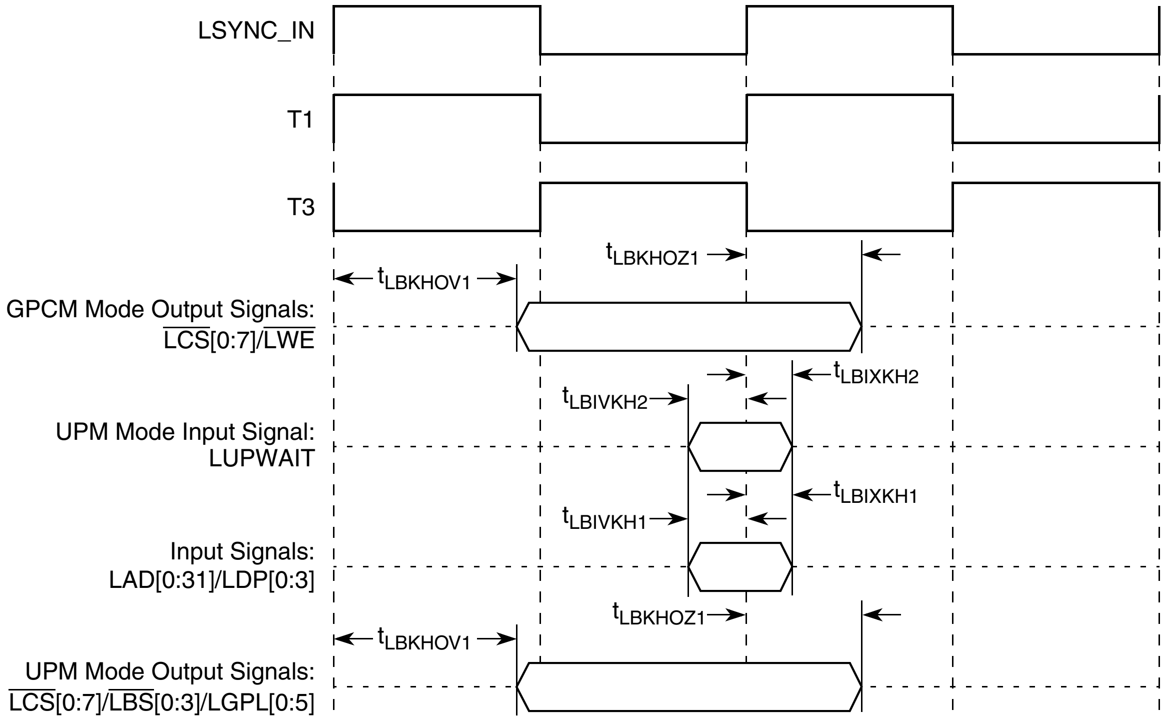



**Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)**

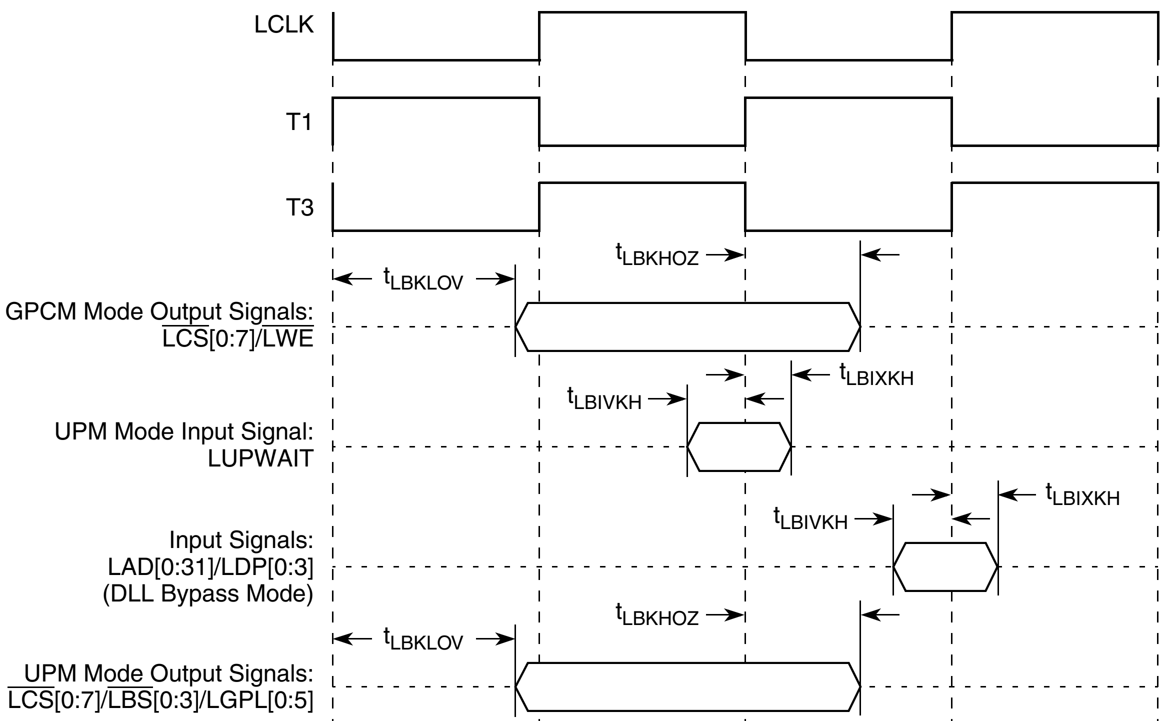



**Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)**

**Table 41. PCI AC Timing Specifications at 66 MHz[1] (continued)**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 3, 5 |

**Notes:**
1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

**Table 42. PCI AC Timing Specifications at 33 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 11 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 2 | — | ns | 2 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 2, 4 |

**Notes:**
1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 30 provides the AC test load for PCI.

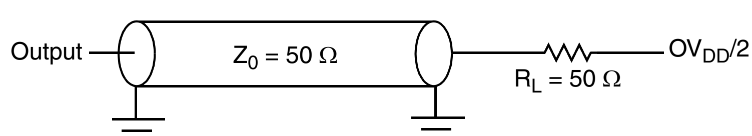



**Figure 30. PCI AC Test Load**

| | |
|---|---|
| Module height (typical) | 2.23 mm |
| Module height (minimum) | 2.00 mm |
| Solder balls | 62 Sn/36 Pb/2 Ag (ZQ package)<br>96.5 Sn/3.5Ag (VR package) |
| Ball diameter (typical) | 0.60 mm |

## 18.3 Pinout Listings

Table 51 provides the pin-out listing for the MPC8343EA, 620-PBGA package.

**Table 51. MPC8343EA (PBGA) Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| | **PCI** | | | |
| PCI1_INTA/IRQ_OUT | D20 | O | $OV_{DD}$ | 2 |
| PCI1_RESET_OUT | B21 | O | $OV_{DD}$ | — |
| PCI1_AD[31:0] | E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8 | I/O | $OV_{DD}$ | — |
| PCI1_C/BE[3:0] | A17, A14, A11, B10 | I/O | $OV_{DD}$ | — |
| PCI1_PAR | D13 | I/O | $OV_{DD}$ | — |
| PCI1_FRAME | B14 | I/O | $OV_{DD}$ | 5 |
| PCI1_TRDY | A13 | I/O | $OV_{DD}$ | 5 |
| PCI1_IRDY | E13 | I/O | $OV_{DD}$ | 5 |
| PCI1_STOP | C13 | I/O | $OV_{DD}$ | 5 |
| PCI1_DEVSEL | B13 | I/O | $OV_{DD}$ | 5 |
| PCI1_IDSEL | C17 | I | $OV_{DD}$ | — |
| PCI1_SERR | C12 | I/O | $OV_{DD}$ | 5 |
| PCI1_PERR | B12 | I/O | $OV_{DD}$ | 5 |
| PCI1_REQ[0] | A21 | I/O | $OV_{DD}$ | — |
| PCI1_REQ[1]/CPCI1_HS_ES | C19 | I | $OV_{DD}$ | — |
| PCI1_REQ[2:4] | C18, A19, E20 | I | $OV_{DD}$ | — |
| PCI1_GNT0 | B20 | I/O | $OV_{DD}$ | — |
| PCI1_GNT1/CPCI1_HS_LED | C20 | O | $OV_{DD}$ | — |
| PCI1_GNT2/CPCI1_HS_ENUM | B19 | O | $OV_{DD}$ | — |
| PCI1_GNT[3:4] | A20, E18 | O | $OV_{DD}$ | — |
| M66EN | L26 | I | $OV_{DD}$ | — |
| | **DDR SDRAM Memory Interface** | | | |
| MDQ[0:31] | AC25, AD27, AD25, AH27, AE28, AD26, AD24, AF27, AF25, AF28, AH24, AG26, AE25, AG25, AH26, AH25, AG22, AH22, AE21, AD19, AE22, AF23, AE19, AG20, AG19, AD17, AE16, AF16, AF18, AG18, AH17, AH16 | I/O | $GV_{DD}$ | — |

**Table 51. MPC8343EA (PBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LBCTL | H5 | O | $OV_{DD}$ | — |
| LALE | E3 | O | $OV_{DD}$ | — |
| LGPL0/LSDA10/cfg_reset_source0 | F4 | I/O | $OV_{DD}$ | — |
| LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1 | D2 | I/O | $OV_{DD}$ | — |
| LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$ | C1 | O | $OV_{DD}$ | — |
| LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2 | C2 | I/O | $OV_{DD}$ | — |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE | C3 | I/O | $OV_{DD}$ | 12 |
| LGPL5/cfg_clkin_div | B3 | I/O | $OV_{DD}$ | — |
| LCKE | E4 | O | $OV_{DD}$ | — |
| LCLK[0:2] | D4, A3, C4 | O | $OV_{DD}$ | — |
| LSYNC_OUT | U3 | O | $OV_{DD}$ | — |
| LSYNC_IN | Y2 | I | $OV_{DD}$ | — |
| **General Purpose I/O Timers** | | | | |
| GPIO1[0]/$\overline{\text{DMA\_DREQ0}}$/GTM1_TIN1/ GTM2_TIN2 | D27 | I/O | $OV_{DD}$ | — |
| GPIO1[1]/$\overline{\text{DMA\_DACK0}}$/$\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$ | E26 | I/O | $OV_{DD}$ | — |
| GPIO1[2]/$\overline{\text{DMA\_DDONE0}}$/ $\overline{\text{GTM1\_TOUT1}}$ | D28 | I/O | $OV_{DD}$ | — |
| GPIO1[3]/$\overline{\text{DMA\_DREQ1}}$/GTM1_TIN2/ GTM2_TIN1 | G25 | I/O | $OV_{DD}$ | — |
| GPIO1[4]/$\overline{\text{DMA\_DACK1}}$/ $\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$ | J24 | I/O | $OV_{DD}$ | — |
| GPIO1[5]/$\overline{\text{DMA\_DDONE1}}$/ $\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$ | F26 | I/O | $OV_{DD}$ | — |
| GPIO1[6]/$\overline{\text{DMA\_DREQ2}}$/GTM1_TIN3/ GTM2_TIN4 | E27 | I/O | $OV_{DD}$ | — |
| GPIO1[7]/$\overline{\text{DMA\_DACK2}}$/$\overline{\text{GTM1\_TGATE3}}$/ $\overline{\text{GTM2\_TGATE4}}$ | E28 | I/O | $OV_{DD}$ | — |
| GPIO1[8]/$\overline{\text{DMA\_DDONE2}}$/ $\overline{\text{GTM1\_TOUT3}}$ | H25 | I/O | $OV_{DD}$ | — |
| GPIO1[9]/$\overline{\text{DMA\_DREQ3}}$/GTM1_TIN4/ GTM2_TIN3 | F27 | I/O | $OV_{DD}$ | — |
| GPIO1[10]/$\overline{\text{DMA\_DACK3}}$/ $\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$ | K24 | I/O | $OV_{DD}$ | — |
| GPIO1[11]/$\overline{\text{DMA\_DDONE3}}$/ $\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$ | G26 | I/O | $OV_{DD}$ | — |

**Table 51. MPC8343EA (PBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| TSEC1_RX_DV | U24 | I | $LV_{DD1}$ | — |
| TSEC1_RX_ER/GPIO2[26] | L28 | I/O | $OV_{DD}$ | — |
| TSEC1_RXD[3:0] | W26, W24, Y28, Y27 | I | $LV_{DD1}$ | — |
| TSEC1_TX_CLK | N25 | I | $OV_{DD}$ | — |
| TSEC1_TXD[3:0] | V28, V27, V26, W28 | O | $LV_{DD1}$ | 10 |
| TSEC1_TX_EN | W27 | O | $LV_{DD1}$ | — |
| TSEC1_TX_ER/GPIO2[31] | N24 | I/O | $OV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 2)** | | | | |
| TSEC2_COL/GPIO1[21] | P28 | I/O | $OV_{DD}$ | — |
| TSEC2_CRS/GPIO1[22] | AC28 | I/O | $LV_{DD2}$ | — |
| TSEC2_GTX_CLK | AC27 | O | $LV_{DD2}$ | — |
| TSEC2_RX_CLK | AB25 | I | $LV_{DD2}$ | — |
| TSEC2_RX_DV/GPIO1[23] | AC26 | I/O | $LV_{DD2}$ | — |
| TSEC2_RXD[3:0]/GPIO1[13:16] | AA25, AA26, AA27, AA28 | I/O | $LV_{DD2}$ | — |
| TSEC2_RX_ER/GPIO1[25] | R25 | I/O | $OV_{DD}$ | — |
| TSEC2_TXD[3:0]/GPIO1[17:20] | AB26, AB27, AA24, AB28 | I/O | $LV_{DD2}$ | — |
| TSEC2_TX_ER/GPIO1[24] | R27 | I/O | $OV_{DD}$ | — |
| TSEC2_TX_EN/GPIO1[12] | AD28 | I/O | $LV_{DD2}$ | 3 |
| TSEC2_TX_CLK/GPIO1[30] | R26 | I/O | $OV_{DD}$ | — |
| **DUART** | | | | |
| UART_SOUT[1:2]/MSRCID[0:1]/ LSRCID[0:1] | B4, A4 | O | $OV_{DD}$ | — |
| UART_SIN[1:2]/MSRCID[2:3]/ LSRCID[2:3] | D5, C5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{UART\_CTS}}$[1]/MSRCID4/LSRCID4 | B5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{UART\_CTS}}$[2]/MDVAL/LDVAL | A5 | I/O | $OV_{DD}$ | — |
| $\overline{\text{UART\_RTS}}$[1:2] | D6, C6 | O | $OV_{DD}$ | — |
| **$I^2C$ interface** | | | | |
| IIC1_SDA | E5 | I/O | $OV_{DD}$ | 2 |
| IIC1_SCL | A6 | I/O | $OV_{DD}$ | 2 |
| IIC2_SDA | B6 | I/O | $OV_{DD}$ | 2 |
| IIC2_SCL | E7 | I/O | $OV_{DD}$ | 2 |

**Table 57. e300 Core PLL Configuration (continued)**

| RCWL[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider[1] |
|---|---|---|---|---|
| 0–1 | 2–5 | 6 | | |
| **00** | **0010** | 0 | 2:1 | 2 |
| **01** | **0010** | 0 | 2:1 | 4 |
| **10** | **0010** | 0 | 2:1 | 8 |
| **11** | **0010** | 0 | 2:1 | 8 |
| **00** | **0010** | 1 | 2.5:1 | 2 |
| **01** | **0010** | 1 | 2.5:1 | 4 |
| **10** | **0010** | 1 | 2.5:1 | 8 |
| **11** | **0010** | 1 | 2.5:1 | 8 |
| **00** | **0011** | 0 | 3:1 | 2 |
| **01** | **0011** | 0 | 3:1 | 4 |
| **10** | **0011** | 0 | 3:1 | 8 |
| **11** | **0011** | 0 | 3:1 | 8 |

1 Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

## 19.3 Suggested PLL Configurations

Table 58 shows suggested PLL configurations for 33 and 66 MHz input clocks, when CFG_CLKIN_DIV is low at reset.

**Table 58. Suggested PLL Configurations**

| Ref No.[1] | RCWL | | 266 MHz Device | | | 333 MHz Device | | | 400 MHz Device | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | SPMF | CORE PLL | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) |
| 33 MHz CLKIN/PCI_CLK Options | | | | | | | | | | | |
| **343** | **0011** | **1000011** | 33 | 100 | 150 | 33 | 100 | 150 | 33 | 100 | 150 |
| **324** | **0011** | **0100100** | 33 | 100 | 200 | 33 | 100 | 200 | 33 | 100 | 200 |
| **423** | **0100** | **0100011** | 33 | 133 | 200 | 33 | 133 | 200 | 33 | 133 | 200 |
| **622** | **0110** | **0100010** | 33 | 200 | 200 | 33 | 200 | 200 | 33 | 200 | 200 |
| **523** | **0101** | **0100011** | 33 | 166 | 250 | 33 | 166 | 250 | 33 | 166 | 250 |
| **424** | **0100** | **0100100** | 33 | 133 | 266 | 33 | 133 | 266 | 33 | 133 | 266 |
| **822** | **1000** | **0100010** | 33 | 266 | 266 | 33 | 266 | 266 | 33 | 266 | 266 |

**Table 58. Suggested PLL Configurations (continued)**

| Ref No.[1] | RCWL | | 266 MHz Device | | | 333 MHz Device | | | 400 MHz Device | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | SPMF | CORE PLL | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) |
| **326** | **0011** | **0100110** | — | | | 33 | 100 | 300 | 33 | 100 | 300 |
| **623** | **0110** | **0100011** | — | | | 33 | 200 | 300 | 33 | 200 | 300 |
| **922** | **1001** | **0100010** | — | | | 33 | 300 | 300 | 33 | 300 | 300 |
| **425** | **0100** | **0100101** | — | | | 33 | 133 | 333 | 33 | 133 | 333 |
| **524** | **0101** | **0100100** | — | | | 33 | 166 | 333 | 33 | 166 | 333 |
| **A22** | **1010** | **0100010** | — | | | 33 | 333 | 333 | 33 | 333 | 333 |
| **723** | **0111** | **0100011** | — | | | — | | | 33 | 233 | 350 |
| **604** | **0110** | **0000100** | — | | | — | | | 33 | 200 | 400 |
| **624** | **0110** | **0100100** | — | | | — | | | 33 | 200 | 400 |
| 823 | 1000 | 0100011 | — | | | — | | | 33 | 266 | 400 |
| **66 MHz CLKIN/PCI_CLK Options** | | | | | | | | | | | |
| **242** | **0010** | **1000010** | 66 | 133 | 133 | 66 | 133 | 133 | 66 | 133 | 133 |
| **322** | **0011** | **0100010** | 66 | 200 | 200 | 66 | 200 | 200 | 66 | 200 | 200 |
| **224** | **0010** | **0100100** | 66 | 133 | 266 | 66 | 133 | 266 | 66 | 133 | 266 |
| **422** | **0100** | **0100010** | 66 | 266 | 266 | 66 | 266 | 266 | 66 | 266 | 266 |
| **323** | **0011** | **0100011** | — | | | 66 | 200 | 300 | 66 | 200 | 300 |
| **223** | **0010** | **0100101** | — | | | 66 | 133 | 333 | 66 | 133 | 333 |
| **522** | **0101** | **0100010** | — | | | 66 | 333 | 333 | 66 | 333 | 333 |
| **304** | **0011** | **0000100** | — | | | — | | | 66 | 200 | 400 |
| **324** | **0011** | **0100100** | — | | | — | | | 66 | 200 | 400 |
| **403** | **0100** | **0000011** | — | | | — | | | 66 | 266 | 400 |
| **423** | **0100** | **0100011** | — | | | — | | | 66 | 266 | 400 |

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.
2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

## 21.7 Pull-Up Resistor Requirements

The MPC8343EA requires high resistance pull-up resistors (10 kΩ is recommended) on open-drain pins, including $I^2C$ pins, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, “PowerQUICC Design Checklist.”

# 22 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

**NOTE**

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8343EEC).

## 22.1 Part Numbers Fully Addressed by This Document

Table 62 shows an analysis of the Freescale part numbering nomenclature for the MPC8343EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration