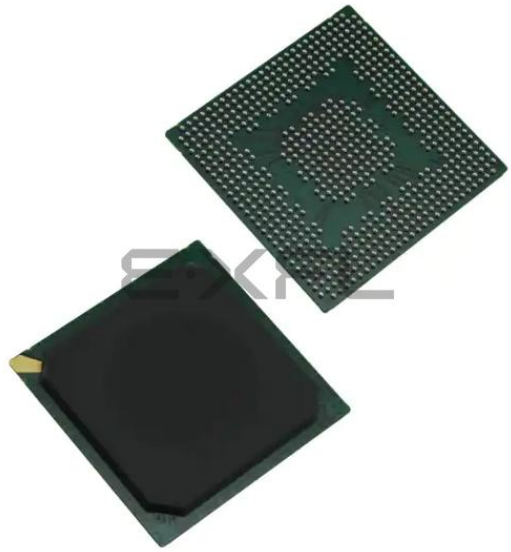

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (3) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 620-BBGA Exposed Pad |
| Supplier Device Package | 620-HBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8343ezqagd |

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI

- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - Public key execution unit (PKEU) :
    - RSA and Diffie-Hellman algorithms
    - Programmable field size up to 2048 bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511 bits
  - Data encryption standard (DES) execution unit (DEU)
    - DES and 3DES algorithms
    - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric-key cipher
    - Key lengths of 128, 192, and 256 bits
    - ECB, CBC, CCM, and counter (CTR) modes
  - XOR parity generation accelerator for RAID applications
  - ARC four execution unit (AFEU)
    - Stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - Message digest execution unit (MDEU)
    - SHA with 160-, 224-, or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Random number generator (RNG)
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Static and/or dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality
  - Complies with USB specification Rev. 2.0
  - Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints

  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects for eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard $I^2C$ interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from $I^2C$-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters

  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - 39 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8343EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | –0.3 to 1.32 | V | — |
| PLL supply voltage | $AV_{DD}$ | –0.3 to 1.32 | V | — |
| DDR and DDR2 DRAM I/O voltage | $GV_{DD}$ | –0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| Three-speed Ethernet I/O, MII management voltage | $LV_{DD}$ | –0.3 to 3.63 | V | — |
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | $OV_{DD}$ | –0.3 to 3.63 | V | — |

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8343EA for the 3.3-V signals, respectively.

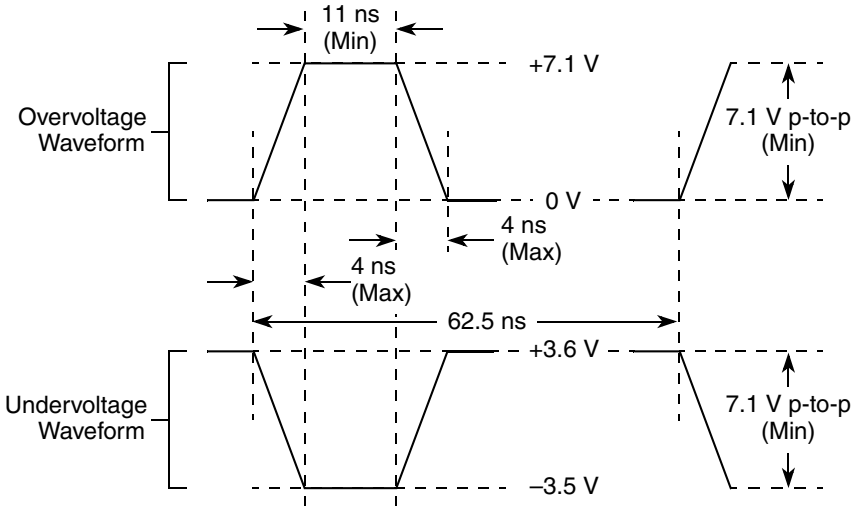


**Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling**

### 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

| Driver Type | Output Impedance (Ω) | Supply Voltage |
|---|---|---|
| Local bus interface utilities signals | 40 | $OV_{DD}$ = 3.3 V |
| PCI signals (not including PCI output clocks) | 25 | |
| PCI output clocks (including PCI_SYNC_OUT) | 40 | |
| DDR signal | 18 | $GV_{DD}$ = 2.5 V |
| DDR2 signal | 18<br>36 (half-strength mode) | $GV_{DD}$ = 1.8 V |
| TSEC/10/100 signals | 40 | $LV_{DD}$ = 2.5/3.3 V |
| DUART, system control, $I^2C$, JTAG, USB | 40 | $OV_{DD}$ = 3.3 V |
| GPIO signals | 40 | $OV_{DD}$ = 3.3 V,<br>$LV_{DD}$ = 2.5/3.3 V |

## 2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8343EA.

### 2.2.1 Power-Up Sequencing

MPC8343EAdoes not require the core supply voltage ($V_{DD}$ and $AV_{DD}$) and I/O supply voltages ($GV_{DD}$, $LV_{DD}$, and $OV_{DD}$) to be applied in any particular order. During the power ramp up, before the power

## 5.2 RESET AC Electrical Characteristics

Table 10 provides the reset initialization AC timing specifications of the MPC8343EA.

**Table 10. RESET Initialization Timing Specifications**

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8343EA is in PCI host mode | 32 | — | $t_{CLKIN}$ | 2 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8343EA is in PCI agent mode | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output) | 512 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output) | 16 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8343EA is in PCI host mode | 4 | — | $t_{CLKIN}$ | 2 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8343EA is in PCI agent mode | 4 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | — |
| Time for the MPC8343EA to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 3 |
| Time for the MPC8343EA to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$ | 1 | — | $t_{PCI\_SYNC\_IN}$ | 1, 3 |

**Notes:**

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
2. $t_{CLKIN}$ is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

**Table 11. PLL and DLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| PLL lock times | — | 100 | μs | — |
| DLL lock times | 7680 | 122,880 | csb_clk cycles | 1, 2 |

**Notes:**

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, “Clocking.”

# 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8343EA. Note that DDR SDRAM is $GV_{DD}$(typ) = 2.5 V and DDR2 SDRAM is $GV_{DD}$(typ) = 1.8 V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

**NOTE**

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

## 6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8343EA when $GV_{DD}$(typ) = 1.8 V.

**Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.71 | 1.89 | V | 1 |
| I/O reference voltage | $MV_{REF}$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF}$ – 0.04 | $MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.125 | $GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF}$ – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –9.9 | 9.9 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**

1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to equal 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ cannot exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal $MV_{REF}$. This rail should track variations in the DC level of $MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

Table 13 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

**Table 13. DDR2 SDRAM Capacitance for $GV_{DD}(typ) = 1.8$ V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. $GV_{DD} = 1.8$ V ± 0.090 V, f = 1 MHz, $T_A = 25°C$, $V_{OUT} = GV_{DD}/2$, $V_{OUT}$ (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5$ V.

**Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5$ V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 2.375 | 2.625 | V | 1 |
| I/O reference voltage | $MV_{REF}$ | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF} - 0.04$ | $MV_{REF} + 0.04$ | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF} + 0.18$ | $GV_{DD} + 0.3$ | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF} - 0.18$ | V | — |
| Output leakage current | $I_{OZ}$ | –9.9 | –9.9 | μA | 4 |
| Output high current ($V_{OUT} = 1.95$ V) | $I_{OH}$ | –15.2 | — | mA | — |
| Output low current ($V_{OUT} = 0.35$ V) | $I_{OL}$ | 15.2 | — | mA | — |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to be equal to $0.5 \times GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MV_{REF}$. This rail should track variations in the DC level of $MV_{REF}$.
4. Output leakage is measured with all outputs disabled, $0 \text{ V} \le V_{OUT} \le GV_{DD}$.

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

**Table 15. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5$ V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. $GV_{DD} = 2.5$ V ± 0.125 V, f = 1 MHz, $T_A = 25°C$, $V_{OUT} = GV_{DD}/2$, $V_{OUT}$ (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for $MV_{REF}$.

**Table 16. Current Draw Characteristics for $MV_{REF}$**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Current draw for $MV_{REF}$ | $I_{MVREF}$ | — | 500 | μA | 1 |

**Note:**
1. The voltage regulator for $MV_{REF}$ must supply up to 500 μA current.

## 6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

### 6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}$(typ) = 1.8 V.

**Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.25 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.25 | — | V | — |

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}$(typ) = 2.5 V.

**Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface**

At recommended operating conditions with $GV_{DD}$ of 2.5 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.31 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.31 | — | V | — |

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of (1.8 or 2.5 V) ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Controller Skew for MDQS—MDQ/MECC/MDM | $t_{CISKEW}$ | | | ps | 1, 2 |
| 400 MHz | | –600 | 600 | | 3 |
| 333 MHz | | –750 | 750 | | — |

**Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications (continued)**

At recommended operating conditions with $GV_{DD}$ of (1.8 or 2.5 V) ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| 266 MHz | | –750 | 750 | | — |
| 200 MHz | | –750 | 750 | | — |

**Notes:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$. This can be determined by the equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$; where T is the clock period and abs ($t_{CISKEW}$) is the absolute value of $t_{CISKEW}$.
3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the $t_{DISKEW}$ timing parameter.

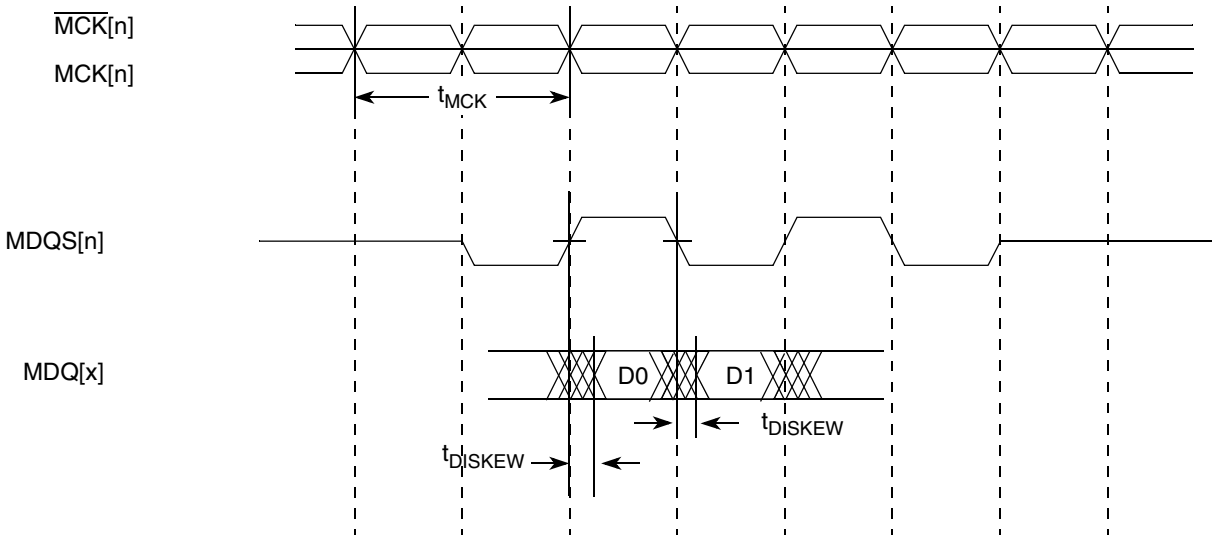


**Figure 5. DDR Input Timing Diagram**

## 6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

**Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of (1.8 or 2.5 V) ± 5%.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, (MCK[n]/MCK[n] crossing) | $t_{MCK}$ | 7.5 | 10 | ns | 2 |
| ADDR/CMD/MODT output setup with respect to MCK | $t_{DDKHAS}$ | | | ns | 3 |
| 400 MHz | | 1.95 | — | | |
| 333 MHz | | 2.40 | — | | |
| 266 MHz | | 3.15 | — | | |
| 200 MHz | | 4.20 | — | | |

Figure 7 shows the DDR SDRAM output timing diagram.

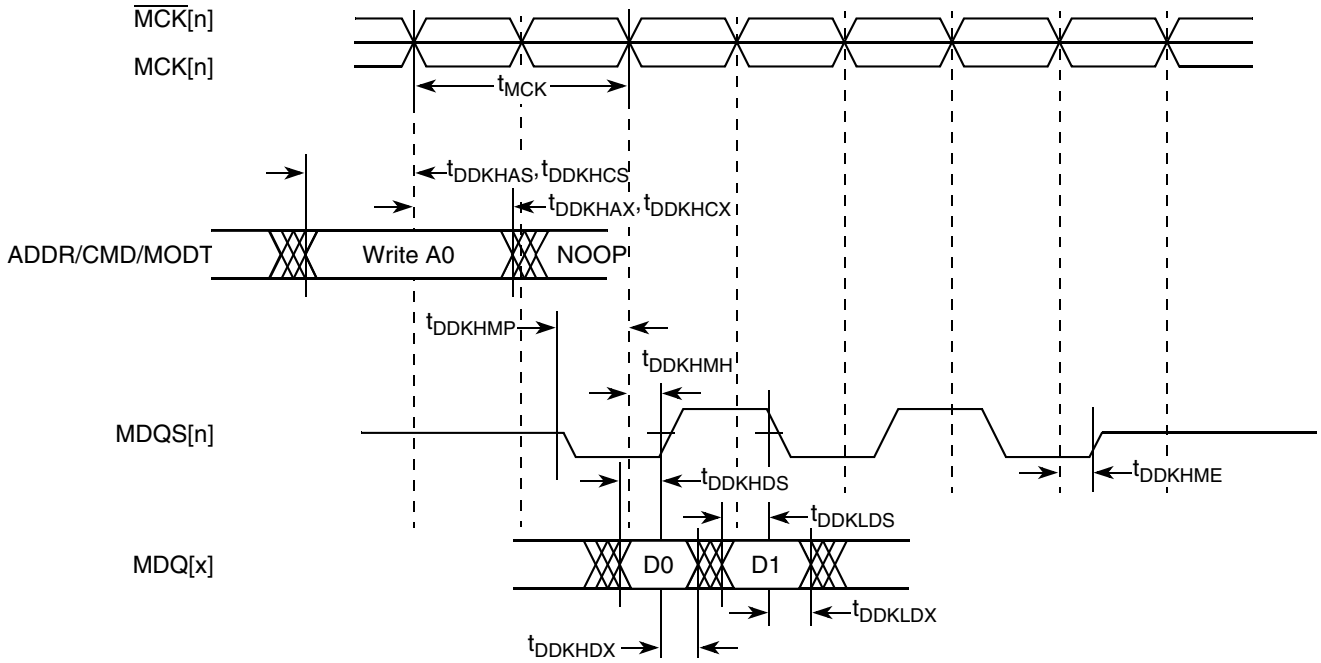


**Figure 7. DDR SDRAM Output Timing Diagram**

Figure 8 provides the AC test load for the DDR bus.

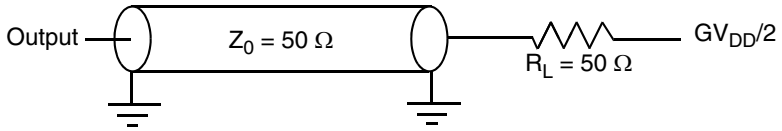


**Figure 8. DDR AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8343EA.

## 7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface of the MPC8343EA.

**Table 21. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current (0.8 V ≤ $V_{IN}$ ≤ 2 V) | $I_{IN}$ | — | ±5 | μA |

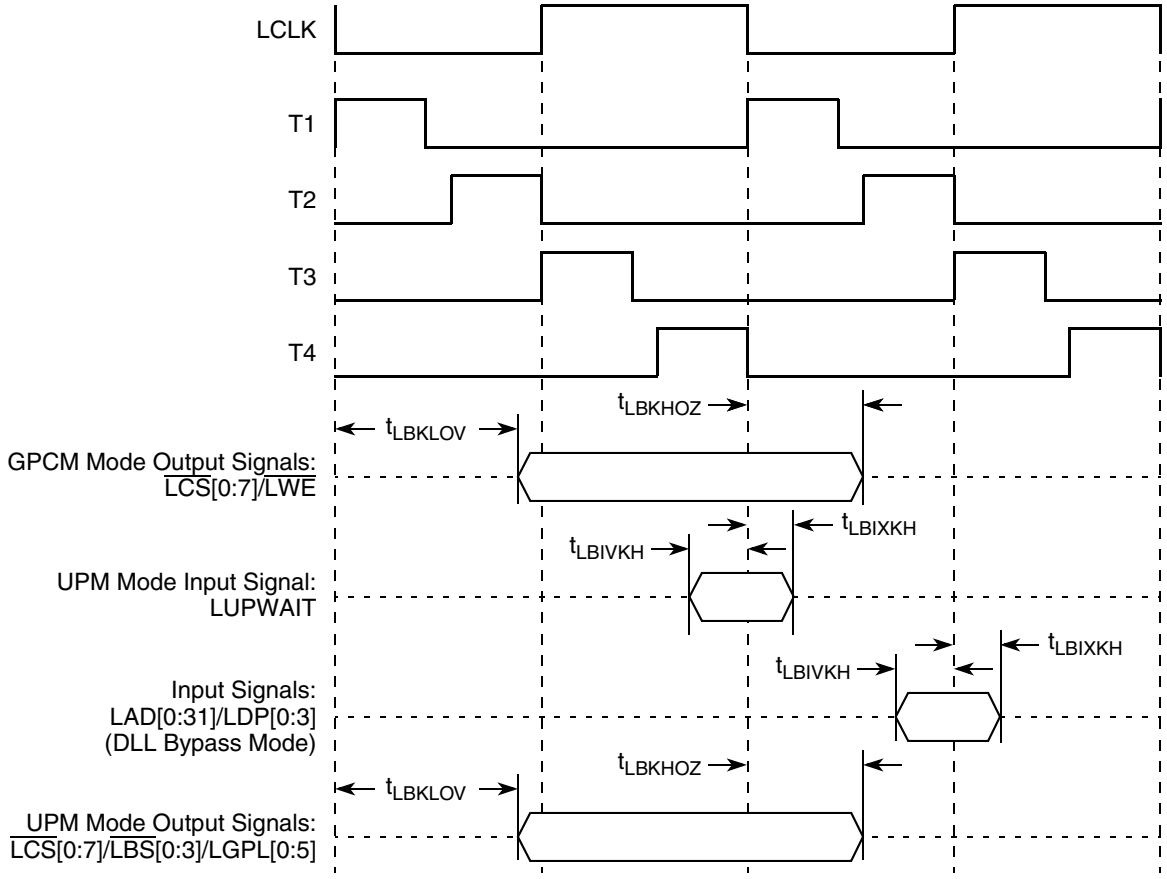


**Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)**

**Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)**

At recommended operating conditions (see Table 2).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>2<br>2 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design and characterization.

Figure 23 provides the AC test load for TDO and the boundary-scan outputs of the MPC8343EA.

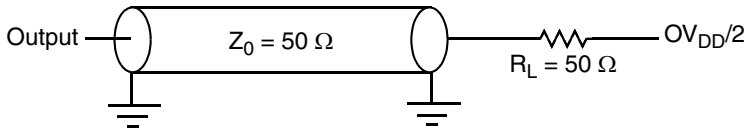


**Figure 23. AC Test Load for the JTAG Interface**

Figure 24 provides the JTAG clock input timing diagram.

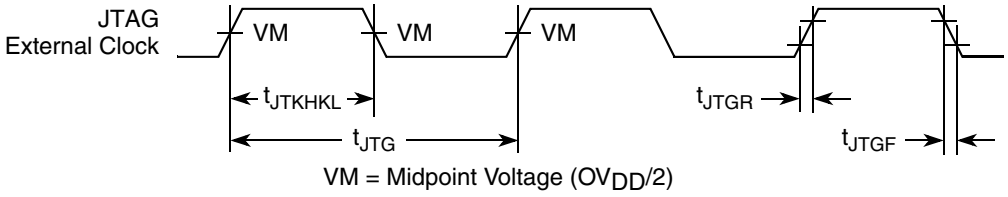


**Figure 24. JTAG Clock Input Timing Diagram**

Figure 25 provides the $\overline{\text{TRST}}$ timing diagram.

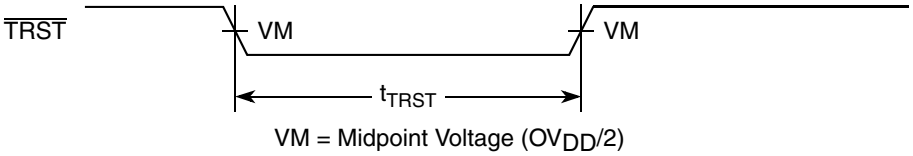


**Figure 25. $\overline{\text{TRST}}$ Timing Diagram**

# 12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8343EA.

## 12.1 I²C DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the I²C interface of the MPC8343EA.

**Table 38. I²C DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 10%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | $0.2 \times OV_{DD}$ | V | 1 |
| Output fall time from $V_{IH}$(min) to $V_{IL}$(max) with a bus capacitance from 10 to 400 pF | $t_{I2KLKV}$ | $20 + 0.1 \times C_B$ | 250 | ns | 2 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max) | $I_I$ | –10 | 10 | μA | 4 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. $C_B$ = capacitance of one bus line in pF.
3. Refer to the *MPC8349EA Integrated Host Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 12.2 I²C AC Electrical Specifications

Table 39 provides the AC timing parameters for the I²C interface of the MPC8343EA. Note that all values refer to $V_{IH}$(min) and $V_{IL}$(max) levels (see Table 38).

**Table 39. I²C AC Electrical Specifications**

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |
| Data hold time:CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | —<br>0[2] | —<br>0.9[3] | μs |

**Table 51. MPC8343EA (PBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| MECC[0:4]/MSRCID[0:4] | AG13, AE14, AH12, AH10, AE15 | I/O | $GV_{DD}$ | — |
| MECC[5]/MDVAL | AH14 | I/O | $GV_{DD}$ | — |
| MECC[6:7] | AE13, AH11 | I/O | $GV_{DD}$ | — |
| MDM[0:3] | AG28, AG24, AF20, AG17 | O | $GV_{DD}$ | — |
| MDM[8] | AG12 | O | $GV_{DD}$ | — |
| MDQS[0:3] | AE27, AE26, AE20, AH18 | I/O | $GV_{DD}$ | — |
| MDQS[8] | AH13 | I/O | $GV_{DD}$ | — |
| MBA[0:1] | AF10, AF11 | O | $GV_{DD}$ | — |
| MA[0:14] | AF13, AF15, AG16, AD16, AF17, AH20, AH19, AH21, AD18, AG21, AD13, AF21, AF22, AE1, AA5 | O | $GV_{DD}$ | — |
| $\overline{\text{MWE}}$ | AD10 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | AF7 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | AG6 | O | $GV_{DD}$ | — |
| $\overline{\text{MCS}}$[0:3] | AE7, AH7, AH4, AF2 | O | $GV_{DD}$ | — |
| MCKE[0:1] | AG23, AH23 | O | $GV_{DD}$ | 3 |
| MCK[0:3] | AH15, AE24, AE2, AF14 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:3] | AG15, AD23, AE3, AG14 | O | $GV_{DD}$ | — |
| MODT[0:3] | AG5, AD4, AH6, AF4 | O | $GV_{DD}$ | — |
| MBA[2] | AD22 | O | $GV_{DD}$ | — |
| MDIC0 | AG11 | I/O | — | 9 |
| MDIC1 | AF12 | I/O | — | 9 |
| **Local Bus Controller Interface** | | | | |
| LAD[0:31] | T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3 | I/O | $OV_{DD}$ | — |
| LDP[0]/$\overline{\text{CKSTOP\_OUT}}$ | H1 | I/O | $OV_{DD}$ | — |
| LDP[1]/$\overline{\text{CKSTOP\_IN}}$ | K5 | I/O | $OV_{DD}$ | — |
| LDP[2]/$\overline{\text{LCS}}$[4] | H2 | I/O | $OV_{DD}$ | — |
| LDP[3]/$\overline{\text{LCS}}$[5] | G1 | I/O | $OV_{DD}$ | — |
| LA[27:31] | J4, H3, G2, F1, G3 | O | $OV_{DD}$ | — |
| $\overline{\text{LCS}}$[0:3] | J5, H4, F2, E1 | O | $OV_{DD}$ | — |
| $\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3] | F3, G4, D1, E2 | O | $OV_{DD}$ | — |

**Table 51. MPC8343EA (PBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **USB** | | | | |
| DR_D0_ENABLEN | C28 | I/O | $OV_{DD}$ | — |
| DR_D1_SER_TXD | F25 | I/O | $OV_{DD}$ | — |
| DR_D2_VMO_SE0 | B28 | I/O | $OV_{DD}$ | — |
| DR_D3_SPEED | C27 | I/O | $OV_{DD}$ | — |
| DR_D4_DP | D26 | I/O | $OV_{DD}$ | — |
| DR_D5_DM | E25 | I/O | $OV_{DD}$ | — |
| DR_D6_SER_RCV | C26 | I/O | $OV_{DD}$ | — |
| DR_D7_DRVVBUS | D25 | I/O | $OV_{DD}$ | — |
| DR_SESS_VLD_NXT | B26 | I | $OV_{DD}$ | — |
| DR_XCVR_SEL_DPPULLUP | E24 | I/O | $OV_{DD}$ | — |
| DR_STP_SUSPEND | A27 | O | $OV_{DD}$ | — |
| DR_RX_ERROR_PWRFAULT | C25 | I | $OV_{DD}$ | — |
| DR_TX_VALID_PCTL0 | A26 | O | $OV_{DD}$ | — |
| DR_TX_VALIDH_PCTL1 | B25 | O | $OV_{DD}$ | — |
| DR_CLK | A25 | I | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | |
| $\overline{\text{MCP\_OUT}}$ | E8 | O | $OV_{DD}$ | 2 |
| $\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12] | J28 | I/O | $OV_{DD}$ | — |
| $\overline{\text{IRQ}}$[1:5]/GPIO2[13:17] | K25, J25, H26, L24, G27 | I/O | $OV_{DD}$ | — |
| $\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT | G28 | I/O | $OV_{DD}$ | — |
| $\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN | J26 | I/O | $OV_{DD}$ | — |
| **Ethernet Management Interface** | | | | |
| EC_MDC | Y24 | O | $LV_{DD1}$ | — |
| EC_MDIO | Y25 | I/O | $LV_{DD1}$ | 11 |
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | Y26 | I | $LV_{DD1}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_COL/GPIO2[20] | M26 | I/O | $OV_{DD}$ | — |
| TSEC1_CRS/GPIO2[21] | U25 | I/O | $LV_{DD1}$ | — |
| TSEC1_GTX_CLK | V24 | O | $LV_{DD1}$ | 3 |
| TSEC1_RX_CLK | U26 | I | $LV_{DD1}$ | — |

As shown in Figure 37, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + RCWL[DDRCM])$$

*ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + RCWL[LBIUCM])$$

*lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 52 specifies which units have a configurable clock frequency.

**Table 52. Configurable Clock Units**

| Unit | Default Frequency | Options |
|---|---|---|
| TSEC1 | *csb_clk/3* | Off, *csb_clk, csb_clk/2, csb_clk/3* |
| TSEC2, $I^2C1$ | *csb_clk/3* | Off, *csb_clk, csb_clk/2, csb_clk/3* |
| Security core | *csb_clk/3* | Off, *csb_clk,* csb_clk/2, *csb_clk/3* |
| USB DR, USB MPH | *csb_clk/3* | Off, csb_clk, csb_clk/2, *csb_clk/3* |
| PCI and DMA complex | *csb_clk* | Off, *csb_clk* |

All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 22.1, “Part Numbers Fully Addressed by This Document,” for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

Table 53 provides the operating frequencies for the MPC8343EA PBGA under recommended operating conditions.

**Table 53. Operating Frequencies for PBGA**

| Parameter[1] | 266 MHz | 333 MHz | 400 MHz | Unit |
|---|---|---|---|---|
| e300 core frequency (*core_clk*) | 200–266 | 200–333 | 200–400 | MHz |
| Coherent system bus frequency (*csb_clk*) | 100–266 | | | MHz |
| DDR1 memory bus frequency (MCK)[2] | 100–133 | | | MHz |
| DDR2 memory bus frequency (MCK)[3] | 100–133 | | | MHz |
| Local bus frequency (LCLK*n*)[4] | 16.67–133 | | | MHz |
| PCI input frequency (CLKIN or PCI_CLK) | 25–66 | | | MHz |
| Security core maximum internal operating frequency | 133 | | | MHz |
| USB_DR, USB_MPH maximum internal operating frequency | 133 | | | MHz |

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

2 The DDR data rate is 2× the DDR memory bus frequency.

3 The DDR data rate is 2× the DDR memory bus frequency.

4 The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBIUCM]).

## 19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 54 shows the multiplication factor encodings for the system PLL.

**Table 54. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | × 16 |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111 | × 7 |
| 1000 | × 8 |
| 1001 | × 9 |
| 1010 | × 10 |

**Table 54. System PLL Multiplication Factors (continued)**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 1011 | × 11 |
| 1100 | × 12 |
| 1101 | × 13 |
| 1110 | × 14 |
| 1111 | × 15 |

As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 55 and Table 56 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

**Table 55. CSB Frequency Options for Host Mode**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0010 | 2 : 1 | | | | 133 |
| Low | 0011 | 3 : 1 | | | 100 | 200 |
| Low | 0100 | 4 : 1 | | 100 | 133 | 266 |
| Low | 0101 | 5 : 1 | | 125 | 166 | 333 |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |

**Table 58. Suggested PLL Configurations (continued)**

| Ref No.[1] | RCWL | | 266 MHz Device | | | 333 MHz Device | | | 400 MHz Device | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | SPMF | CORE PLL | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) |
| **326** | **0011** | **0100110** | — | | | 33 | 100 | 300 | 33 | 100 | 300 |
| **623** | **0110** | **0100011** | — | | | 33 | 200 | 300 | 33 | 200 | 300 |
| **922** | **1001** | **0100010** | — | | | 33 | 300 | 300 | 33 | 300 | 300 |
| **425** | **0100** | **0100101** | — | | | 33 | 133 | 333 | 33 | 133 | 333 |
| **524** | **0101** | **0100100** | — | | | 33 | 166 | 333 | 33 | 166 | 333 |
| **A22** | **1010** | **0100010** | — | | | 33 | 333 | 333 | 33 | 333 | 333 |
| **723** | **0111** | **0100011** | — | | | — | | | 33 | 233 | 350 |
| **604** | **0110** | **0000100** | — | | | — | | | 33 | 200 | 400 |
| **624** | **0110** | **0100100** | — | | | — | | | 33 | 200 | 400 |
| 823 | 1000 | 0100011 | — | | | — | | | 33 | 266 | 400 |
| **66 MHz CLKIN/PCI_CLK Options** | | | | | | | | | | | |
| **242** | **0010** | **1000010** | 66 | 133 | 133 | 66 | 133 | 133 | 66 | 133 | 133 |
| **322** | **0011** | **0100010** | 66 | 200 | 200 | 66 | 200 | 200 | 66 | 200 | 200 |
| **224** | **0010** | **0100100** | 66 | 133 | 266 | 66 | 133 | 266 | 66 | 133 | 266 |
| **422** | **0100** | **0100010** | 66 | 266 | 266 | 66 | 266 | 266 | 66 | 266 | 266 |
| **323** | **0011** | **0100011** | — | | | 66 | 200 | 300 | 66 | 200 | 300 |
| **223** | **0010** | **0100101** | — | | | 66 | 133 | 333 | 66 | 133 | 333 |
| **522** | **0101** | **0100010** | — | | | 66 | 333 | 333 | 66 | 333 | 333 |
| **304** | **0011** | **0000100** | — | | | — | | | 66 | 200 | 400 |
| **324** | **0011** | **0100100** | — | | | — | | | 66 | 200 | 400 |
| **403** | **0100** | **0000011** | — | | | — | | | 66 | 266 | 400 |
| **423** | **0100** | **0100011** | — | | | — | | | 66 | 266 | 400 |

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

### 20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_A$ = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D$ = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

### 20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter ($\Psi_{JT}$) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_T$ = thermocouple temperature on top of package (°C)

$\Psi_{JT}$ = junction-to-ambient thermal resistance (°C/W)

$P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so