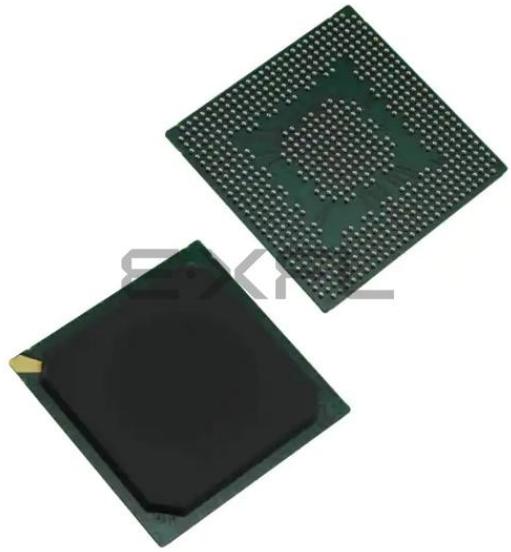

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8343ezqagdb

  - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
  - DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
  - Full error checking and correction (ECC) support
  - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep-mode support for SDRAM self refresh
  - Auto refresh
  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 RGMII, IEEE Std. 802.3z RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- PCI interface
  - Designed to comply with *PCI Specification Revision 2.3*
  - Data bus width:
    - 32-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities
  - PCI agent mode on PCI interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration supporting five masters on PCI
  - Accesses to all PCI address spaces
  - Parity supported
  - Selectable hardware-enforced coherency

  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects for eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters

supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

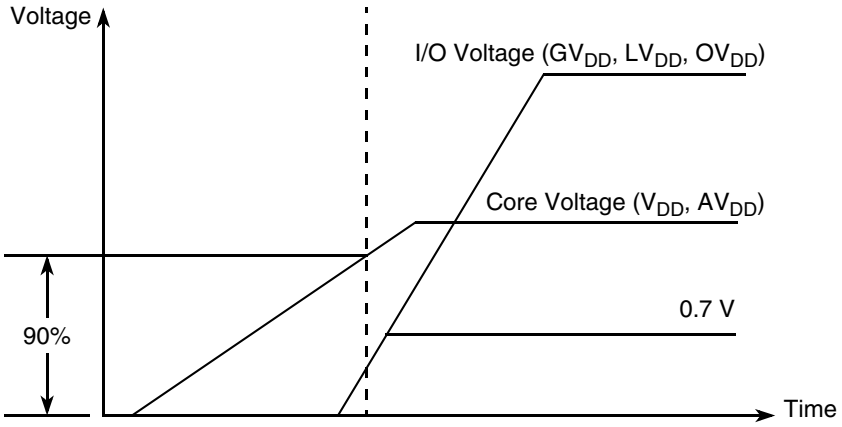


Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

3 Power Characteristics

The estimated typical power dissipation for the MPC8343EA device is shown in Table 4.

Table 4. MPC8343EA Power Dissipation[1]

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T_J = 65	Typical[2,3]	Maximum[4]	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W

1 The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.

2 Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

3 Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

4 Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

Table 5 shows the estimated typical I/O power dissipation for MPC8343EA.

Table 5. MPC8343EA Typical I/O Power Dissipation

Interface	Parameter	DDR2 GV_{DD} (1.8 V)	DDR1 GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	200 MHz, 32 bits	0.31	0.42	—	—	—	W	—
	266 MHz, 32 bits	0.35	0.5	—	—	—	W	—
PCI I/O load = 30 pF	33 MHz, 32 bits	—	—	0.04	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
Local bus I/O load = 25 pF	167 MHz, 32 bits	—	—	0.34	—	—	W	—
	133 MHz, 32 bits	—	—	0.27	—	—	W	—
	83 MHz, 32 bits	—	—	0.17	—	—	W	—
	66 MHz, 32 bits	—	—	0.14	—	—	W	—
	50 MHz, 32 bits	—	—	0.11	—	—	W	—
TSEC I/O load = 25 pF	MII	—	—		0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—		0.06	—	W	
	RGMII or RTBI	—	—		—	0.04	W	
USB	12 MHz	—	—	0.01	—	—	W	—
	480 MHz	—	—	0.2	—	—	W	—
Other I/O		—	—	0.01	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8343EA.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	$0 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8343EA. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

NOTE

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8343EA when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to equal 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
266 MHz		–750	750		—
200 MHz		–750	750		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$; where T is the clock period and abs (t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

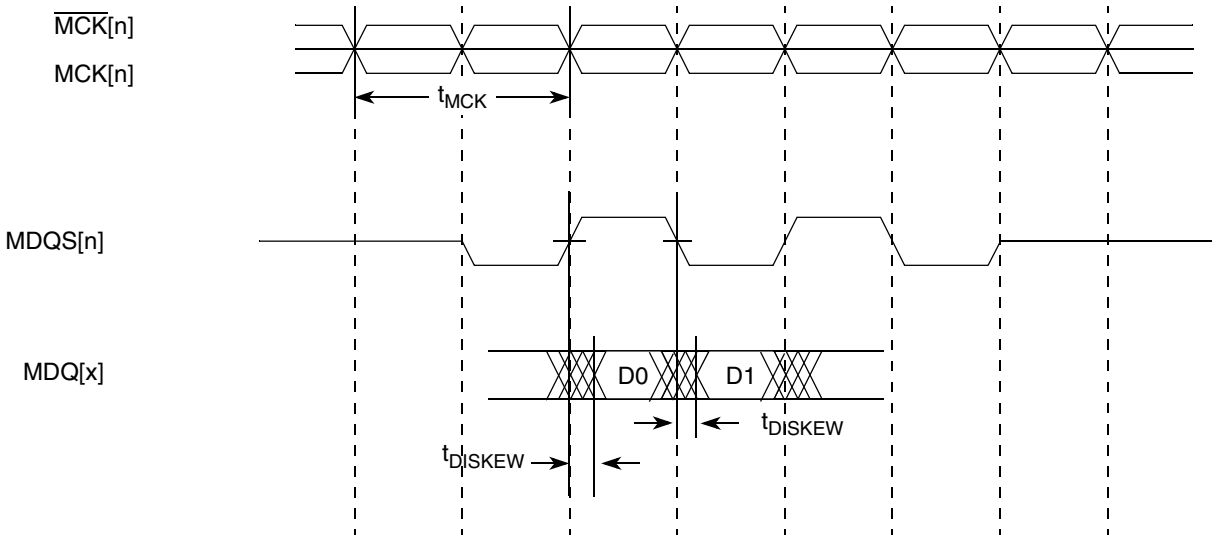


Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t_{MCK}	7.5	10	ns	2
ADDR/CMD/MODT output setup with respect to MCK	t_{DDKHAS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		

8.2 MII, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RGMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

Table 25 provides the MII transmit AC timing specifications.

Table 25. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the MII transmit AC timing diagram.

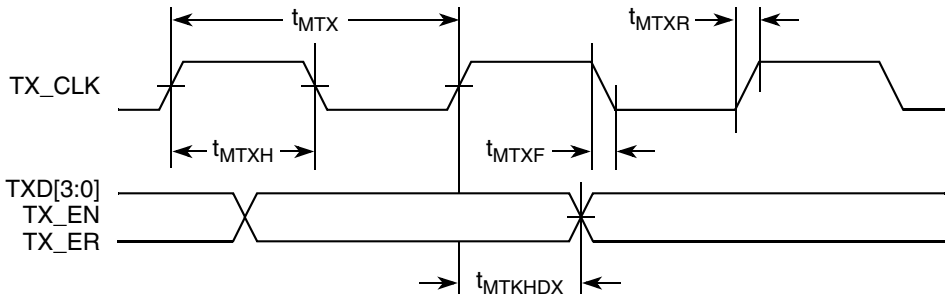


Figure 9. MII Transmit AC Timing Diagram

Table 30. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 13 shows the MII management AC timing diagram.

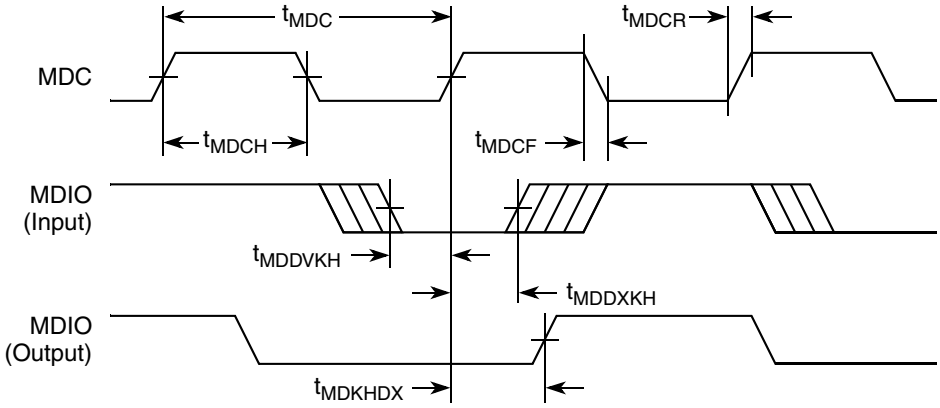


Figure 13. MII Management Interface Timing Diagram

Figure 14 and Figure 15 provide the AC test load and signals for the USB, respectively.

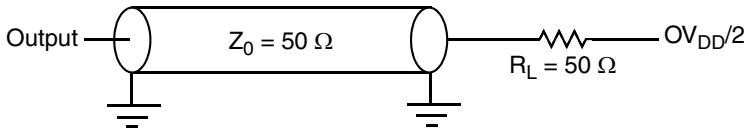


Figure 14. USB AC Test Load

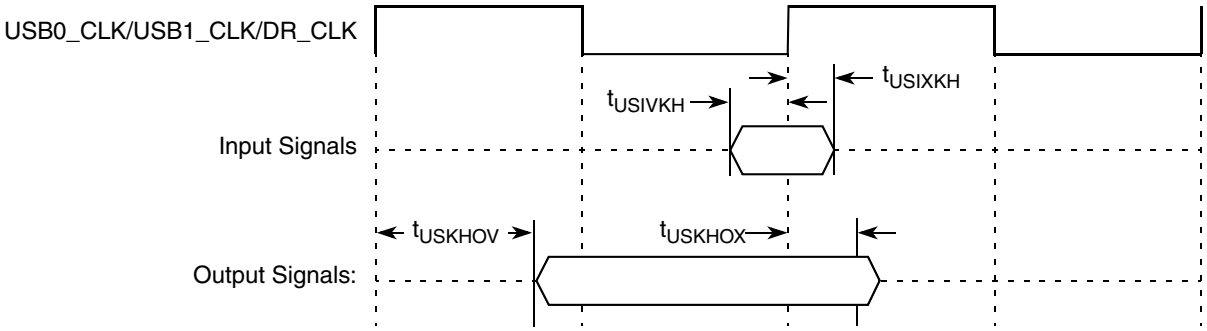


Figure 15. USB Signals

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8343EA.

10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

Table 33. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

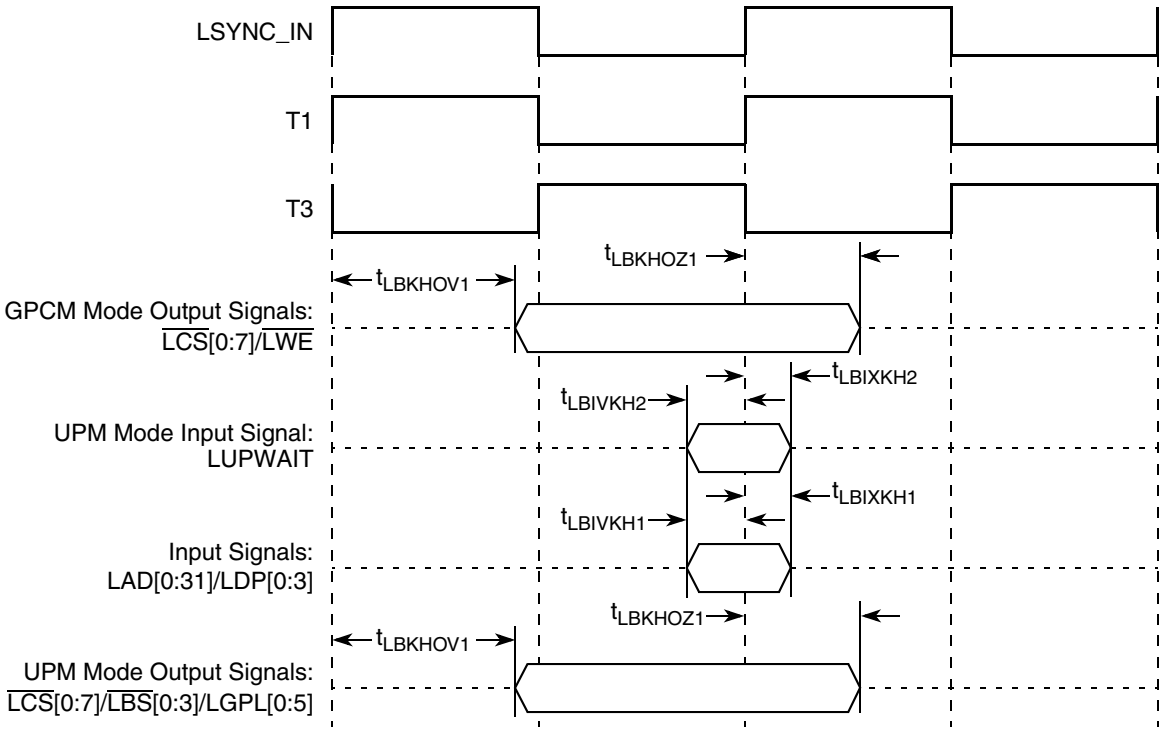


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

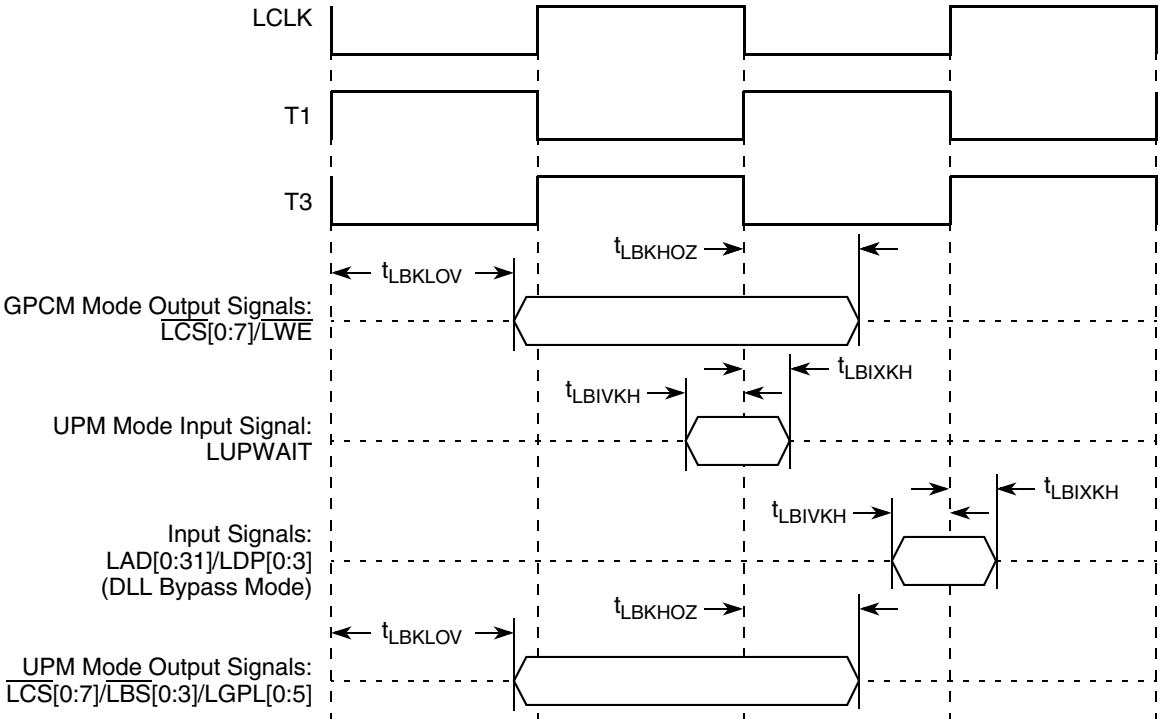


Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LBCTL	H5	O	OV_{DD}	—
LALE	E3	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV_{DD}	—
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV_{DD}	—
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV_{DD}	—
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV_{DD}	12
LGPL5/cfg_clkin_div	B3	I/O	OV_{DD}	—
LCKE	E4	O	OV_{DD}	—
LCLK[0:2]	D4, A3, C4	O	OV_{DD}	—
LSYNC_OUT	U3	O	OV_{DD}	—
LSYNC_IN	Y2	I	OV_{DD}	—
General Purpose I/O Timers				
GPIO1[0]/$\overline{\text{DMA\_DREQ0}}$/GTM1_TIN1/ GTM2_TIN2	D27	I/O	OV_{DD}	—
GPIO1[1]/$\overline{\text{DMA\_DACK0}}$/$\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$	E26	I/O	OV_{DD}	—
GPIO1[2]/$\overline{\text{DMA\_DDONE0}}$/ $\overline{\text{GTM1\_TOUT1}}$	D28	I/O	OV_{DD}	—
GPIO1[3]/$\overline{\text{DMA\_DREQ1}}$/GTM1_TIN2/ GTM2_TIN1	G25	I/O	OV_{DD}	—
GPIO1[4]/$\overline{\text{DMA\_DACK1}}$/ $\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	J24	I/O	OV_{DD}	—
GPIO1[5]/$\overline{\text{DMA\_DDONE1}}$/ $\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	F26	I/O	OV_{DD}	—
GPIO1[6]/$\overline{\text{DMA\_DREQ2}}$/GTM1_TIN3/ GTM2_TIN4	E27	I/O	OV_{DD}	—
GPIO1[7]/$\overline{\text{DMA\_DACK2}}$/$\overline{\text{GTM1\_TGATE3}}$/ $\overline{\text{GTM2\_TGATE4}}$	E28	I/O	OV_{DD}	—
GPIO1[8]/$\overline{\text{DMA\_DDONE2}}$/ $\overline{\text{GTM1\_TOUT3}}$	H25	I/O	OV_{DD}	—
GPIO1[9]/$\overline{\text{DMA\_DREQ3}}$/GTM1_TIN4/ GTM2_TIN3	F27	I/O	OV_{DD}	—
GPIO1[10]/$\overline{\text{DMA\_DACK3}}$/ $\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	K24	I/O	OV_{DD}	—
GPIO1[11]/$\overline{\text{DMA\_DDONE3}}$/ $\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	G26	I/O	OV_{DD}	—

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Signals				
$AV_{DD}1$	C15	Power for e300 PLL (1.2 V)	$AV_{DD}1$	—
$AV_{DD}2$	U1	Power for system PLL (1.2 V)	$AV_{DD}2$	—
$AV_{DD}3$	AF9	Power for DDR DLL (1.2 V)	—	—
$AV_{DD}4$	U2	Power for LBIU DLL (1.2 V)	$AV_{DD}4$	—
GND	A2, B1, B2, D10, D18, E6, E14, E22, F9, F12, F15, F18, F21, F24, G5, H6, J23, L4, L6, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, M16, M17, M18, M23, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, P24, R5, R23, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U6, U11, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V23, V25, W4, Y6, AA23, AB24, AC5, AC8, AC11, AC14, AC17, AC20, AD9, AD15, AD21, AE12, AE18, AF3, AF26	—	—	—
GV_{DD}	U9, V9, W10, W19, Y11, Y12, Y14, Y15, Y17, Y18, AA6, AB5, AC9, AC12, AC15, AC18, AC21, AC24, AD6, AD8, AD14, AD20, AE5, AE11, AE17, AG2, AG27	Power for DDR DRAM I/O voltage (2.5 V)	GV_{DD}	—
LV_{DD1}	U20, W25	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5V, 3.3V)	LV_{DD1}	—
LV_{DD2}	V20, Y23	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV_{DD2}	—
V_{DD}	J11, J12, J15, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L18, L19, M10, M19, N10, N19, P9, P10, P19, R10, R19, R20, T10, T19, U10, U19, V10, V11, V18, V19, W11, W12, W13, W14, W15, W16, W17, W18	Power for core (1.2 V)	V_{DD}	—

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
OV_{DD}	B27, D3, D11, D19, E15, E23, F5, F8, F11, F14, F17, F20, G24, H23, H24, J6, J14, J17, J18, K4, L9, L20, L23, L25, M6, M9, M20, P5, P20, P23, R6, R9, R24, U23, V4, V6	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	—
MVREF1	AF19	I	DDR reference voltage	—
MVREF2	AE10	I	DDR reference voltage	—
No Connection				
NC	A22, A23, A24, B22, B23, B24, C21, C22, C23, C24, D21, D22, D23, D24, E21, M27, M28, N26, N27, N28, P25, P26, P27, R28, T24, T25, T26, T27, T28, U27, U28, Y3, Y4, Y5, AA1, AA2, AA3, AA4, AB1, AB2, AB3, AB4, AC1, AC2, AC3, AC4, AD1, AD2, AD3, AD5, AD7, AD11, AD12, AE4, AE6, AE8, AE9, AE23, AF1, AF5, AF6, AF8, AF24, AG1, AG3, AG4, AG7, AG8, AG9, AG10, AH2, AH3, AH5, AH8, AH9, V5, V2, V1	—	—	—

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must be always be tied to GND.
7. This pin must always be pulled up to OV_{DD}.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
11. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to LV_{DD1}.
12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pull up on LGPL4 is required.

As shown in Figure 37, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + RCWL[DDRCM])$$

ddr_clk is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + RCWL[LBIUCM])$$

lbiu_clk is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 52 specifies which units have a configurable clock frequency.

Table 52. Configurable Clock Units

Unit	Default Frequency	Options
TSEC1	*csb_clk/3*	Off, *csb_clk, csb_clk/2, csb_clk/3*
TSEC2, I^2C1	*csb_clk/3*	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security core	*csb_clk/3*	Off, *csb_clk,* csb_clk/2, *csb_clk/3*
USB DR, USB MPH	*csb_clk/3*	Off, csb_clk, csb_clk/2, *csb_clk/3*
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 22.1, “Part Numbers Fully Addressed by This Document,” for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

Table 55. CSB Frequency Options for Host Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

1 CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Table 56. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8343EA.

21.1 System Clocking

The MPC8343EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, “Core PLL Configuration.”

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The AV_{DD} level should always equal to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 38, one to each of the four AV_{DD} pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV_{DD} pin being supplied. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 38 shows the PLL power supply filter circuit.

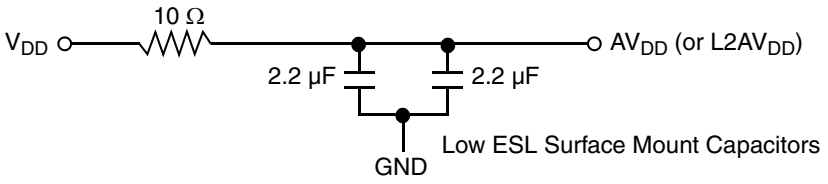


Figure 38. PLL Power Supply Filter Circuit

$OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

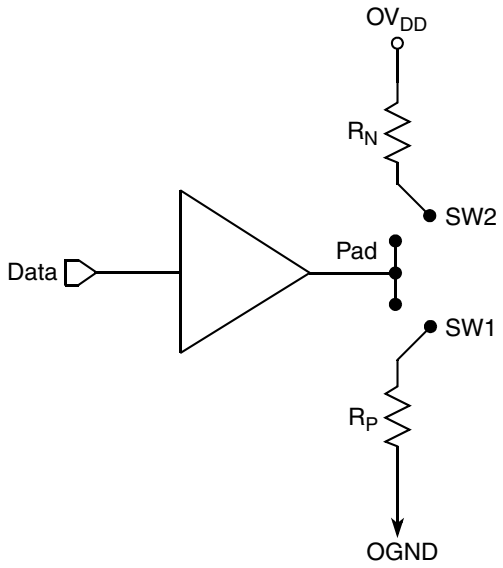


Figure 39. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1 \div (1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1 \div V_2 - 1)$. The drive current is then $I_{source} = V_1 \div R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 61. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	W
Differential	NA	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

21.6 Configuration Pin Multiplexing

The MPC8343EA power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.

parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 62. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature[1] Range**	**Package[2]**	**Processor Frequency[3]**	**Platform Frequency**	**Revision Level**
MPC	8343	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400	D = 266	B = 3.1

Notes:
1. For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266 and up to with a platform frequency of 333
2. See Section 18, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

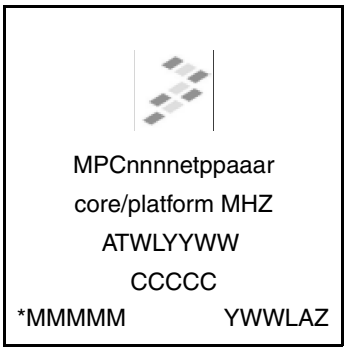
Table 63 shows the SVR settings by device and package type.

Table 63. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8343EA	PBGA	8056_0030
MPC8343A	PBGA	8057_0030

22.2 Part Marking

Parts are marked as in the example shown in Figure 40.



PBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 40. Freescale Part Marking for PBGA Devices

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