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NXP USA Inc. - KMPC8343ZQAGD Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	•
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8343zqagd

Email: info@E-XFL.COM

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NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8343EA.



Figure 1. MPC8343EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 400 MHz
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
 - Programmable timing supporting DDR1 and DDR2 SDRAM
 - 32- bit data interface, up to 266 MHz data rate



Overview

- Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- DRAM chip configurations from 64 Mbits to 1 Gbit with $\times 8/\times 16$ data ports
- Full error checking and correction (ECC) support
- Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep-mode support for SDRAM self refresh
- Auto refresh
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3TM, 802.3uTM, 820.3xTM, 802.3zTM, 802.3acTM standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 RGMII, IEEE Std. 802.3z RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- PCI interface
 - Designed to comply with PCI Specification Revision 2.3
 - Data bus width:
 - 32-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities
 - PCI agent mode on PCI interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration supporting five masters on PCI
 - Accesses to all PCI address spaces
 - Parity supported
 - Selectable hardware-enforced coherency

Parameter	Symbol	Recommended Value	Unit	Notes
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	_

Table 2. Recommended Operating Conditions (continued)

Note:

¹ GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8343EA.



Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$



DDR and DDR2 SDRAM

Table 13 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	_
Output leakage current	I _{OZ}	-9.9	-9.9	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	—	mA	_
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	—	mA	_

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.



DDR and DDR2 SDRAM

Table 16 provides the current draw characteristics for MV_{REF} .

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV _{REF}	I _{MVREF}		500	μA	1

Note:

1. The voltage regulator for MV_{REF} must supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 \pm 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V	_
AC input high voltage	V _{IH}	MV _{REF} + 0.25	_	V	

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 V$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 \pm 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	_
AC input high voltage	V _{IH}	MV _{REF} + 0.31	_	V	_

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t _{CISKEW}			ps	1, 2
400 MHz		-600	600		3
333 MHz		-750	750		—



DDR and DDR2 SDRAM

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_DD of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
ADDR/CMD/MODT output hold with respect to MCK	t _{DDKHAX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output setup with respect to MCK	t _{DDKHCS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output hold with respect to MCK	t _{DDKHCX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	^t DDKHDS, t _{DDKLDS}			ps	5
400 MHz		700	—		
333 MHz		775	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	t _{DDKHDX,} t _{DDKLDX}			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5\times t_{MCK}+0.6$	ns	6

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DDR and DDR2 SDRAM

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
- 4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual for the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).



Figure 6. Timing Diagram for t_{DDKHMH}



Table 30. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

- 2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 13 shows the MII management AC timing diagram.



Figure 13. MII Management Interface Timing Diagram



JTAG

Table 36. JTAG Interface DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Мах	Unit
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA. Table 37 provides the JTAG AC timing specifications as defined in Figure 24 through Figure 27.

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter		Symbol ²	Min	Мах	Unit	Notes
JTAG external clock frequer	ncy of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle ti	me	t _{JTG}	30	—	ns	—
JTAG external clock pulse w	vidth measured at 1.4 V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and	d fall times	t _{JTGR} , t _{JTGF}	0	2	ns	—
TRST assert time		t _{TRST}	25	_	ns	3
Input setup times:	Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 4		ns	4
Input hold times:	Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	10 10		ns	4
Valid times:	Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	2 2	11 11	ns	5
Output hold times:	Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	2 2		ns	5



Figure 26 provides the boundary-scan timing diagram.



Figure 26. Boundary-Scan Timing Diagram





Figure 27. Test Access Port Timing Diagram



PCI

Table 41. PCI AC Timing Specifications at 66 MHz¹ (continued)

Parameter	Symbol ²	Min	Мах	Unit	Notes
Input hold from clock	t _{PCIXKH}	0	—	ns	3, 5

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.}
- 3. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

Table 42. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output valid	^t PCKHOV	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	—	ns	2
Clock to output high impedance	t _{PCKHOZ}	-	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	_	ns	2, 4

Notes:

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

Figure 30 provides the AC test load for PCI.



Figure 30. PCI AC Test Load

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>



16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the external interrupt pins.

Table 47. IPIC DC Electrical Characteristics¹

Parameter	Symbol	Condition	Min	Мах	Unit	Notes
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	_	-0.3	0.8	V	—
Input current	I _{IN}	—	—	±5	μA	—
Output low voltage	V _{OL}	l _{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V	2

Notes:

1. This table applies for pins $\overline{IRQ}[0:7]$, \overline{IRQ}_{OUT} , and \overline{MCP}_{OUT} .

2. $\overline{IRQ_OUT}$ and $\overline{MCP_OUT}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 48 provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.

 IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 49 provides the SPI DC electrical characteristics.

Table 49. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V



Figure 34 and Figure 35 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 34 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 35 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8343EA is available in a plastic ball grid array (PBGA). See Section 18.1, "Package Parameters for the MPC8343EA PBGA," and Section 18.2, "Mechanical Dimensions for the MPC8343EA PBGA."

18.1 Package Parameters for the MPC8343EA PBGA

The package parameters are as provided in the following list. The package type is $29 \text{ mm} \times 29 \text{ mm}$, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm



Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
	USB						
DR_D0_ENABLEN	C28	I/O	OV _{DD}				
DR_D1_SER_TXD	F25	I/O	OV _{DD}				
DR_D2_VMO_SE0	B28	I/O	OV _{DD}				
DR_D3_SPEED	C27	I/O	OV _{DD}				
DR_D4_DP	D26	I/O	OV _{DD}				
DR_D5_DM	E25	I/O	OV _{DD}				
DR_D6_SER_RCV	C26	I/O	OV _{DD}	_			
DR_D7_DRVVBUS	D25	I/O	OV _{DD}	_			
DR_SESS_VLD_NXT	B26	I	OV _{DD}	_			
DR_XCVR_SEL_DPPULLUP	E24	I/O	OV _{DD}	_			
DR_STP_SUSPEND	A27	0	OV _{DD}	_			
DR_RX_ERROR_PWRFAULT	C25	I	OV _{DD}	_			
DR_TX_VALID_PCTL0	A26	0	OV _{DD}	_			
DR_TX_VALIDH_PCTL1	B25	0	OV _{DD}	_			
DR_CLK	A25	I	OV _{DD}	_			
	Programmable Interrupt Controller		•				
MCP_OUT	E8	0	OV _{DD}	2			
IRQ0/MCP_IN/GPIO2[12]	J28	I/O	OV _{DD}	_			
IRQ[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV _{DD}	_			
IRQ[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV _{DD}	_			
IRQ[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV _{DD}	_			
	Ethernet Management Interface						
EC_MDC	Y24	0	LV _{DD1}	_			
EC_MDIO	Y25	I/O	LV _{DD1}	11			
Gigabit Reference Clock							
EC_GTX_CLK125	Y26	I	LV _{DD1}	_			
Three-S	peed Ethernet Controller (Gigabit Ethe	rnet 1)					
TSEC1_COL/GPIO2[20]	M26	I/O	OV _{DD}	_			
TSEC1_CRS/GPIO2[21]	U25	I/O	LV _{DD1}				
TSEC1_GTX_CLK	V24	0	LV _{DD1}	3			
TSEC1_RX_CLK	U26	I	LV _{DD1}	_			

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)



Package and Pin Listings

Table 51 MPC83/3EA			na (contin	(bau
TADIE 31. INF CO343EA	(FDGA)) Fillout Listii	ig (contin	ueu)

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
	SPI		-	•			
SPIMOSI/LCS[6]	D7	I/O	OV _{DD}	—			
SPIMISO/LCS[7]	C7	I/O	OV _{DD}	—			
SPICLK	B7	I/O	OV _{DD}	—			
SPISEL	A7	I	OV _{DD}	—			
	Clocks						
PCI_CLK_OUT[0:2]	Y1, W3, W2	0	OV _{DD}	—			
PCI_CLK_OUT[3]/LCS[6]	W1	0	OV _{DD}	—			
PCI_CLK_OUT[4]/LCS[7]	V3	0	OV _{DD}	—			
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV _{DD}	—			
PCI_SYNC_OUT	U5	0	OV _{DD}	3			
RTC/PIT_CLOCK	E9	I	OV _{DD}	—			
CLKIN	W5	I	OV _{DD}	—			
	JTAG						
тск	H27	I	OV _{DD}	—			
TDI	H28	I	OV _{DD}	4			
TDO	M24	0	OV _{DD}	3			
TMS	J27	I	OV _{DD}	4			
TRST	K26	I	OV _{DD}	4			
	Test						
TEST	F28	I	OV _{DD}	6			
TEST_SEL	Т3	I	OV _{DD}	7			
	РМС						
QUIESCE	K27	0	OV _{DD}	—			
System Control							
PORESET	K28	I	OV _{DD}	—			
HRESET	M25	I/O	OV _{DD}	1			
SRESET	L27	I/O	OV _{DD}	2			
	Thermal Management	_					
THERM0	B15	I	_	8			



Clocking

I	RCWL[COREPLI	-]	aara alki aab alk Datia		
0–1	2–5	6	<i>core_cik</i> : <i>csb_cik</i> Ralio	VCO Divider	
00	0010	0	2:1	2	
01	0010	0	2:1	4	
10	0010	0	2:1	8	
11	0010	0	2:1	8	
00	0010	1	2.5:1	2	
01	0010	1	2.5:1	4	
10	0010	1	2.5:1	8	
11	0010	1	2.5:1	8	
00	0011	0	3:1	2	
01	0011	0	3:1	4	
10	0011	0	3:1	8	
11	0011	0	3:1	8	

Table 57. e300 Core PLL Configuration (continued)

¹ Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

19.3 Suggested PLL Configurations

Table 58 shows suggested PLL configurations for 33 and 66 MHz input clocks, when CFG_CLKIN_DIV is low at reset.

	RCWL		266 MHz Device		333 MHz Device			400 MHz Device			
Ref No. ¹	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
33 MHz CLKIN/PCI_CLK Options											
343	0011	1000011	33	100	150	33	100	150	33	100	150
324	0011	0100100	33	100	200	33	100	200	33	100	200
423	0100	0100011	33	133	200	33	133	200	33	133	200
622	0110	0100010	33	200	200	33	200	200	33	200	200
523	0101	0100011	33	166	250	33	166	250	33	166	250
424	0100	0100100	33	133	266	33	133	266	33	133	266
822	1000	0100010	33	266	266	33	266	266	33	266	266

Table 58. Suggested PLL Configurations



	RCWL		266 MHz Device			333 MHz Device			400 MHz Device		
Ref No. ¹	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
326	0011	0100110				33	100	300	33	100	300
623	0110	0100011	—			33	200	300	33	200	300
922	1001	0100010		_		33	300	300	33	300	300
425	0100	0100101	—			33	133	333	33	133	333
524	0101	0100100	—			33	166	333	33	166	333
A22	1010	0100010	_			33	333	333	33	333	333
723	0111	0100011	_			—			33	233	350
604	0110	0000100	_			—			33	200	400
624	0110	0100100	—			_			33	200	400
823	1000	0100011	_				—		33	266	400
				66 N	IHz CLKIN	/PCI_CLK	Options				
242	0010	1000010	66	133	133	66	133	133	66	133	133
322	0011	0100010	66	200	200	66	200	200	66	200	200
224	0010	0100100	66	133	266	66	133	266	66	133	266
422	0100	0100010	66	266	266	66	266	266	66	266	266
323	0011	0100011		_		66	200	300	66	200	300
223	0010	0100101	—			66	133	333	66	133	333
522	0101	0100010	_			66	333	333	66	333	333
304	0011	0000100	_		—		66	200	400		
324	0011	0100100	—		—		66	200	400		
403	0100	0000011		_		—		66	266	400	
423	0100	0100011	_			—			66	266	400

Table 58. Suggested PLI	- Configurations	(continued)
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¹ The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.
 ² The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.



Thermal

that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W) $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 60 shows heat sink thermal resistance for PBGA of the MPC8343EA.

Table 60. Heat Sink and Thermal Resistance of MPC8343EA (PBGA)

Heat Sink Assuming Thermal Grease		29 $ imes$ 29 mm PBGA	
neat Sink Assuming merinal Grease	AITTOW	Thermal Resistance	
AAVID $30 \times 30 \times 9.4$ mm pin fin	Natural convection	13.5	
AAVID $30 \times 30 \times 9.4$ mm pin fin	1 m/s	9.6	
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	8.8	
AAVID 31 \times 35 \times 23 mm pin fin	Natural convection	11.3	
AAVID 31 \times 35 \times 23 mm pin fin	1 m/s	8.1	
AAVID 31 \times 35 \times 23 mm pin fin	2 m/s	7.5	
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	9.1	
Wakefield, $53\times53\times25$ mm pin fin	1 m/s	7.1	
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	6.5	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	10.1	



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Interface	material	vendors	include	the	tollowing:

6	
Chomerics, Inc.	781-935-4850
77 Dragon Ct.	
Woburn, MA 01801	
Internet: www.chomerics.com	
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 T_J = junction temperature (°C) T_C = case temperature of the package (°C)



 $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.



Figure 39. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = (1 \div (1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1 \div V_2 - 1)$. The drive current is then $I_{source} = V_1 \div R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R _N	42 Target	25 Target	42 Target	20 Target	Z ₀	W
R _P	42 Target	25 Target	42 Target	20 Target	Z ₀	W
Differential	NA	NA	NA	NA	Z _{DIFF}	W

Table 61. Impedance Characteristics

Note: Nominal supply voltages. See Table 1, $T_i = 105^{\circ}C$.

21.6 Configuration Pin Multiplexing

The MPC8343EA power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.