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NXP USA Inc. - MPC8343CVRADD Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8343cvradd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

- Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- DRAM chip configurations from 64 Mbits to 1 Gbit with $\times 8/\times 16$ data ports
- Full error checking and correction (ECC) support
- Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep-mode support for SDRAM self refresh
- Auto refresh
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3TM, 802.3uTM, 820.3xTM, 802.3zTM, 802.3acTM standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 RGMII, IEEE Std. 802.3z RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- PCI interface
 - Designed to comply with PCI Specification Revision 2.3
 - Data bus width:
 - 32-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities
 - PCI agent mode on PCI interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration supporting five masters on PCI
 - Accesses to all PCI address spaces
 - Parity supported
 - Selectable hardware-enforced coherency



Overview

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i[®], iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
 - XOR parity generation accelerator for RAID applications
 - ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints



DDR and DDR2 SDRAM

Table 13 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	_
Output leakage current	I _{OZ}	-9.9	-9.9	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	—	mA	_
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	—	mA	_

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.



DDR and DDR2 SDRAM

Table 16 provides the current draw characteristics for MV_{REF} .

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV _{REF}	I _{MVREF}		500	μA	1

Note:

1. The voltage regulator for MV_{REF} must supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 \pm 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V	_
AC input high voltage	V _{IH}	MV _{REF} + 0.25	_	V	

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 V$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 \pm 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	_
AC input high voltage	V _{IH}	MV _{REF} + 0.31	_	V	_

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t _{CISKEW}			ps	1, 2
400 MHz		-600	600		3
333 MHz		-750	750		—



DDR and DDR2 SDRAM

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol	Min	Max	Unit	Notes
266 MHz		-750	750		
200 MHz		-750	750		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: t_{DISKEW} = ± (T/4 – abs (t_{CISKEW})); where T is the clock period and abs (t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.



Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	7.5	10	ns	2
ADDR/CMD/MODT output setup with respect to MCK	t _{DDKHAS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		



Table 21. DUA	RT DC Electrica	Characteristics	(continued)
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Parameter	Symbol	Min	Мах	Unit
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8343EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16		2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—MII/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII interface is defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."



Ethernet: Three-Speed Ethernet, MII Management

Table 28. MII Management DC Electrical Characteristics Powered at 2.5 V (continued)

Parameter	Symbol	Conditions	Min	Мах	Unit
Input high current	I _{IH}	$V_{IN}^{1} = LV_{DD}$	—	10	μA
Input low current	IIL	$V_{IN} = LV_{DD}$	-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 29. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	LV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	$LV_{DD} = Min$	2.10	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—		2.00	-	V
Input low voltage	V _{IL}	—		—	0.80	V
Input high current	I _{IH}	LV _{DD} = Max	$V_{IN}^{1} = 2.1 V$	—	40	μA
Input low current	۱ _{IL}	LV _{DD} = Max	V _{IN} = 0.5 V	-600	_	μA

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 30 provides the MII management AC timing specifications.

Table 30. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	—	400	—	ns	—
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t _{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t _{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0	—	—	ns	—
MDC rise time	t _{MDCR}			10	ns	_



Table 30. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

- 2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 13 shows the MII management AC timing diagram.



Figure 13. MII Management Interface Timing Diagram



10.2 Local Bus AC Electrical Specification

Table 34 and Table 35 describe the general timing parameters of the local bus interface of the MPC8343EA.

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	_	ns	2
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	1.5	_	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	2.2	_	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.0	_	ns	3, 4
LUPWAIT Input hold from local bus clock	t _{LBIXKH2}	1.0	_	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	_	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7
Local bus clock to LALE rise	t _{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	4.5	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	1	_	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}	_	3.8	ns	8

Table 34. Local Bus General Timing Parameters—DLL On

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

- 2. All timings are in reference to the rising edge of LSYNC_IN.
- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
- 6. t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
- 8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	15	—	ns	2
Input setup to local bus clock	t _{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t _{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	—	ns	7
Local bus clock to output valid	t _{LBKLOV}	_	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}	—	4	ns	8

Table 35. Local Bus General Timing Parameters—DLL Bypass⁹

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

- 2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
- 6. t_{LBOTOT2} should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.the
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is not set and when the load on the LALE output pin equals to the load on the LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 16 provides the AC test load for the local bus.



Figure 16. Local Bus C Test Load







Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

11.1 JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	OV _{DD} - 0.3	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V



Table 37. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t_{TCLK}.

5. Non-JTAG signal output timing with respect to t_{TCLK}.

6. Guaranteed by design and characterization.

Figure 23 provides the AC test load for TDO and the boundary-scan outputs of the MPC8343EA.



Figure 23. AC Test Load for the JTAG Interface

Figure 24 provides the JTAG clock input timing diagram.



Figure 24. JTAG Clock Input Timing Diagram

Figure 25 provides the $\overline{\text{TRST}}$ timing diagram.





Figure 26 provides the boundary-scan timing diagram.



Figure 26. Boundary-Scan Timing Diagram





Figure 27. Test Access Port Timing Diagram

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t _{I2CF}	—	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6	_	μS
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μS
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V

Table 39. I²C AC Electrical Specifications (continued)

Notes:

- 1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2DVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.
- 5.)The device does not follow the "I2C-BUS Specifications" version 2.1 regarding the tI2CF AC parameter.

Figure 28 provides the AC test load for the I^2C .



Figure 28. I²C AC Test Load

Figure 29 shows the AC timing diagram for the I^2C bus.



Figure 29. I²C Bus AC Timing Diagram



PCI

Table 41. PCI AC Timing Specifications at 66 MHz¹ (continued)

Parameter	Symbol ²	Min	Max	Unit	Notes
Input hold from clock	t _{PCIXKH}	0		ns	3, 5

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.}
- 3. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

Table 42. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	^t PCKHOV	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	-	ns	2
Clock to output high impedance	t _{PCKHOZ}	-	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	-	ns	2, 4
Input hold from clock	t _{PCIXKH}	0		ns	2, 4

Notes:

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

Figure 30 provides the AC test load for PCI.



Figure 30. PCI AC Test Load

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
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Package and Pin Listings

Table 51. MPC8343EA	(PBGA) Pinout	Listing	(continued))
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Signal	Package Pin Number		Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	AG13, AE14, AH12, AH10, AE15	0, AE15 I/O		—
MECC[5]/MDVAL	AH14	I/O	GV _{DD}	—
MECC[6:7]	AE13, AH11	I/O	GV _{DD}	—
MDM[0:3]	AG28, AG24, AF20, AG17	0	GV _{DD}	—
MDM[8]	AG12	0	GV _{DD}	—
MDQS[0:3]	AE27, AE26, AE20, AH18	I/O	GV _{DD}	—
MDQS[8]	AH13	I/O	GV _{DD}	—
MBA[0:1]	AF10, AF11	0	GV _{DD}	—
MA[0:14]	AF13, AF15, AG16, AD16, AF17, AH20, AH19, AH21, AD18, AG21, AD13, AF21, AF22, AE1, AA5	0	GV _{DD}	_
MWE	AD10	0	GV _{DD}	—
MRAS	AF7	0	GV _{DD}	—
MCAS	AG6	0	GV _{DD}	—
MCS[0:3]	AE7, AH7, AH4, AF2	0	GV _{DD}	—
MCKE[0:1]	AG23, AH23	0	GV _{DD}	3
MCK[0:3]	AH15, AE24, AE2, AF14	0	GV _{DD}	—
MCK[0:3]	AG15, AD23, AE3, AG14	0	GV _{DD}	—
MODT[0:3]	AG5, AD4, AH6, AF4	O GV _{DD}		—
MBA[2]	AD22	0	GV _{DD}	—
MDIC0	AG11	I/O	—	9
MDIC1	AF12	I/O	—	9
	Local Bus Controller Interface			
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	H1	I/O	OV _{DD}	—
LDP[1]/CKSTOP_IN	К5	I/O	OV _{DD}	—
LDP[2]/LCS[4]	H2 I/O C		OV _{DD}	—
LDP[3]/LCS[5]	G1 I/O OV _I		OV _{DD}	—
LA[27:31]	J4, H3, G2, F1, G3 O OV _{DD}		OV _{DD}	—
LCS[0:3]	J5, H4, F2, E1	J5, H4, F2, E1 O OV _{DD}		—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	F3, G4, D1, E2	0	OV _{DD}	—



Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
Power and Ground Signals						
AV _{DD} 1	C15	Power for e300 PLL (1.2 V)	AV _{DD} 1	—		
AV _{DD} 2	U1	Power for system PLL (1.2 V)	AV _{DD} 2	_		
AV _{DD} 3	AF9	Power for DDR DLL (1.2 V)	_			
AV _{DD} 4	U2	Power for LBIU DLL (1.2 V)	AV _{DD} 4	—		
GND	 A2, B1, B2, D10, D18, E6, E14, E22, F9, F12, F15, F18, F21, F24, G5, H6, J23, L4, L6, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, M16, M17, M18, M23, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, P24, R5, R23, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U6, U11, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V23, V25, W4, Y6, AA23, AB24, AC5, AC8, AC11, AC14, AC17, AC20, AD9, AD15, AD21, AE12, AE18, AF3, AF26 	_	_	_		
GV _{DD}	U9, V9, W10, W19, Y11, Y12, Y14, Y15, Y17, Y18, AA6, AB5, AC9, AC12, AC15, AC18, AC21, AC24, AD6, AD8, AD14, AD20, AE5, AE11, AE17, AG2, AG27	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}			
LV _{DD1}	U20, W25	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5V, 3.3V)	LV _{DD1}	—		
LV _{DD2}	V20, Y23	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD2}			
V _{DD}	J11, J12, J15, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L18, L19, M10, M19, N10, N19, P9, P10, P19, R10, R19, R20, T10, T19, U10, U19, V10, V11, V18, V19, W11, W12, W13, W14, W15, W16, W17, W18	Power for core (1.2 V)	V _{DD}	_		

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

RCWL[SPMF]	System PLL Multiplication Factor
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

Table 54. Sy	ystem PLL	Multiplication	Factors ((continued)
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As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 55 and Table 56 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
				<i>csb_clk</i> Freq	uency (MHz)	
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			

Table 55. CSB Frequency Options for Host Mode

NP

Thermal

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_I = junction temperature (°C)

 T_A = ambient temperature for the package (°C)

 $R_{\theta IA}$ = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_I = junction temperature (°C)

 T_T = thermocouple temperature on top of package (°C)

 Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so



System Design Information

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8343EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8343EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8343EA.

21.5 Output Buffer DC Impedance

The MPC8343EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 39). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals