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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8343cvraddb

  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects for eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters

  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - 39 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8343EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Parameter	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.32	V	—
PLL supply voltage	AV_{DD}	–0.3 to 1.32	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage	LV_{DD}	–0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—

Table 5 shows the estimated typical I/O power dissipation for MPC8343EA.

Table 5. MPC8343EA Typical I/O Power Dissipation

Interface	Parameter	DDR2 GV_{DD} (1.8 V)	DDR1 GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	200 MHz, 32 bits	0.31	0.42	—	—	—	W	—
	266 MHz, 32 bits	0.35	0.5	—	—	—	W	—
PCI I/O load = 30 pF	33 MHz, 32 bits	—	—	0.04	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
Local bus I/O load = 25 pF	167 MHz, 32 bits	—	—	0.34	—	—	W	—
	133 MHz, 32 bits	—	—	0.27	—	—	W	—
	83 MHz, 32 bits	—	—	0.17	—	—	W	—
	66 MHz, 32 bits	—	—	0.14	—	—	W	—
	50 MHz, 32 bits	—	—	0.11	—	—	W	—
TSEC I/O load = 25 pF	MII	—	—		0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—		0.06	—	W	
	RGMII or RTBI	—	—		—	0.04	W	
USB	12 MHz	—	—	0.01	—	—	W	—
	480 MHz	—	—	0.2	—	—	W	—
Other I/O		—	—	0.01	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8343EA.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	$0 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA

5.2 RESET AC Electrical Characteristics

Table 10 provides the reset initialization AC timing specifications of the MPC8343EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8343EA is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8343EA is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8343EA is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8343EA is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8343EA to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8343EA to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, “Clocking.”

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
ADDR/CMD/MODT output hold with respect to MCK	t_{DDKHAX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{MCS}$(n) output setup with respect to MCK	t_{DDKHCS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{MCS}$(n) output hold with respect to MCK	t_{DDKHCX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
400 MHz		700	—		
333 MHz		775	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 30. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 13 shows the MII management AC timing diagram.

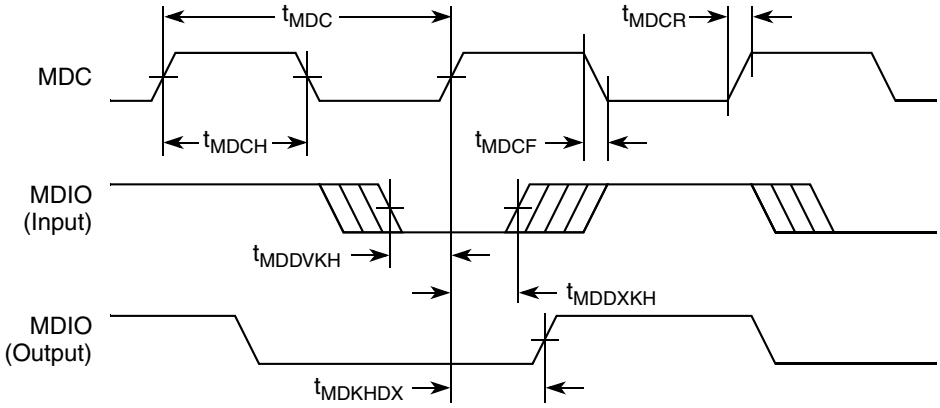


Figure 13. MII Management Interface Timing Diagram

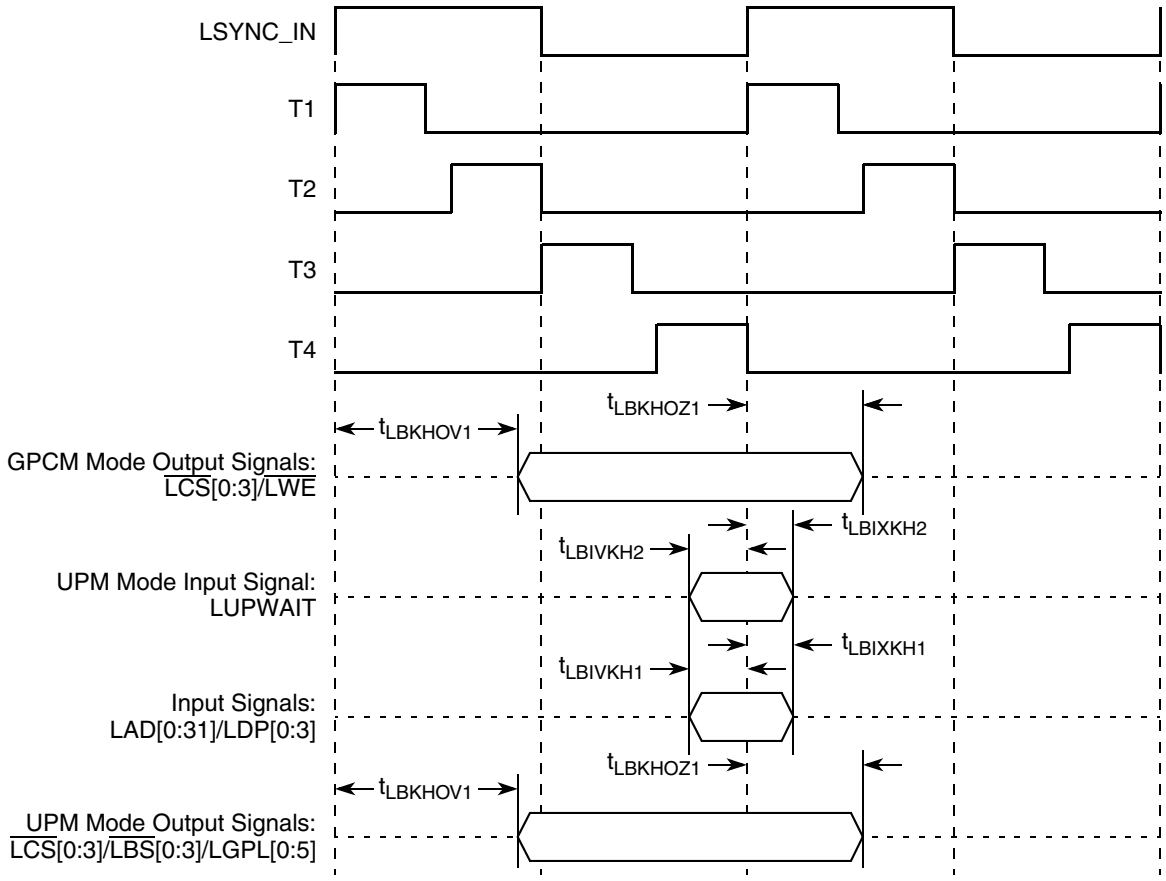


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

11.1 JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

Table 36. JTAG Interface DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	OV_{DD} – 0.3	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8343EA.

13.1 PCI DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the PCI interface of the MPC8343EA.

Table 40. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN}[1]= 0 V or $V_{IN} = OV_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8343EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 41 provides the PCI AC timing specifications at 66 MHz.

Table 41. PCI AC Timing Specifications at 66 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

Table 41. PCI AC Timing Specifications at 66 MHz[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Input hold from clock	t_{PCIXKH}	0	—	ns	3, 5

Notes:
1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

Table 42. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 30 provides the AC test load for PCI.

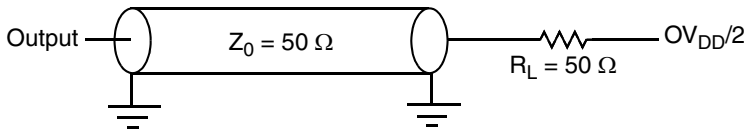


Figure 30. PCI AC Test Load

Table 49. SPI DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 50 provides the SPI input and output AC timing specifications.

Table 50. SPI AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the SPI.

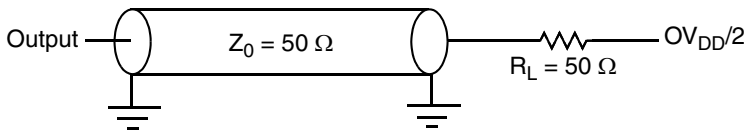
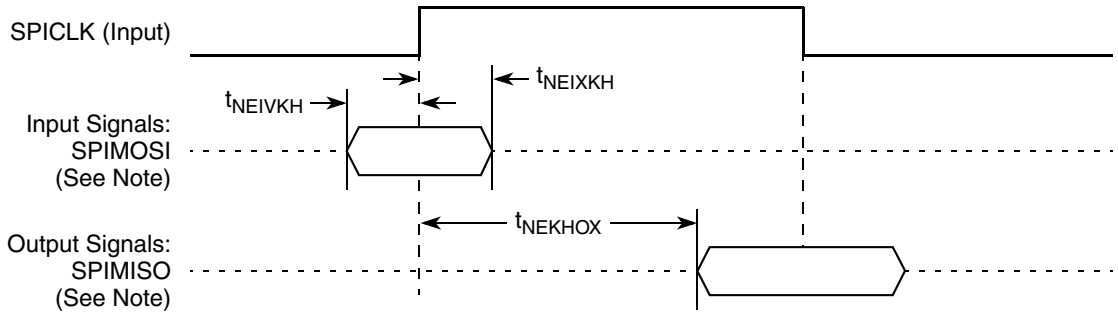


Figure 33. SPI AC Test Load

Figure 34 and Figure 35 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

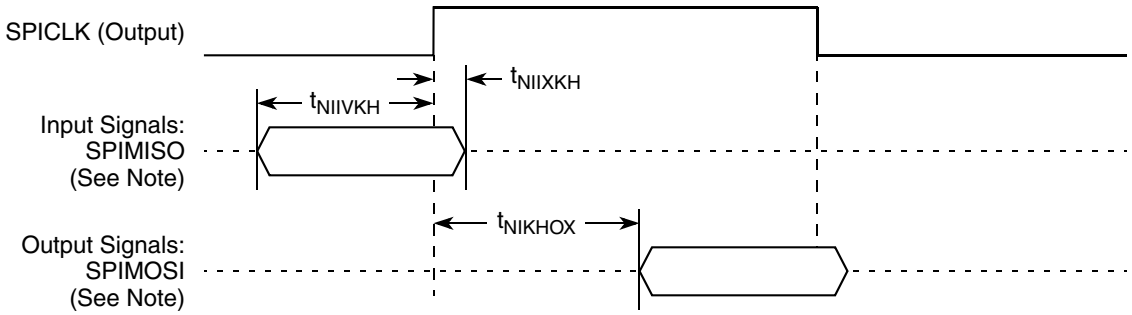
Figure 34 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 35 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8343EA is available in a plastic ball grid array (PBGA). See Section 18.1, "Package Parameters for the MPC8343EA PBGA," and Section 18.2, "Mechanical Dimensions for the MPC8343EA PBGA."

18.1 Package Parameters for the MPC8343EA PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm

Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 96.5 Sn/3.5Ag (VR package)
Ball diameter (typical)	0.60 mm

19 Clocking

Figure 37 shows the internal distribution of the clocks.

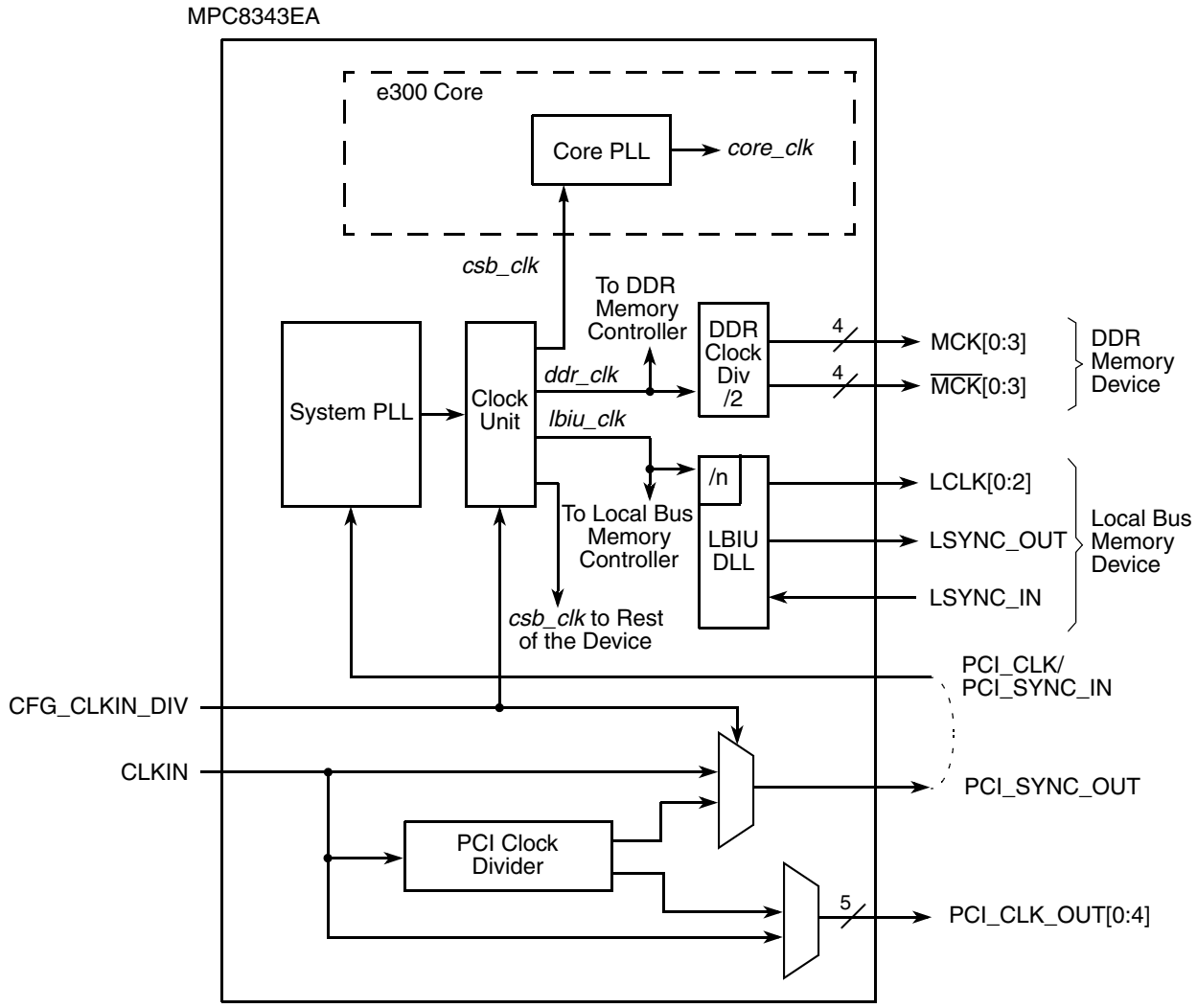


Figure 37. MPC8343EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8343EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8343EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

Table 53 provides the operating frequencies for the MPC8343EA PBGA under recommended operating conditions.

Table 53. Operating Frequencies for PBGA

Parameter[1]	266 MHz	333 MHz	400 MHz	Unit
e300 core frequency (*core_clk*)	200–266	200–333	200–400	MHz
Coherent system bus frequency (*csb_clk*)	100–266			MHz
DDR1 memory bus frequency (MCK)[2]	100–133			MHz
DDR2 memory bus frequency (MCK)[3]	100–133			MHz
Local bus frequency (LCLK*n*)[4]	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66			MHz
Security core maximum internal operating frequency	133			MHz
USB_DR, USB_MPH maximum internal operating frequency	133			MHz

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

2 The DDR data rate is 2× the DDR memory bus frequency.

3 The DDR data rate is 2× the DDR memory bus frequency.

4 The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBIUCM]).

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 54 shows the multiplication factor encodings for the system PLL.

Table 54. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10

Table 54. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 55 and Table 56 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 55. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			

Table 56. CSB Frequency Options for Agent Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

1 CFG_CLKIN_DIV doubles csb_clk if set high.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 57 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 57 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

Table 57. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider[1]
0–1	2–5	6		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
11	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
11	**0001**	1	1.5:1	8

Table 57. e300 Core PLL Configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider[1]
0–1	2–5	6		
00	0010	0	2:1	2
01	0010	0	2:1	4
10	0010	0	2:1	8
11	0010	0	2:1	8
00	0010	1	2.5:1	2
01	0010	1	2.5:1	4
10	0010	1	2.5:1	8
11	0010	1	2.5:1	8
00	0011	0	3:1	2
01	0011	0	3:1	4
10	0011	0	3:1	8
11	0011	0	3:1	8

1 Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

19.3 Suggested PLL Configurations

Table 58 shows suggested PLL configurations for 33 and 66 MHz input clocks, when CFG_CLKIN_DIV is low at reset.

Table 58. Suggested PLL Configurations

Ref No.[1]	RCWL		266 MHz Device			333 MHz Device			400 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
33 MHz CLKIN/PCI_CLK Options											
343	0011	1000011	33	100	150	33	100	150	33	100	150
324	0011	0100100	33	100	200	33	100	200	33	100	200
423	0100	0100011	33	133	200	33	133	200	33	133	200
622	0110	0100010	33	200	200	33	200	200	33	200	200
523	0101	0100011	33	166	250	33	166	250	33	166	250
424	0100	0100100	33	133	266	33	133	266	33	133	266
822	1000	0100010	33	266	266	33	266	266	33	266	266

Table 58. Suggested PLL Configurations (continued)

Ref No.[1]	RCWL		266 MHz Device			333 MHz Device			400 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
326	**0011**	**0100110**	—			33	100	300	33	100	300
623	**0110**	**0100011**	—			33	200	300	33	200	300
922	**1001**	**0100010**	—			33	300	300	33	300	300
425	**0100**	**0100101**	—			33	133	333	33	133	333
524	**0101**	**0100100**	—			33	166	333	33	166	333
A22	**1010**	**0100010**	—			33	333	333	33	333	333
723	**0111**	**0100011**	—			—			33	233	350
604	**0110**	**0000100**	—			—			33	200	400
624	**0110**	**0100100**	—			—			33	200	400
823	1000	0100011	—			—			33	266	400
66 MHz CLKIN/PCI_CLK Options											
242	**0010**	**1000010**	66	133	133	66	133	133	66	133	133
322	**0011**	**0100010**	66	200	200	66	200	200	66	200	200
224	**0010**	**0100100**	66	133	266	66	133	266	66	133	266
422	**0100**	**0100010**	66	266	266	66	266	266	66	266	266
323	**0011**	**0100011**	—			66	200	300	66	200	300
223	**0010**	**0100101**	—			66	133	333	66	133	333
522	**0101**	**0100010**	—			66	333	333	66	333	333
304	**0011**	**0000100**	—			—			66	200	400
324	**0011**	**0100100**	—			—			66	200	400
403	**0100**	**0000011**	—			—			66	266	400
423	**0100**	**0100011**	—			—			66	266	400

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

20 Thermal

This section describes the thermal specifications of the MPC8343EA.

20.1 Thermal Characteristics

.Table 59 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8343EA.

Table 59. Package Thermal Characteristics for PBGA

Parameter	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	17	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	ψ_{JT}	5	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

23 Document Revision History

This table provides a revision history of this document.

Table 64. Document Revision History

Rev. Number	Date	Substantive Change(s)
11	09/2011	• In Section 2.2, "Power Sequencing," added Section 2.2.1, "Power-Up Sequencing" and Figure 4. • In Table 25, Table 29, and Table 27, removed the GTX_CLK125. • In Table 30, updated t_{MDKHDX} Max value from 170ns to 70ns.
10	11/2010	• In Table 51, added overbar to $\overline{LCS}$[4] and $\overline{LCS}$[5] signals. In Table 51 added note for pin LGPL4. • In Section 21.7, "Pull-Up Resistor Requirements, updated the list of open drain type pins.
9	05/2010	• In Table 25 through Table 26, changed V_{IL}(min) to V_{IH}(max) to (20%–80%). • Added Table 8, "EC_GTX_CLK125 AC Timing Specifications."
8	5/2009	• In Section 18.1, "Package Parameters for the MPC8343EA PBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. • In Table 53, added two columns for the DDR1 and DDR2 memory bus frequency. • In Table 62, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.
7	2/2009	• Added footnote 6 to Table 7. • In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. • In Table 35, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 18, Figure 20, and Figure 21 for output signals. • Added footnote 10 to Table 51. • In Table 51, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net." • In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. • In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." • In Table 62, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266."
6	4/2007	• In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. • In Section 21.7, "Pull-Up Resistor Requirements,"deleted last two paragraphs and after first paragraph, added a new paragraph. • Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
5	3/2007	• Page 1, updated first paragraph to reflect PowerQUICC II Pro information. • In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. • In Figure 38, "JTAG Interface Connection," updated with new figure. • In Figure 38, "JTAG Interface Connection," updated with new figure. • In Section 23, "Ordering Information," replaced first paragraph and added a note. • In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T_{ddkhds} for 333 MHz from 900 ps to 775 ps.