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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8343czqagd

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications.*

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8343EA.
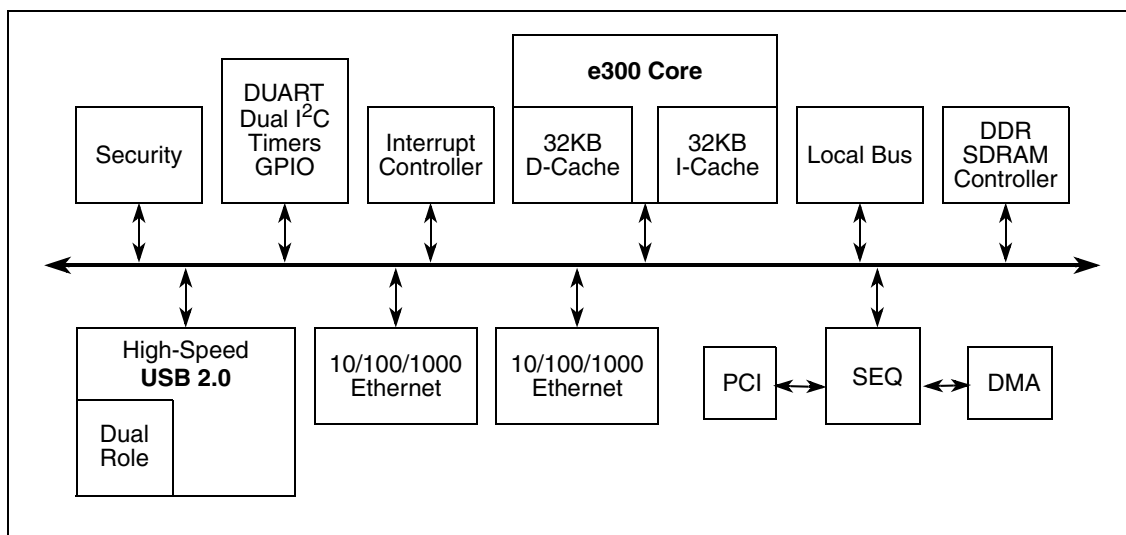

Figure 1. MPC8343EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 400 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- bit data interface, up to 266 MHz data rate

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- — Misaligned transfer capability
- — Data chaining and direct mode
- — Interrupt on completed segment and chain
- DUART
  - — Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - — Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - — 39 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - — Periodic interrupt timer
  - — Real-time clock
  - — Software watchdog timer
  - — Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8343EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Parameter	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	−0.3 to 1.32	V	—
PLL supply voltage	AV_{DD}	−0.3 to 1.32	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	−0.3 to 2.75 −0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage	LV_{DD}	−0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I²C, and JTAG I/O voltage	OV_{DD}	−0.3 to 3.63	V	—

Table 1. Absolute Maximum Ratings[1] (continued)

Parameter		Symbol	Max Value	Unit	Notes
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	−0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I²C, and JTAG signals	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	−55 to 150	°C	—

Notes:

[1] Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

[2] **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[3] **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[4] **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[5] $(M,L,O)V_{IN}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

[6] OVIN on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8343EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—

Table 2. Recommended Operating Conditions (continued)

Parameter	Symbol	Recommended Value	Unit	Notes
PCI, local bus, DUART, system control and power management, I^{2}C, and JTAG I/O voltage	OV$_{DD}$	3.3 V ± 330 mV	V	—

Note:

[1] GV$_{DD}$, LV$_{DD}$, OV$_{DD}$, AV$_{DD}$, and V$_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8343EA.
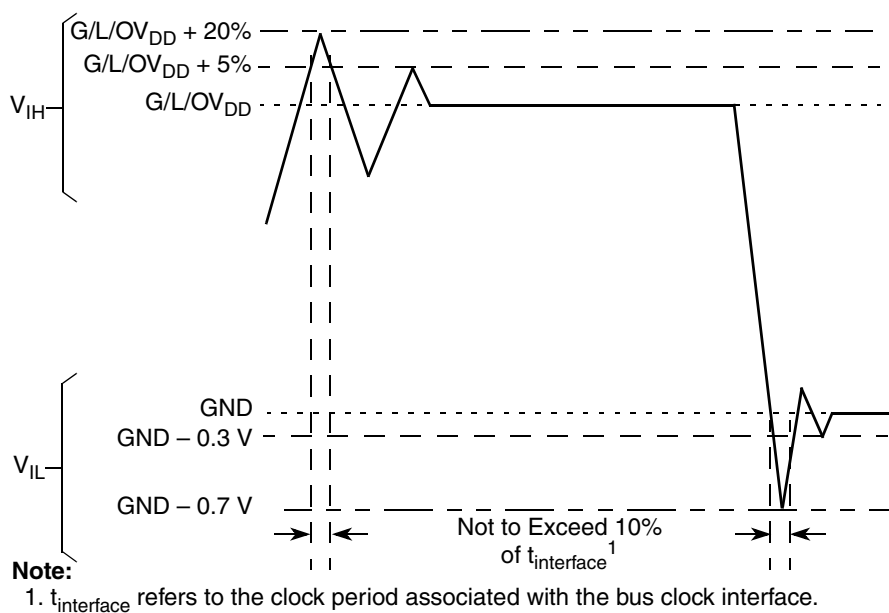

Note:

1. t$_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GV$_{DD}$/OV$_{DD}$/LV$_{DD}$

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8343EA for the 3.3-V signals, respectively.
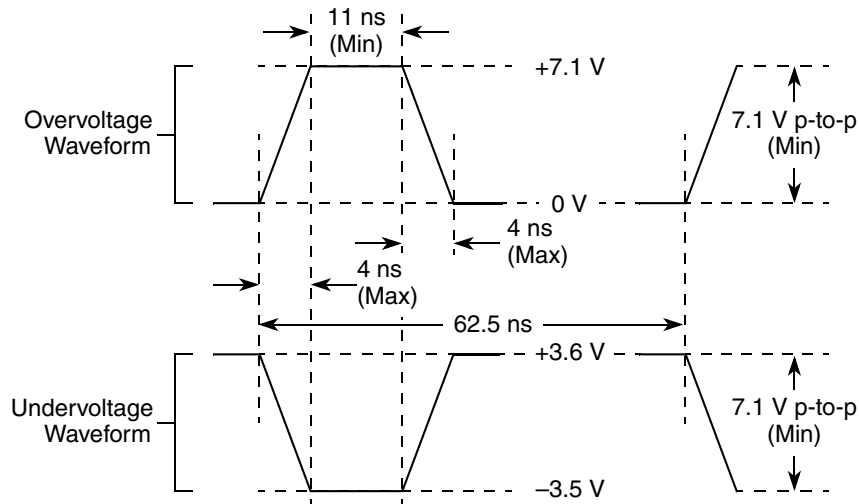

Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3   Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV_{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV_{DD} = 1.8 V
TSEC/10/100 signals	40	LV_{DD} = 2.5/3.3 V
DUART, system control, I^{2}C, JTAG, USB	40	OV_{DD} = 3.3 V
GPIO signals	40	OV_{DD} = 3.3 V, LV_{DD} = 2.5/3.3 V

2.2   Power Sequencing

This section details the power sequencing considerations for the MPC8343EA.

2.2.1   Power-Up Sequencing

MPC8343EAdoes not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

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6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8343EA. Note that DDR SDRAM is $GV_{DD}(typ) = 2.5$ V and DDR2 SDRAM is $GV_{DD}(typ) = 1.8$ V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

NOTE

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications.* See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8343EA when $GV_{DD}(typ) = 1.8$ V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 1.8$ V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	-9.9	9.9	μA	4
Output high current ($V_{OUT} = 1.420$ V)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280$ V)	I_{OL}	13.4	—	mA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to equal $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V $\leq V_{OUT} \leq GV_{DD}$.

Table 21. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8343EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8   Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—MII/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII interface is defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

MII, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}[2]	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0$ mA	LV_{DD} = Min	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0$ mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	−0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = GND		−600	—	μA

Notes:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	LV_{DD} = Min	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	LV_{DD} = Min	GND − 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	−0.3	0.70	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN}[1] = GND		−15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2.2 RGMII and RTBI AC Timing Specifications

Table 27 presents the RGMII and RTBI AC timing specifications.

Table 27. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	−0.5	—	0.5	ns
Data to clock input skew (at receiver)[2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration[3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T[4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX[3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).

2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.

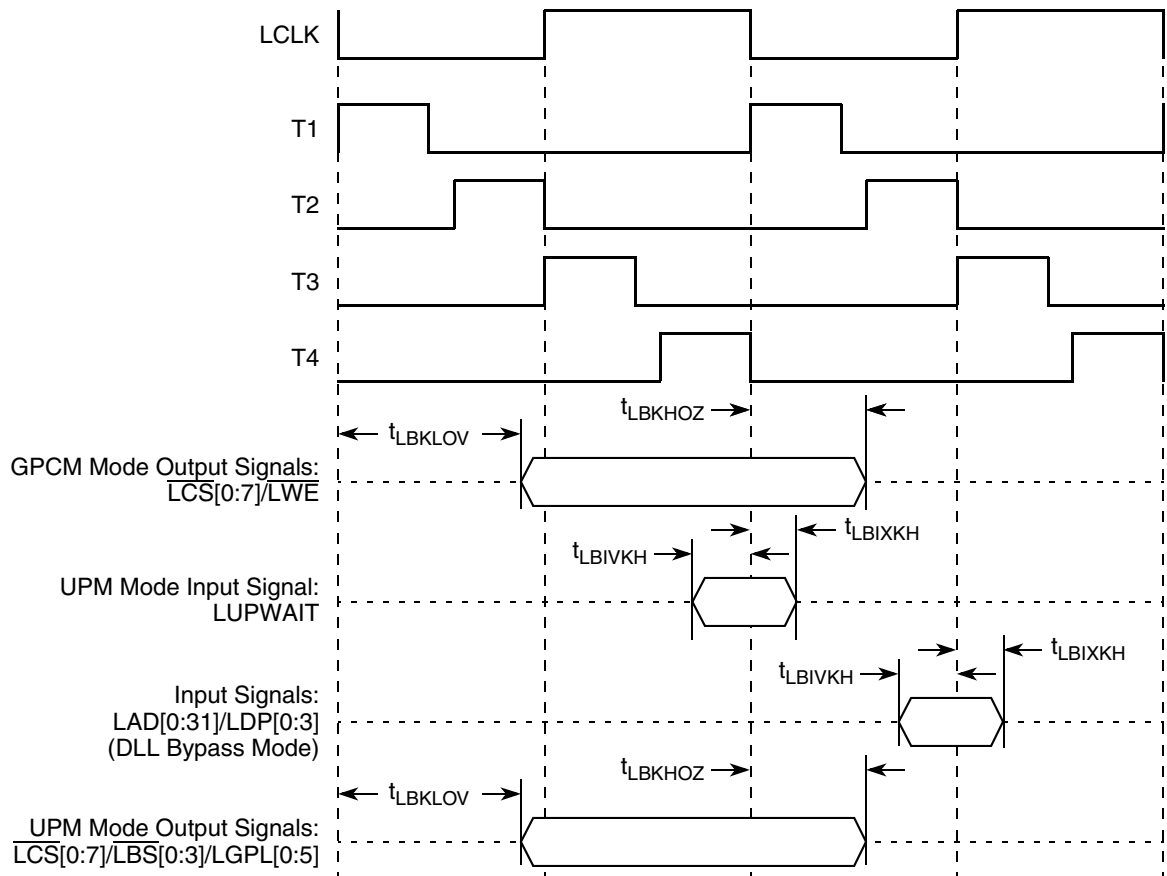5. Duty cycle reference is $LV_{DD}/2$.

Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	5, 6
Boundary-scan data	t_{JTKLDZ}	2	19		
TDO	t_{JTKLOZ}	2	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t_{TCLK}.

5. Non-JTAG signal output timing with respect to t_{TCLK}.

6. Guaranteed by design and characterization.

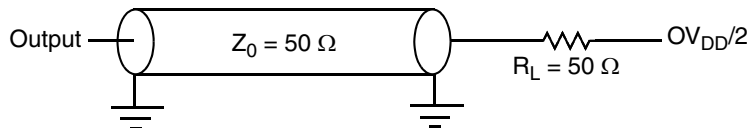Figure 23 provides the AC test load for TDO and the boundary-scan outputs of the MPC8343EA.

Figure 23. AC Test Load for the JTAG Interface

Figure 24 provides the JTAG clock input timing diagram.
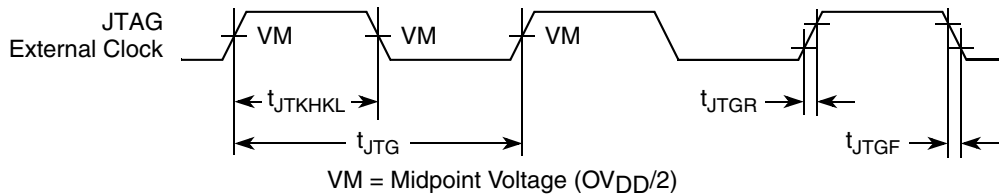

VM = Midpoint Voltage (OV$_{DD}$/2)

Figure 24. JTAG Clock Input Timing Diagram

Figure 25 provides the $\overline{TRST}$ timing diagram.
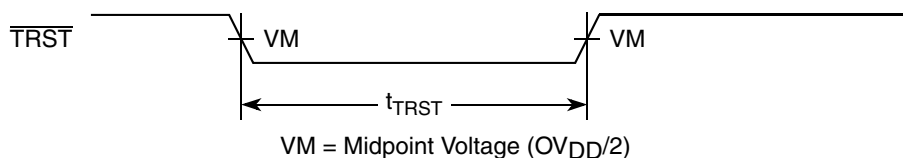

VM = Midpoint Voltage (OV$_{DD}$/2)

Figure 25. $\overline{TRST}$ Timing Diagram

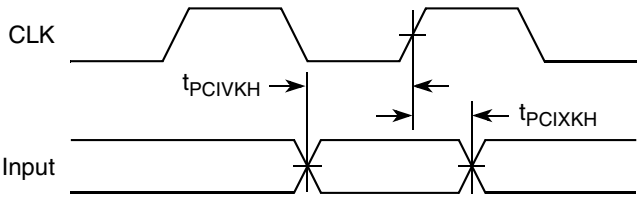Figure 31 shows the PCI input AC timing diagram.

Figure 31. PCI Input AC Timing Diagram

Figure 32 shows the PCI output AC timing diagram.
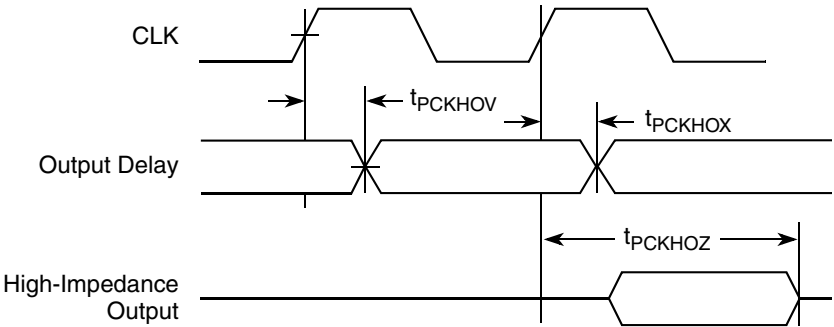
Figure 32. PCI Output AC Timing Diagram

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the MPC8343EA timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 43. Timer DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

Table 44. Timers Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8343EA GPIO.

Table 45. GPIO DC Electrical Characteristics

PArameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = –8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 46 provides the GPIO input and output AC timing specifications.

Table 46. GPIO Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package)
	96.5 Sn/3.5Ag (VR package)
Ball diameter (typical)	0.60 mm

18.3 Pinout Listings

Table 51 provides the pin-out listing for the MPC8343EA, 620-PBGA package.

Table 51. MPC8343EA (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI1_INTA/IRQ_OUT	D20	O	OV$_{DD}$	2
PCI1_RESET_OUT	B21	O	OV$_{DD}$	—
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV$_{DD}$	—
PCI1_C/BE[3:0]	A17, A14, A11, B10	I/O	OV$_{DD}$	—
PCI1_PAR	D13	I/O	OV$_{DD}$	—
PCI1_FRAME	B14	I/O	OV$_{DD}$	5
PCI1_TRDY	A13	I/O	OV$_{DD}$	5
PCI1_IRDY	E13	I/O	OV$_{DD}$	5
PCI1_STOP	C13	I/O	OV$_{DD}$	5
PCI1_DEVSEL	B13	I/O	OV$_{DD}$	5
PCI1_IDSEL	C17	I	OV$_{DD}$	—
PCI1_SERR	C12	I/O	OV$_{DD}$	5
PCI1_PERR	B12	I/O	OV$_{DD}$	5
PCI1_REQ[0]	A21	I/O	OV$_{DD}$	—
PCI1_REQ[1]/CPCI1_HS_ES	C19	I	OV$_{DD}$	—
PCI1_REQ[2:4]	C18, A19, E20	I	OV$_{DD}$	—
PCI1_GNT0	B20	I/O	OV$_{DD}$	—
PCI1_GNT1/CPCI1_HS_LED	C20	O	OV$_{DD}$	—
PCI1_GNT2/CPCI1_HS_ENUM	B19	O	OV$_{DD}$	—
PCI1_GNT[3:4]	A20, E18	O	OV$_{DD}$	—
M66EN	L26	I	OV$_{DD}$	—
DDR SDRAM Memory Interface				
MDQ[0:31]	AC25, AD27, AD25, AH27, AE28, AD26, AD24, AF27, AF25, AF28, AH24, AG26, AE25, AG25, AH26, AH25, AG22, AH22, AE21, AD19, AE22, AF23, AE19, AG20, AG19, AD17, AE16, AF16, AF18, AG18, AH17, AH16	I/O	GV$_{DD}$	—

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_DV	U24	I	LV_{DD1}	—
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV_{DD}	—
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV_{DD1}	—
TSEC1_TX_CLK	N25	I	OV_{DD}	—
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV_{DD1}	10
TSEC1_TX_EN	W27	O	LV_{DD1}	—
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV_{DD}	—
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV_{DD2}	—
TSEC2_GTX_CLK	AC27	O	LV_{DD2}	—
TSEC2_RX_CLK	AB25	I	LV_{DD2}	—
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV_{DD2}	—
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV_{DD2}	—
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV_{DD}	—
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV_{DD2}	—
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV_{DD}	—
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV_{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV_{DD}	—
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/ LSRCID[0:1]	B4, A4	O	OV_{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/ LSRCID[2:3]	D5, C5	I/O	OV_{DD}	—
$\overline{UART\_CTS}$[1]/MSRCID4/LSRCID4	B5	I/O	OV_{DD}	—
$\overline{UART\_CTS}$[2]/MDVAL/LDVAL	A5	I/O	OV_{DD}	—
$\overline{UART\_RTS}$[1:2]	D6, C6	O	OV_{DD}	—
I²C interface				
IIC1_SDA	E5	I/O	OV_{DD}	2
IIC1_SCL	A6	I/O	OV_{DD}	2
IIC2_SDA	B6	I/O	OV_{DD}	2
IIC2_SCL	E7	I/O	OV_{DD}	2

Table 55. CSB Frequency Options for Host Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	csb_clk : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

[1] CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Table 56. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	csb_clk : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266

Table 56. CSB Frequency Options for Agent Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	csb_clk : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

[1] CFG_CLKIN_DIV doubles csb_clk if set high.

[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 57 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 57 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

Table 57. e300 Core PLL Configuration

RCWL[COREPLL]			core_clk : csb_clk Ratio	VCO Divider[1]
0–1	2–5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	2
01	0001	0	1:1	4
10	0001	0	1:1	8
11	0001	0	1:1	8
00	0001	1	1.5:1	2
01	0001	1	1.5:1	4
10	0001	1	1.5:1	8
11	0001	1	1.5:1	8

that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 60 shows heat sink thermal resistance for PBGA of the MPC8343EA.

Table 60. Heat Sink and Thermal Resistance of MPC8343EA (PBGA)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	13.5
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	9.6
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	8.8
AAVID 31 × 35 × 23 mm pin fin	Natural convection	11.3
AAVID 31 × 35 × 23 mm pin fin	1 m/s	8.1
AAVID 31 × 35 × 23 mm pin fin	2 m/s	7.5
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	9.1
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	7.1
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	6.5
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	10.1

$OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.
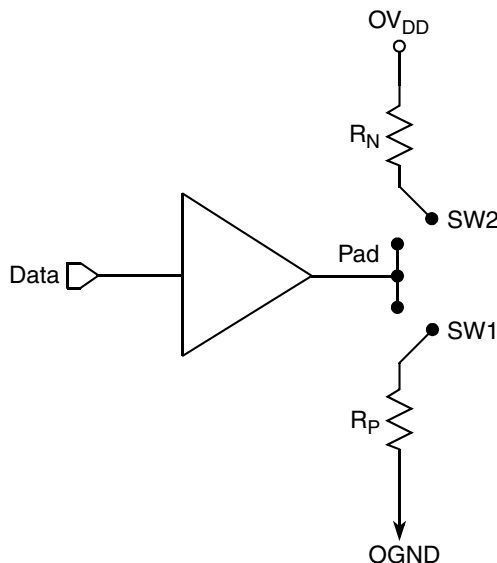

Figure 39. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1 \div (1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1 \div V_2 - 1)$. The drive current is then $I_{source} = V_1 \div R_{source}$.

Table 61 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 61. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	W
Differential	NA	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

21.6 Configuration Pin Multiplexing

The MPC8343EA power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.