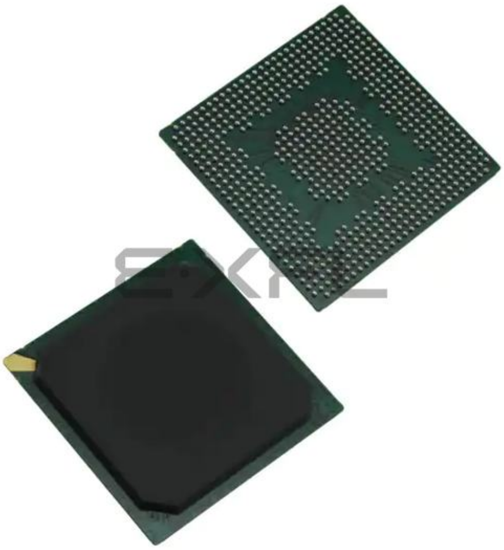

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (3) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 620-BBGA Exposed Pad |
| Supplier Device Package | 620-HBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8343czqagdb |

- — Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- — DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
- — Full error checking and correction (ECC) support
- — Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- — Contiguous or discontiguous memory mapping
- — Read-modify-write support
- — Sleep-mode support for SDRAM self refresh
- — Auto refresh
- — On-the-fly power management using CKE
- — Registered DIMM support
- — 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2

- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - — Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - — Ethernet physical interfaces:
    - – 1000 Mbps IEEE Std. 802.3 RGMII, IEEE Std. 802.3z RTBI, full-duplex
    - – 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - — Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - — 9.6-Kbyte jumbo frame support
  - — RMON statistics support
  - — Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - — MII management interface for control and status
  - — Programmable CRC generation and checking
- PCI interface
  - — Designed to comply with *PCI Specification Revision 2.3*
  - — Data bus width:
    - – 32-bit data PCI interface operating at up to 66 MHz
  - — PCI 3.3-V compatible
  - — PCI host bridge capabilities
  - — PCI agent mode on PCI interface
  - — PCI-to-memory and memory-to-PCI streaming
  - — Memory prefetching of PCI read accesses and support for delayed read transactions
  - — Posting of processor-to-PCI and PCI-to-memory writes
  - — On-chip arbitration supporting five masters on PCI
  - — Accesses to all PCI address spaces
  - — Parity supported
  - — Selectable hardware-enforced coherency

**Table 8. EC_GTX_CLK125 AC Timing Specifications**
**At recommended operating conditions with $LV_{DD}$ = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)**

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 duty cycle<br>GMII, TBI<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 2 |
| EC_GTX_CLK125 jitter | — | — | — | ±150 | ps | 2 |

**Notes:**
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD}$ = 2.5 V and from 0.6 and 2.7 V for $LV_{DD}$ = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

# 5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8343EA.

## 5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8343EA.

**Table 9. RESET Pins DC Electrical Characteristics[1]**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±5 | μA |
| Output high voltage[2] | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

**Notes:**
1. This table applies for pins $\overline{PORESET}$, $\overline{HRESET}$, $\overline{SRESET}$, and $\overline{QUIESCE}$.
2. $\overline{HRESET}$ and $\overline{SRESET}$ are open drain pins, thus $V_{OH}$ is not relevant for those pins.

Table 16 provides the current draw characteristics for $MV_{REF}$.

**Table 16. Current Draw Characteristics for $MV_{REF}$**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Current draw for $MV_{REF}$ | $I_{MVREF}$ | — | 500 | μA | 1 |

**Note:**
1. The voltage regulator for $MV_{REF}$ must supply up to 500 μA current.

## 6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

### 6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}$(typ) = 1.8 V.

**Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.25 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.25 | — | V | — |

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}$(typ) = 2.5 V.

**Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface**

At recommended operating conditions with $GV_{DD}$ of 2.5 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.31 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.31 | — | V | — |

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of (1.8 or 2.5 V) ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Controller Skew for MDQS—MDQ/MECC/MDM | $t_{CISKEW}$ | | | ps | 1, 2 |
| 400 MHz | | –600 | 600 | | 3 |
| 333 MHz | | –750 | 750 | | — |

**Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)**

At recommended operating conditions with $GV_{DD}$ of (1.8 or 2.5 V) ± 5%.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6 |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
4. $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

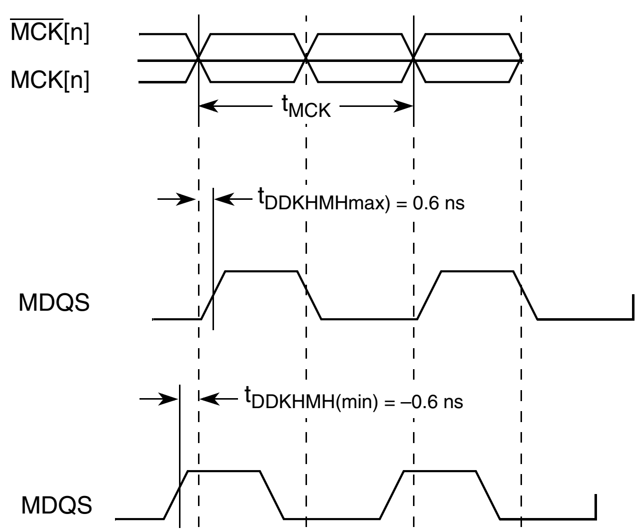



**Figure 6. Timing Diagram for $t_{DDKHMH}$**

**Table 30. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}$ is 3.3 V ± 10% or 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 13 shows the MII management AC timing diagram.

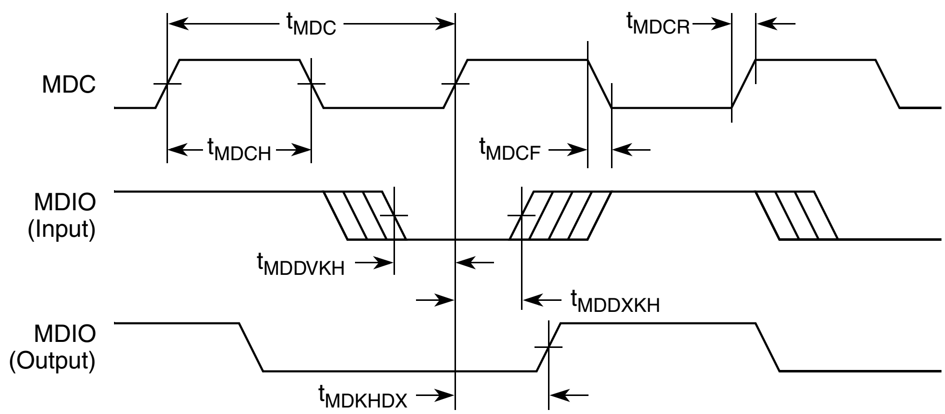



**Figure 13. MII Management Interface Timing Diagram**

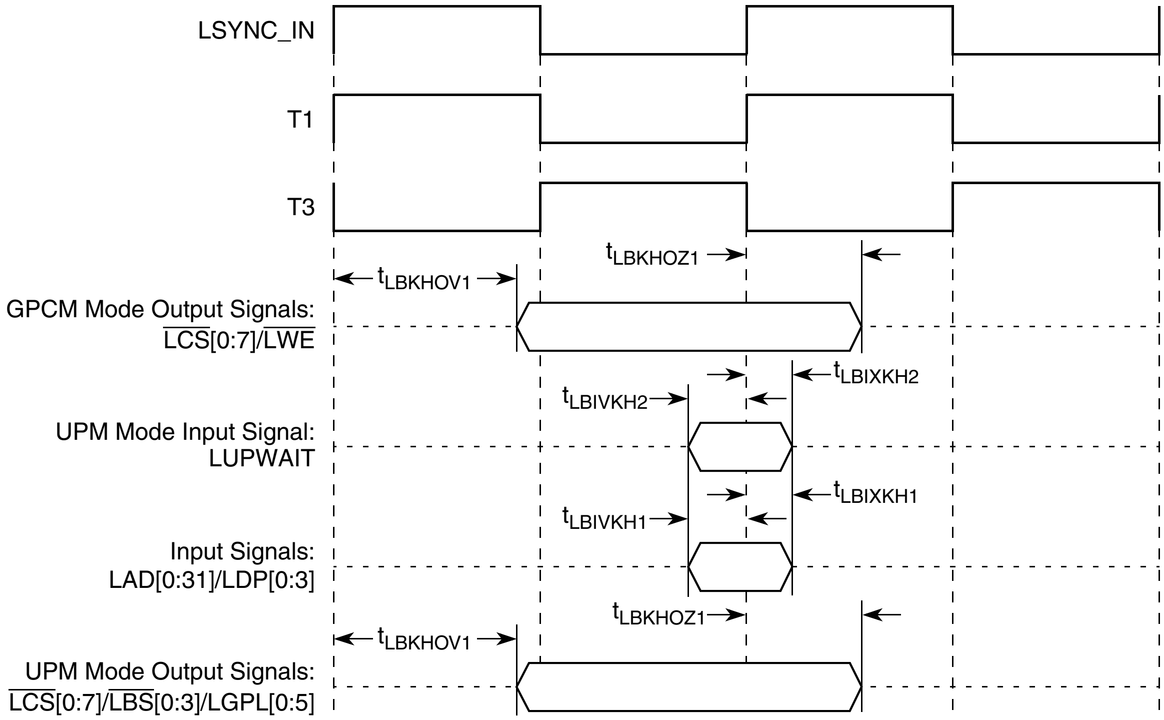



**Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)**

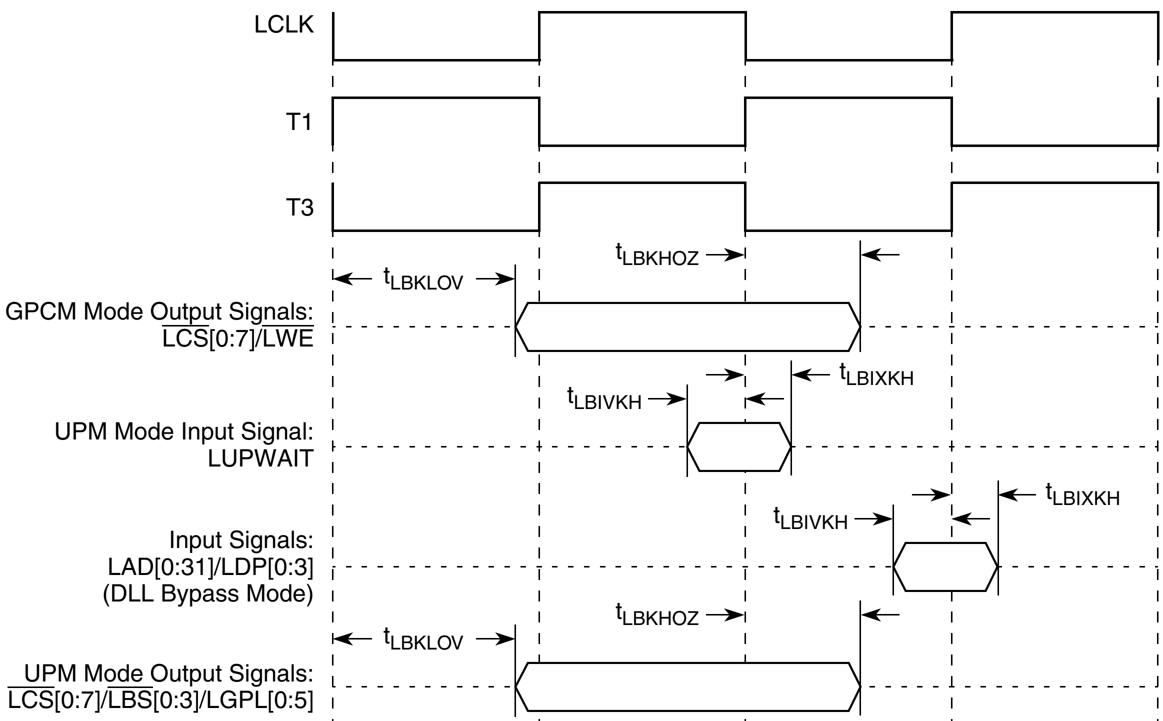



**Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)**

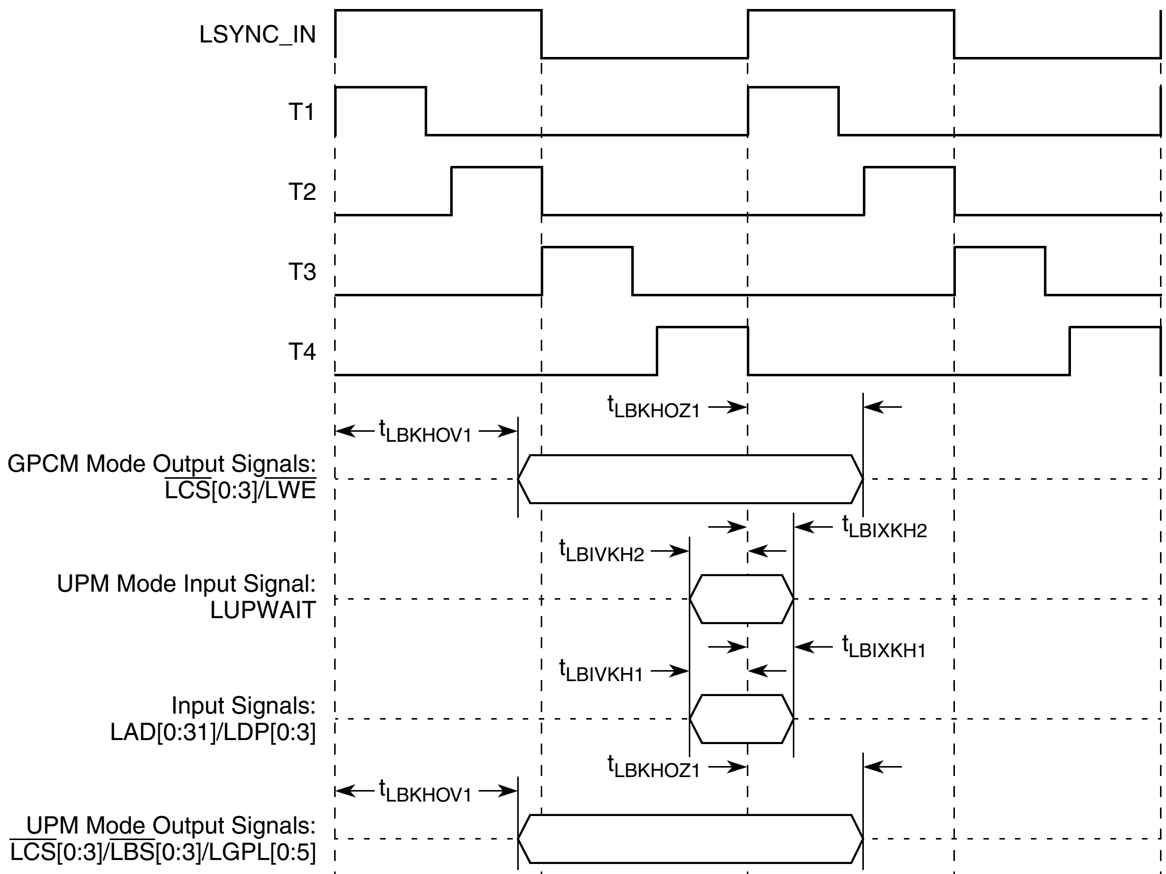



**Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)**

# 11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

## 11.1 JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8343EA.

**Table 36. JTAG Interface DC Electrical Characteristics**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | $OV_{DD}$ – 0.3 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |

Figure 26 provides the boundary-scan timing diagram.

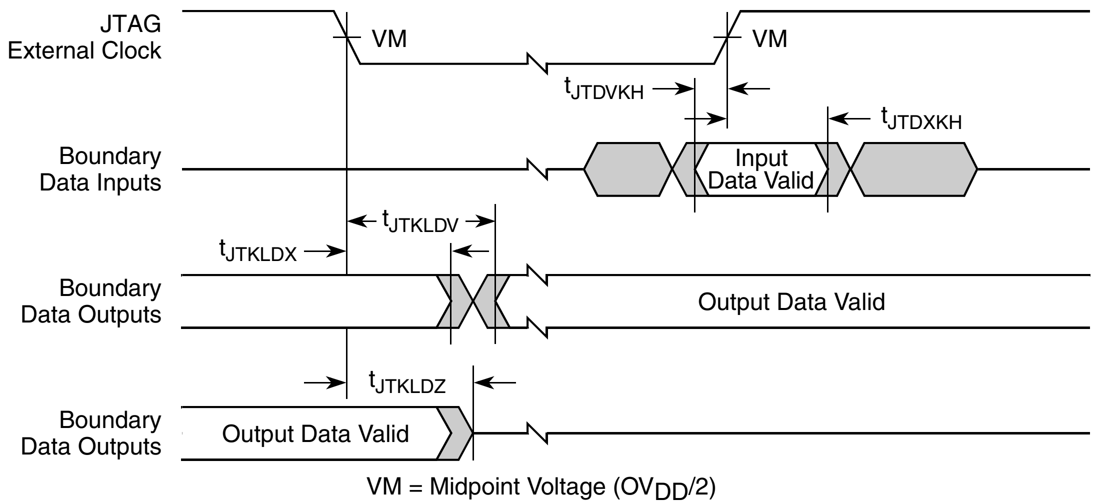



**Figure 26. Boundary-Scan Timing Diagram**

Figure 27 provides the test access port timing diagram.

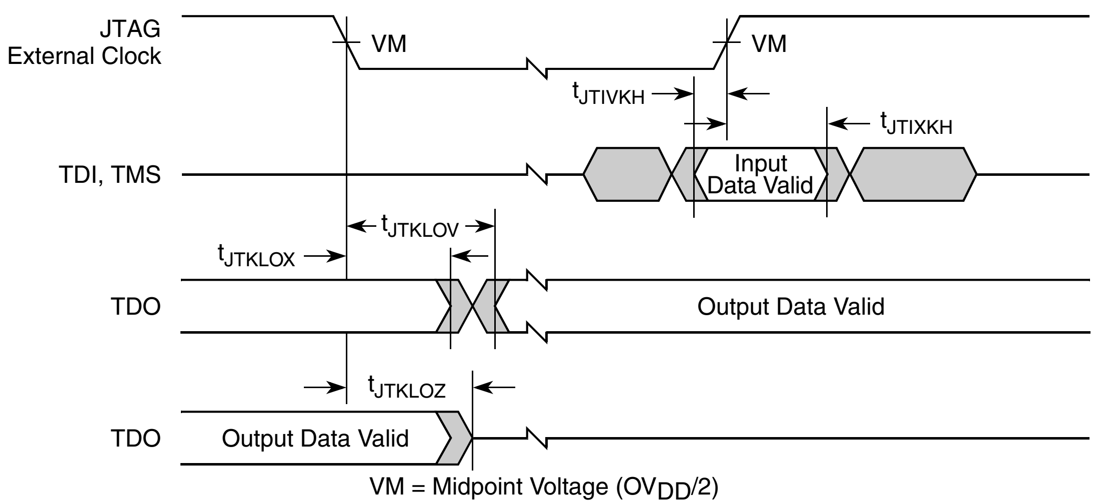



**Figure 27. Test Access Port Timing Diagram**

# 13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8343EA.

## 13.1 PCI DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the PCI interface of the MPC8343EA.

**Table 40. PCI DC Electrical Characteristics**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{OUT} \geq V_{OH}$ (min) or | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | $V_{OUT} \leq V_{OL}$ (max) | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $V_{IN}$[1]= 0 V or $V_{IN}$ = $OV_{DD}$ | — | ±5 | μA |
| High-level output voltage | $V_{OH}$ | $OV_{DD}$ = min, $I_{OH}$ = –100 μA | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage | $V_{OL}$ | $OV_{DD}$ = min, $I_{OL}$ = 100 μA | — | 0.2 | V |

**Note:**

1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1.

## 13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8343EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 41 provides the PCI AC timing specifications at 66 MHz.

**Table 41. PCI AC Timing Specifications at 66 MHz[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 6.0 | ns | 3 |
| Output hold from clock | $t_{PCKHOX}$ | 1 | — | ns | 3 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 3, 4 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 3, 5 |

| | |
|---|---|
| Module height (typical) | 2.23 mm |
| Module height (minimum) | 2.00 mm |
| Solder balls | 62 Sn/36 Pb/2 Ag (ZQ package)<br>96.5 Sn/3.5Ag (VR package) |
| Ball diameter (typical) | 0.60 mm |

# 19 Clocking

Figure 37 shows the internal distribution of the clocks.

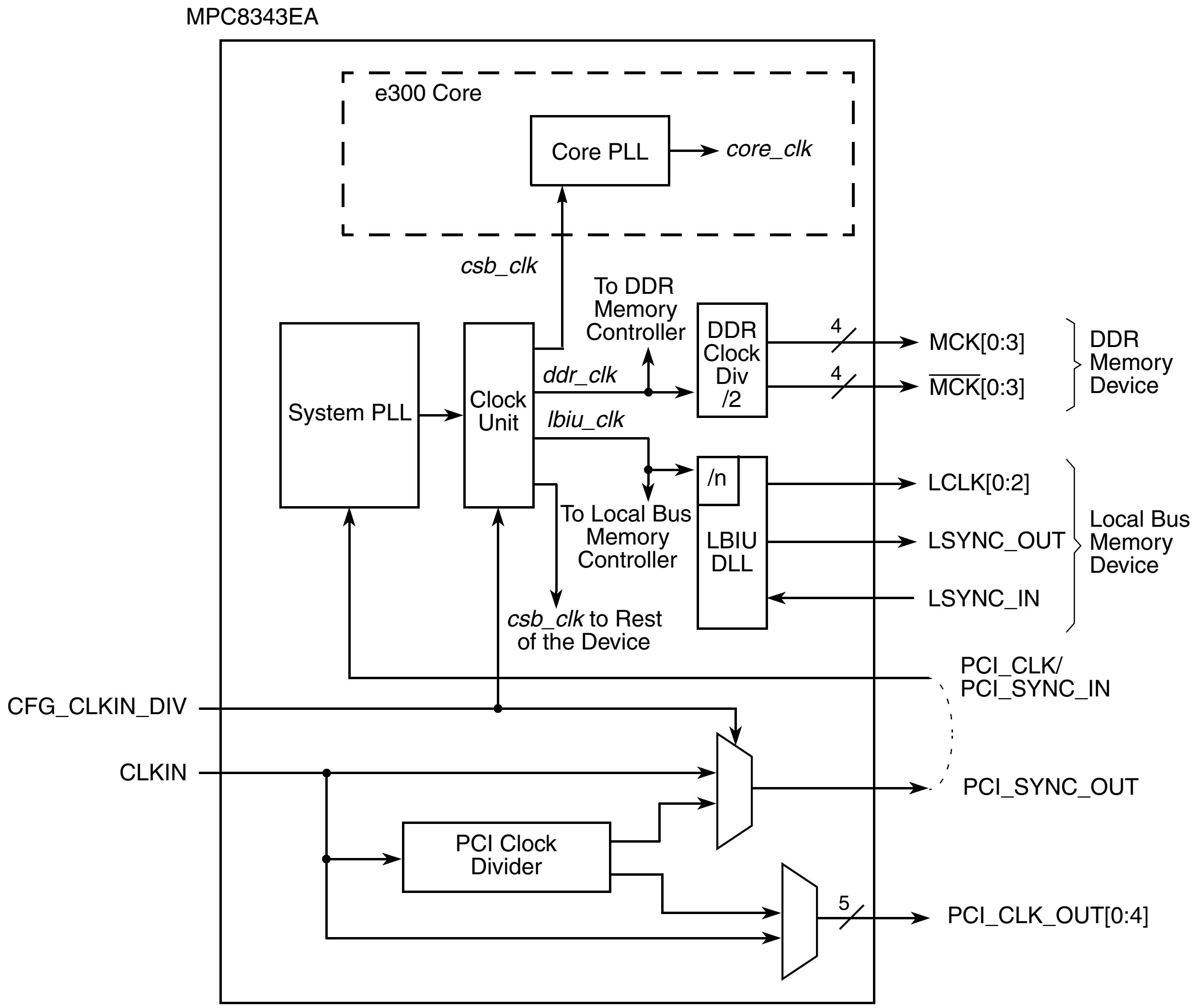



**Figure 37. MPC8343EA Clock Subsystem**

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8343EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8343EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

Table 53 provides the operating frequencies for the MPC8343EA PBGA under recommended operating conditions.

**Table 53. Operating Frequencies for PBGA**

| Parameter[1] | 266 MHz | 333 MHz | 400 MHz | Unit |
|---|---|---|---|---|
| e300 core frequency (*core_clk*) | 200–266 | 200–333 | 200–400 | MHz |
| Coherent system bus frequency (*csb_clk*) | 100–266 | | | MHz |
| DDR1 memory bus frequency (MCK)[2] | 100–133 | | | MHz |
| DDR2 memory bus frequency (MCK)[3] | 100–133 | | | MHz |
| Local bus frequency (LCLK*n*)[4] | 16.67–133 | | | MHz |
| PCI input frequency (CLKIN or PCI_CLK) | 25–66 | | | MHz |
| Security core maximum internal operating frequency | 133 | | | MHz |
| USB_DR, USB_MPH maximum internal operating frequency | 133 | | | MHz |

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.
2 The DDR data rate is 2× the DDR memory bus frequency.
3 The DDR data rate is 2× the DDR memory bus frequency.
4 The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBIUCM]).

## 19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 54 shows the multiplication factor encodings for the system PLL.

**Table 54. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | × 16 |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111 | × 7 |
| 1000 | × 8 |
| 1001 | × 9 |
| 1010 | × 10 |

**Table 54. System PLL Multiplication Factors (continued)**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 1011 | × 11 |
| 1100 | × 12 |
| 1101 | × 13 |
| 1110 | × 14 |
| 1111 | × 15 |

As described in Section 19, “Clocking,” the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 55 and Table 56 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

**Table 55. CSB Frequency Options for Host Mode**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0010 | 2 : 1 | | | | 133 |
| Low | 0011 | 3 : 1 | | | 100 | 200 |
| Low | 0100 | 4 : 1 | | 100 | 133 | 266 |
| Low | 0101 | 5 : 1 | | 125 | 166 | 333 |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |

**Table 55. CSB Frequency Options for Host Mode (continued)**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| High | 0010 | 2 : 1 | | | | 133 |
| High | 0011 | 3 : 1 | | | 100 | 200 |
| High | 0100 | 4 : 1 | | | 133 | 266 |
| High | 0101 | 5 : 1 | | | 166 | 333 |
| High | 0110 | 6 : 1 | | | 200 | |
| High | 0111 | 7 : 1 | | | 233 | |
| High | 1000 | 8 : 1 | | | | |

1 CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.
2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

**Table 56. CSB Frequency Options for Agent Mode**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0010 | 2 : 1 | | | | 133 |
| Low | 0011 | 3 : 1 | | | 100 | 200 |
| Low | 0100 | 4 : 1 | | 100 | 133 | 266 |
| Low | 0101 | 5 : 1 | | 125 | 166 | 333 |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |
| High | 0010 | 4 : 1 | | 100 | 133 | 266 |

**Table 58. Suggested PLL Configurations (continued)**

| Ref No.[1] | RCWL | | 266 MHz Device | | | 333 MHz Device | | | 400 MHz Device | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | SPMF | CORE PLL | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) |
| **326** | **0011** | **0100110** | | — | | 33 | 100 | 300 | 33 | 100 | 300 |
| **623** | **0110** | **0100011** | | — | | 33 | 200 | 300 | 33 | 200 | 300 |
| **922** | **1001** | **0100010** | | — | | 33 | 300 | 300 | 33 | 300 | 300 |
| **425** | **0100** | **0100101** | | — | | 33 | 133 | 333 | 33 | 133 | 333 |
| **524** | **0101** | **0100100** | | — | | 33 | 166 | 333 | 33 | 166 | 333 |
| **A22** | **1010** | **0100010** | | — | | 33 | 333 | 333 | 33 | 333 | 333 |
| **723** | **0111** | **0100011** | | — | | | — | | 33 | 233 | 350 |
| **604** | **0110** | **0000100** | | — | | | — | | 33 | 200 | 400 |
| **624** | **0110** | **0100100** | | — | | | — | | 33 | 200 | 400 |
| 823 | 1000 | 0100011 | | — | | | — | | 33 | 266 | 400 |
| **66 MHz CLKIN/PCI_CLK Options** | | | | | | | | | | | |
| **242** | **0010** | **1000010** | 66 | 133 | 133 | 66 | 133 | 133 | 66 | 133 | 133 |
| **322** | **0011** | **0100010** | 66 | 200 | 200 | 66 | 200 | 200 | 66 | 200 | 200 |
| **224** | **0010** | **0100100** | 66 | 133 | 266 | 66 | 133 | 266 | 66 | 133 | 266 |
| **422** | **0100** | **0100010** | 66 | 266 | 266 | 66 | 266 | 266 | 66 | 266 | 266 |
| **323** | **0011** | **0100011** | | — | | 66 | 200 | 300 | 66 | 200 | 300 |
| **223** | **0010** | **0100101** | | — | | 66 | 133 | 333 | 66 | 133 | 333 |
| **522** | **0101** | **0100010** | | — | | 66 | 333 | 333 | 66 | 333 | 333 |
| **304** | **0011** | **0000100** | | — | | | — | | 66 | 200 | 400 |
| **324** | **0011** | **0100100** | | — | | | — | | 66 | 200 | 400 |
| **403** | **0100** | **0000011** | | — | | | — | | 66 | 266 | 400 |
| **423** | **0100** | **0100011** | | — | | | — | | 66 | 266 | 400 |

[1] The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

[2] The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

### 20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_A$ = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D$ = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

### 20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter ($\Psi_{JT}$) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_T$ = thermocouple temperature on top of package (°C)

$\Psi_{JT}$ = junction-to-ambient thermal resistance (°C/W)

$P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so

**Table 60. Heat Sink and Thermal Resistance of MPC8343EA (PBGA) (continued)**

| Heat Sink Assuming Thermal Grease | Air Flow | 29 × 29 mm PBGA Thermal Resistance |
|---|---|---|
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 1 m/s | 7.7 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 2 m/s | 6.6 |
| MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass | 1 m/s | 6.9 |

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

| | |
|---|---|
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01801<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Dow-Corning Electronic Materials<br>P.O. Box 994<br>Midland, MI 48686-0997<br>Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| The Bergquist Company<br>18930 West 78th St.<br>Chanhassen, MN 55317<br>Internet: www.bergquistcompany.com | 800-347-4572 |

## 20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

### 20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_C$ = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$P_D$ = power dissipation (W)

# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8343EA.

## 21.1 System Clocking

The MPC8343EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, "System PLL Configuration."
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, "Core PLL Configuration."

## 21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The $AV_{DD}$ level should always equal to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 38, one to each of the four $AV_{DD}$ pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific $AV_{DD}$ pin being supplied. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of package, without the inductance of vias.

Figure 38 shows the PLL power supply filter circuit.

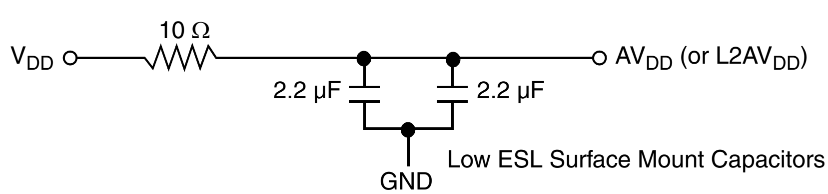



**Figure 38. PLL Power Supply Filter Circuit**

parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

**Table 62. Part Numbering Nomenclature**

| MPC | nnnn | e | t | pp | aa | a | r |
|---|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Encryption Acceleration** | **Temperature[1] Range** | **Package[2]** | **Processor Frequency[3]** | **Platform Frequency** | **Revision Level** |
| MPC | 8343 | Blank = Not included<br>E = included | Blank = 0 to 105°C<br>C = –40 to 105°C | ZQ = PBGA<br>VR = PB Free PBGA | e300 core speed<br>AD = 266<br>AG = 400 | D = 266 | B = 3.1 |

**Notes:**
1. For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266 and up to with a platform frequency of 333
2. See Section 18, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

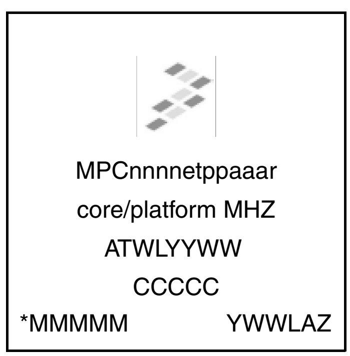
Table 63 shows the SVR settings by device and package type.

**Table 63. SVR Settings**

| Device | Package | SVR (Rev. 3.0) |
|---|---|---|
| MPC8343EA | PBGA | 8056_0030 |
| MPC8343A | PBGA | 8057_0030 |

## 22.2 Part Marking

Parts are marked as in the example shown in Figure 40.




PBGA

**Notes:**
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

**Figure 40. Freescale Part Marking for PBGA Devices**