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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8343ecvraddb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Table 5 shows the estimated typical I/O power dissipation for MPC8343EA.

Interface	Parameter	DDR2 GV _{DD} (1.8 V)	DDR1 GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 32 bits	0.31	0.42	_	_	_	W	—
65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	266 MHz, 32 bits	0.35	0.5				W	—
PCI I/O	33 MHz, 32 bits	_	_	0.04	_		W	—
10ad = 30 pF	66 MHz, 32 bits	_	_	0.07	_		W	—
Local bus I/O	167 MHz, 32 bits	_	_	0.34	_		W	—
10ad = 25 pF	133 MHz, 32 bits	_	_	0.27	_	_	W	—
	83 MHz, 32 bits	_	_	0.17	_	_	W	—
	66 MHz, 32 bits			0.14		_	W	—
	50 MHz, 32 bits			0.11		_	W	—
TSEC I/O	МІІ	_	_		0.01		W	Multiply by number
10ad = 25 pF	GMII or TBI				0.06	_	W	of interfaces used.
	RGMII or RTBI					0.04	W	
USB	12 MHz			0.01		_	W	—
	480 MHz	_	—	0.2	_	_	W	—
Other I/O		_	_	0.01	_	_	W	—

Table 5. MPC8343EA Typical I/O Power Dissipation

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8343EA.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V _{IH}	2.7	OV _{DD} + 0.3	V
Input low voltage	—	V _{IL}	-0.3	0.4	V
CLKIN input current	$0~V \leq V_{IN} \leq OV_{DD}$	I _{IN}	_	±10	μA





Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter	Symbol	Min	Typical	Мах	Unit	Notes
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t _{G125H} /t _{G125}	45 47	_	55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

- 1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
- 2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8343EA.

5.1 **RESET DC Electrical Characteristics**

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8343EA.

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±5	μA
Output high voltage ²	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

Table 9. RESET Pins DC Electrical Characteristics¹

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus V_{OH} is not relevant for those pins.



RESET Initialization

5.2 **RESET AC Electrical Characteristics**

Table 10 provides the reset initialization AC timing specifications of the MPC8343EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of HRESET or SRESET (input) to activate reset flow	32	—	t _{PCI_SYNC_IN}	1
Required assertion time of PORESET with stable clock applied to CLKIN when the MPC8343EA is in PCI host mode	32	—	t _{CLKIN}	2
Required assertion time of $\overrightarrow{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8343EA is in PCI agent mode	32	—	t _{PCI_SYNC_IN}	1
HRESET/SRESET assertion (output)	512	—	t _{PCI_SYNC_IN}	1
HRESET negation to SRESET negation (output)	16	—	t _{PCI_SYNC_IN}	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8343EA is in PCI host mode	4	_	t _{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8343EA is in PCI agent mode	4	—	t _{PCI_SYNC_IN}	1
Input hold time for POR configuration signals with respect to negation of HRESET	0	—	ns	—
Time for the MPC8343EA to turn off POR configuration signals with respect to the assertion of $\overrightarrow{\text{HRESET}}$	—	4	ns	3
Time for the MPC8343EA to turn on POR configuration signals with respect to the negation of HRESET	1		t _{PCI_SYNC_IN}	1, 3

Notes:

1. t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual.

3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."



DDR and DDR2 SDRAM

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol	Min	Max	Unit	Notes
266 MHz		-750	750		
200 MHz		-750	750		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: t_{DISKEW} = ± (T/4 – abs (t_{CISKEW})); where T is the clock period and abs (t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.



Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	7.5	10	ns	2
ADDR/CMD/MODT output setup with respect to MCK	t _{DDKHAS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		

NP

DDR and DDR2 SDRAM

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
- 4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual for the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).



Figure 6. Timing Diagram for t_{DDKHMH}



8.1.1 **TSEC DC Electrical Characteristics**

MII, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage 3.3 V	LV_{DD}^2	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -4.0 mA	$LV_{DD} = Min$	2.40	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 4.0 mA	$LV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—	—	2.0	LV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	—	-0.3	0.90	V
Input high current	IIH	$V_{IN}^{1} = LV_{DD}$		_	40	μA
Input low current	IIL	V _{IN} ¹ =	GND	-600		μA

Table 23. MII DC Electrical Characteristics

Notes:

1. The symbol V_{IN} in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

2. MII pins not needed for RGMII or RTBI operation are powered by the $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Мах	Unit
Supply voltage 2.5 V	LV _{DD}	—		2.37	2.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	$LV_{DD} = Min$	2.00	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND – 0.3	0.40	V
Input high voltage	V _{IH}	—	$LV_{DD} = Min$	1.7	LV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	$LV_{DD} = Min$	-0.3	0.70	V
Input high current	I _{IH}	$V_{IN}^{1} = LV_{DD}$		_	10	μA
Input low current	۱ _{IL}	V _{IN} ¹ =	GND	-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.





Figure 12 shows the RBMII and RTBI AC timing and multiplexing diagrams.

Figure 12. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC)—MII/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28 and Table 29.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (2.5 V)	LV _{DD}	-	_	2.37	2.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = Min$	2.00	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND – 0.3	0.40	V
Input high voltage	V _{IH}	—	LV _{DD} = Min	1.7	_	V
Input low voltage	V _{IL}	—	$LV_{DD} = Min$	-0.3	0.70	V

Table 28. MII Management DC Electrical Characteristics Powered at 2.5 V



USB

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8343EA.

9.1 USB DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the USB interface.

Table 31. USB DC Electrical Characteristics	Table 31. U	ISB DC	Electrical	Characteristics
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Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current	I _{IN}	—	±5	μA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} – 0.2	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 32 describes the general timing parameters of the USB interface of the MPC8343EA.

Table 32. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol ¹	Min	Max	Unit	Notes
USB clock cycle time	t _{USCK}	15	_	ns	2–5
Input setup to USB clock—all inputs	t _{USIVKH}	4	_	ns	2–5
Input hold to USB clock—all inputs	t _{USIXKH}	1	_	ns	2–5
USB clock to output valid—all outputs	t _{USKHOV}	—	7	ns	2–5
Output hold from USB clock—all outputs	t _{USKHOX}	2	_	ns	2–5

Notes:

 The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to USB clock.

3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.

4. Input timings are measured at the pin.

5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 14 and Figure 15 provide the AC test load and signals for the USB, respectively.



10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8343EA.

10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

 Table 33. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current	I _{IN}	_	±5	μA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	_	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	_	0.2	V





Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)



Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t _{I2CF}	—	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6	—	μS
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μS
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V

Table 39. I²C AC Electrical Specifications (continued)

Notes:

- 1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2DVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.
- 5.)The device does not follow the "I2C-BUS Specifications" version 2.1 regarding the tI2CF AC parameter.

Figure 28 provides the AC test load for the I^2C .



Figure 28. I²C AC Test Load

Figure 29 shows the AC timing diagram for the I^2C bus.



Figure 29. I²C Bus AC Timing Diagram



16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the external interrupt pins.

Table 47. IPIC DC Electrical Characteristics¹

Parameter	Symbol	Condition	Min	Мах	Unit	Notes
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	_	-0.3	0.8	V	—
Input current	I _{IN}	—	—	±5	μA	—
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V	2

Notes:

1. This table applies for pins \overline{IRQ} [0:7], \overline{IRQ} _OUT, and \overline{MCP} _OUT.

2. $\overline{IRQ_OUT}$ and $\overline{MCP_OUT}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 48 provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.

 IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 49 provides the SPI DC electrical characteristics.

Table 49. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V



Package and Pin Listings

18.3 Pinout Listings

Table 51 provides the pin-out listing for the MPC8343EA, 620-PBGA package.

Table 51. MPC8343EA (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI			
PCI1_INTA/IRQ_OUT	D20	0	OV _{DD}	2
PCI1_RESET_OUT	B21	0	OV _{DD}	—
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV _{DD}	—
PCI1_C/BE[3:0]	A17, A14, A11, B10	I/O	OV _{DD}	—
PCI1_PAR	D13	I/O	OV _{DD}	—
PCI1_FRAME	B14	I/O	OV _{DD}	5
PCI1_TRDY	A13	I/O	OV _{DD}	5
PCI1_IRDY	E13	I/O	OV _{DD}	5
PCI1_STOP	C13	I/O	OV _{DD}	5
PCI1_DEVSEL	B13	I/O	OV _{DD}	5
PCI1_IDSEL	C17	I	OV _{DD}	—
PCI1_SERR	C12	I/O	OV _{DD}	5
PCI1_PERR	B12	I/O	OV _{DD}	5
PCI1_REQ[0]	A21	I/O	OV _{DD}	—
PCI1_REQ[1]/CPCI1_HS_ES	C19	I	OV _{DD}	—
PCI1_REQ[2:4]	C18, A19, E20	I	OV _{DD}	—
PCI1_GNT0	B20	I/O	OV _{DD}	—
PCI1_GNT1/CPCI1_HS_LED	C20	0	OV _{DD}	—
PCI1_GNT2/CPCI1_HS_ENUM	B19	0	OV _{DD}	—
PCI1_GNT[3:4]	A20, E18	0	OV _{DD}	—
M66EN	L26	I	OV _{DD}	—
	DDR SDRAM Memory Interface			
MDQ[0:31]	AC25, AD27, AD25, AH27, AE28, AD26, AD24, AF27, AF25, AF28, AH24, AG26, AE25, AG25, AH26, AH25, AG22, AH22, AE21, AD19, AE22, AF23, AE19, AG20, AG19, AD17, AE16, AF16, AF18, AG18, AH17, AH16	I/O	GV _{DD}	_



Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
OV _{DD}	B27, D3, D11, D19, E15, E23, F5, F8, F11, F14, F17, F20, G24, H23, H24, J6, J14, J17, J18, K4, L9, L20, L23, L25, M6, M9, M20, P5, P20, P23, R6, R9, R24, U23, V4, V6	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	_
MVREF1	AF19	I	DDR reference voltage	_
MVREF2	AE10	I	DDR reference voltage	_
	No Connection			
NC	A22, A23, A24, B22, B23, B24, C21, C22, C23, C24, D21, D22, D23, D24, E21, M27, M28, N26, N27, N28, P25, P26, P27, R28, T24, T25, T26, T27, T28, U27, U28, Y3, Y4, Y5, AA1, AA2, AA3, AA4, AB1, AB2, AB3, AB4, AC1, AC2, AC3, AC4, AD1, AD2, AD3, AD5, AD7, AD11, AD12, AE4, AE6, AE8, AE9, AE23, AF1, AF5, AF6, AF8, AF24, AG1, AG3, AG4, AG7, AG8, AG9, AG10, AH2, AH3, AH5, AH8, AH9, V5, V2, V1	_	_	_

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.

2. This pin is an open-drain signal. A weak pull-up resistor (2-10 kΩ) should be placed on this pin to OV_{DD}.

3. During reset, this output is actively driven rather than three-stated.

4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.

6. This pin must be always be tied to GND.

7. This pin must always be pulled up to OV_{DD}.

8. Thermal sensitive resistor.

9. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.

10.TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

11. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to LV_{DD1}.

12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pull up on LGPL4 is required.



20 Thermal

This section describes the thermal specifications of the MPC8343EA.

20.1 Thermal Characteristics

.Table 59 provides the package thermal characteristics for the 62029×29 mm PBGA of the MPC8343EA.

Parameter	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{ ext{ heta}JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{ ext{ heta}JMA}$	15	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{ hetaJMA}$	17	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{ hetaJMA}$	12	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	°C/W	4
Junction-to-case thermal	$R_{ ext{ heta}JC}$	5	°C/W	5
Junction-to-package natural convection on top	ΨJT	5	°C/W	6

Table 59. Package Thermal Characteristics for PBGA

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3. Per JEDEC JESD51-6 with the board horizontal.

4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_J = junction temperature (°C)

 T_A = ambient temperature for the package (°C)

 $R_{\theta IA}$ = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

NP

Thermal

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_I = junction temperature (°C)

 T_A = ambient temperature for the package (°C)

 $R_{\theta IA}$ = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_I = junction temperature (°C)

 T_T = thermocouple temperature on top of package (°C)

 Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so



System Design Information

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8343EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8343EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8343EA.

21.5 Output Buffer DC Impedance

The MPC8343EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 39). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals



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However, while HRESET is asserted, these pins are treated as inputs, and the value on these pins is latched when PORESET deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8343EA requires high resistance pull-up resistors (10 k Ω is recommended) on open-drain pins, including I²C pins, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, "PowerQUICC Design Checklist."

22 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8343EEC).

22.1 Part Numbers Fully Addressed by This Document

Table 62 shows an analysis of the Freescale part numbering nomenclature for the MPC8343EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration



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parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

MPC	nnnn	е	t	рр	aa	а	r
Product Code	Part Identifier	Encryption Acceleration	Temperature ¹ Range	Package ²	Processor Frequency ³	Platform Frequency	Revision Level
MPC	8343	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400	D = 266	B = 3.1

Table 62. Part Numbering Nomenclature

Notes:

1. For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266 and up to with a platform frequency of 333

2. See Section 18, "Package and Pin Listings," for more information on available package types.

 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

Table 63 shows the SVR settings by device and package type.

Table 63. SVR Settings

Device	Package SVR (Rev. 3.0)	
MPC8343EA	PBGA	8056_0030
MPC8343A	A PBGA 8057_0030	

22.2 Part Marking

Parts are marked as in the example shown in Figure 40.



Figure 40. Freescale Part Marking for PBGA Devices



Document Revision History

23 Document Revision History

This table provides a revision history of this document.

Table 64.	Document	Revision	History
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Rev. Number	Date	Substantive Change(s)
11	09/2011	 In Section 2.2, "Power Sequencing," added Section 2.2.1, "Power-Up Sequencing" and Figure 4. In Table 25, Table 29, and Table 27, removed the GTX_CLK125. In Table 30, updated t_{MDKHDX} Max value from 170ns to 70ns.
10	11/2010	 In Table 51, added overbar to LCS[4] and LCS[5] signals. In Table 51 added note for pin LGPL4. In Section 21.7, "Pull-Up Resistor Requirements, updated the list of open drain type pins.
9	05/2010	 In Table 25 through Table 26, changed V_{IL}(min) to V_{IH}(max) to (20%–80%). Added Table 8, "EC_GTX_CLK125 AC Timing Specifications."
8	5/2009	 In Section 18.1, "Package Parameters for the MPC8343EA PBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. In Table 53, added two columns for the DDR1 and DDR2 memory bus frequency. In Table 62, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.
7	2/2009	 Added footnote 6 to Table 7. In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. In Table 35, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 18, Figure 20, and Figure 21 for output signals. Added footnote 10 to Table 51. In Table 51, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net." In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the four AVDD pins." In Table 62, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266."
6	4/2007	 In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. In Section 21.7, "Pull-Up Resistor Requirements,"deleted last two paragraphs and after first paragraph, added a new paragraph. Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
5	3/2007	 Page 1, updated first paragraph to reflect PowerQUICC II Pro information. In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. In Figure 38, "JTAG Interface Connection," updated with new figure. In Figure 38, "JTAG Interface Connection," updated with new figure. In Section 23, "Ordering Information," replaced first paragraph and added a note. In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T _{ddkhds} for 333 MHz from 900 ps to 775 ps.