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Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8343ezqadb

5.2 RESET AC Electrical Characteristics

Table 10 provides the reset initialization AC timing specifications of the MPC8343EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{\text{PCI_SYNC_IN}}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8343EA is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8343EA is in PCI agent mode	32	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ / $\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8343EA is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8343EA is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8343EA to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8343EA to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

- $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
- t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
- POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

- DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
- The csb_clk is determined by the CLKIN and system PLL ratio. See [Section 19, "Clocking."](#)

Table 21. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8343EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—MII/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII interface is defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 TSEC DC Electrical Characteristics

MII, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 23](#) and [Table 24](#). The RGMII and RTBI signals in [Table 24](#) are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}^2	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	40	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-600	—	μA

Notes:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).
2. MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$LV_{DD} = \text{Min}$	1.7	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	$LV_{DD} = \text{Min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Table 30. MII Management AC Timing Specifications (continued)

At recommended operating conditions with V_{DD} is 3.3 V \pm 10% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 13 shows the MII management AC timing diagram.

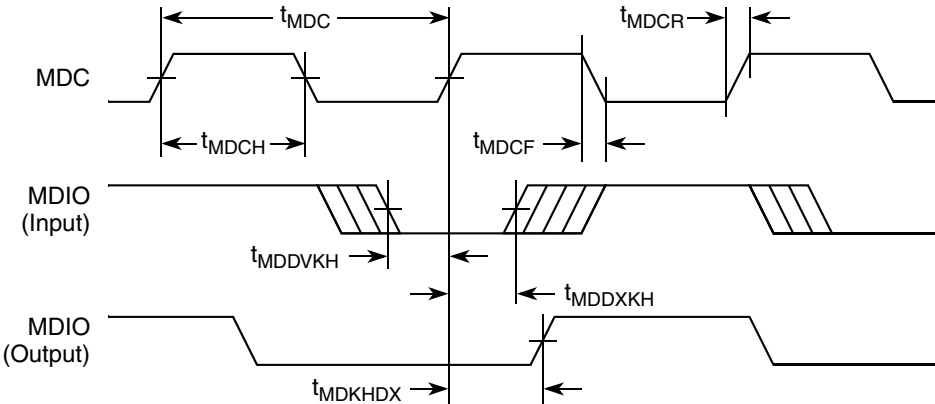


Figure 13. MII Management Interface Timing Diagram

Figure 14 and Figure 15 provide the AC test load and signals for the USB, respectively.

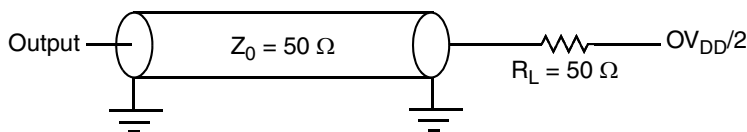


Figure 14. USB AC Test Load

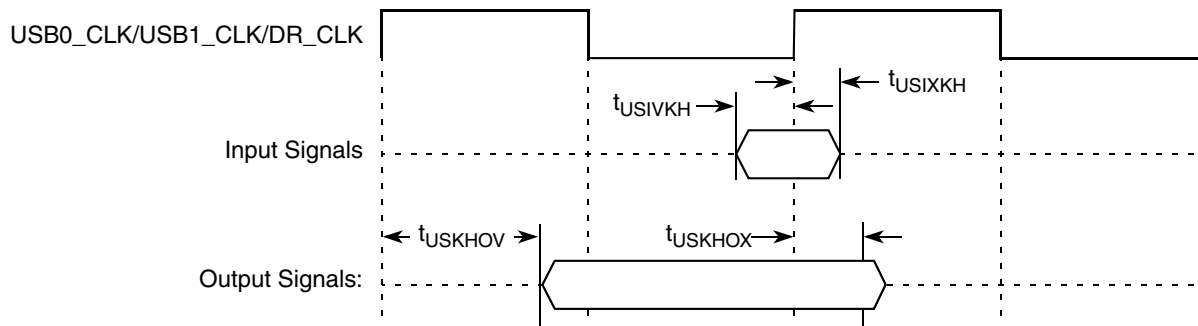


Figure 15. USB Signals

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8343EA.

10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

Table 33. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}	—	± 5	μA
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V

Table 35. Local Bus General Timing Parameters—DLL Bypass⁹

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKLOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for \overline{LGTA} and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin equals to the load on the LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 16 provides the AC test load for the local bus.

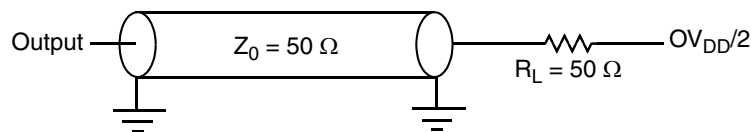
**Figure 16. Local Bus C Test Load**

Figure 17 through Figure 22 show the local bus signals.

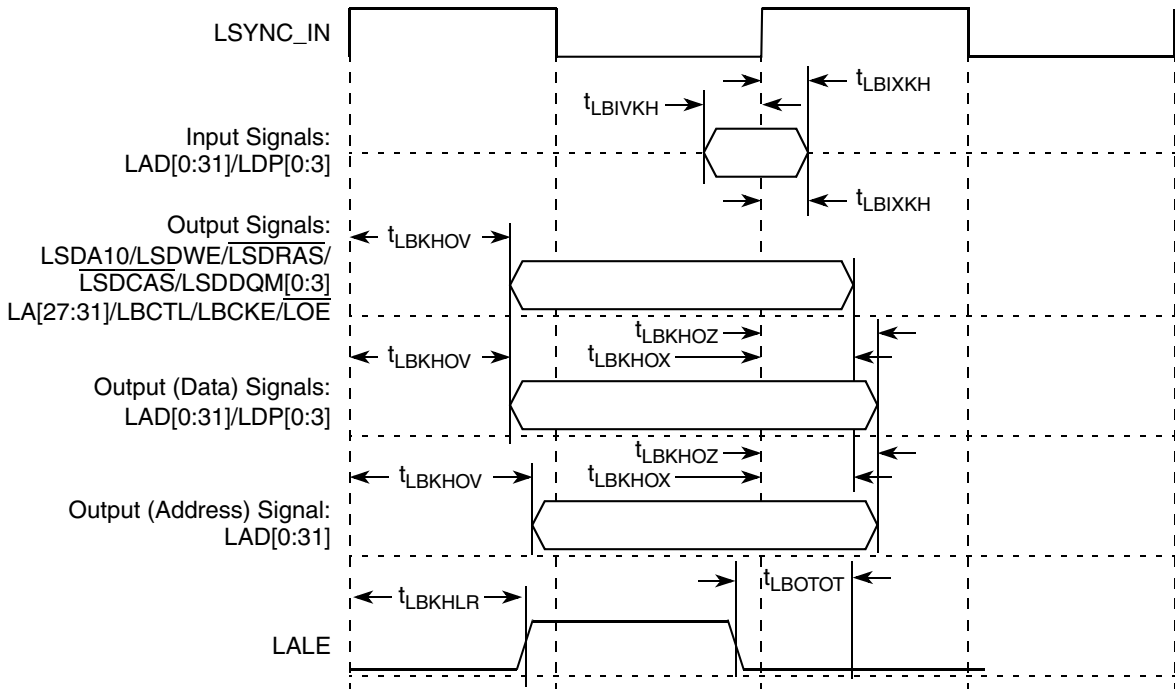


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

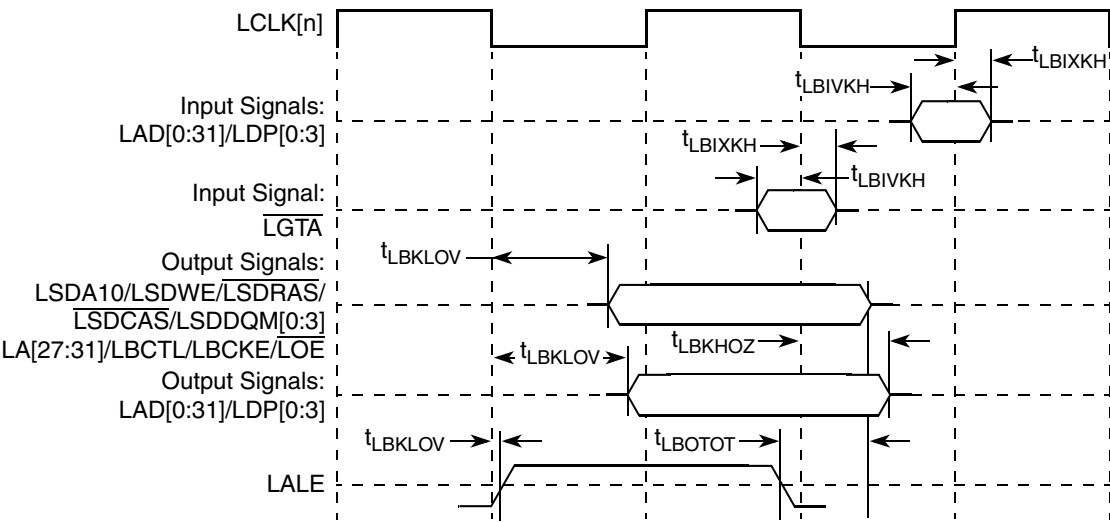


Figure 18. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

Figure 26 provides the boundary-scan timing diagram.

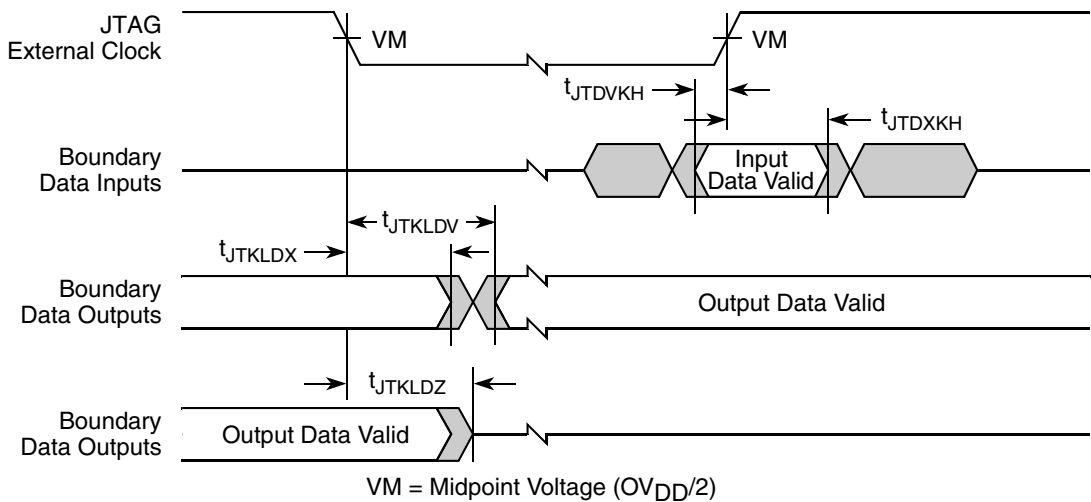


Figure 26. Boundary-Scan Timing Diagram

Figure 27 provides the test access port timing diagram.

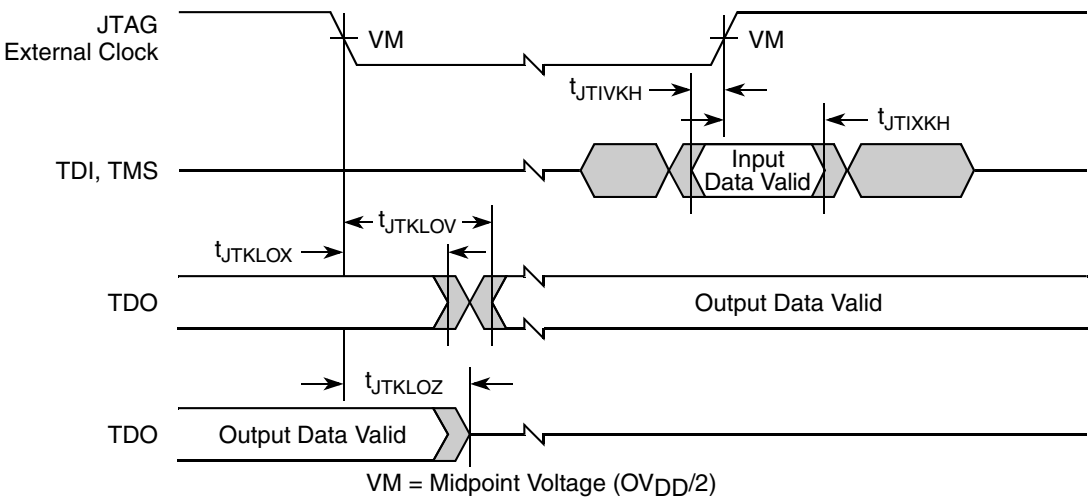


Figure 27. Test Access Port Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8343EA.

13.1 PCI DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the PCI interface of the MPC8343EA.

Table 40. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^1 = 0 \text{ V or } V_{IN} = OV_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min, } I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$	—	0.2	V

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8343EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 41 provides the PCI AC timing specifications at 66 MHz.

Table 41. PCI AC Timing Specifications at 66 MHz¹

Parameter	Symbol ²	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

Table 41. PCI AC Timing Specifications at 66 MHz¹ (continued)

Parameter	Symbol ²	Min	Max	Unit	Notes
Input hold from clock	t_{PCIXKH}	0	—	ns	3, 5

Notes:

1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHEV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

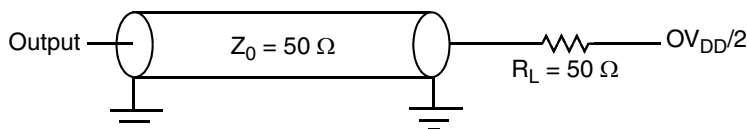
Table 42. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHEV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 30 provides the AC test load for PCI.


Figure 30. PCI AC Test Load

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the external interrupt pins.

Table 47. IPIC DC Electrical Characteristics¹

Parameter	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	—	−0.3	0.8	V	—
Input current	I_{IN}	—	—	±5	μA	—
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V	2
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	2

Notes:

1. This table applies for pins $\overline{IRQ}[0:7]$, $\overline{IRQ_OUT}$, and $\overline{MCP_OUT}$.
2. $\overline{IRQ_OUT}$ and $\overline{MCP_OUT}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 48 provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 49 provides the SPI DC electrical characteristics.

Table 49. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_DV	U24	I	LV _{DD1}	—
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV _{DD}	—
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV _{DD1}	—
TSEC1_TX_CLK	N25	I	OV _{DD}	—
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV _{DD1}	10
TSEC1_TX_EN	W27	O	LV _{DD1}	—
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV _{DD}	—
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV _{DD2}	—
TSEC2_GTX_CLK	AC27	O	LV _{DD2}	—
TSEC2_RX_CLK	AB25	I	LV _{DD2}	—
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV _{DD2}	—
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV _{DD2}	—
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV _{DD}	—
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV _{DD2}	—
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV _{DD}	—
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV _{DD}	—
UART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	B4, A4	O	OV _{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	D5, C5	I/O	OV _{DD}	—
UART_CTS[1]/MSRCID4/LSRCID4	B5	I/O	OV _{DD}	—
UART_CTS[2]/MDVAL/LDVAL	A5	I/O	OV _{DD}	—
UART_RTS[1:2]	D6, C6	O	OV _{DD}	—
I²C interface				
IIC1_SDA	E5	I/O	OV _{DD}	2
IIC1_SCL	A6	I/O	OV _{DD}	2
IIC2_SDA	B6	I/O	OV _{DD}	2
IIC2_SCL	E7	I/O	OV _{DD}	2

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SPI				
SPIMOSI/ $\overline{\text{LCS}}[6]$	D7	I/O	OV_{DD}	—
SPIMISO/ $\overline{\text{LCS}}[7]$	C7	I/O	OV_{DD}	—
SPICLK	B7	I/O	OV_{DD}	—
SPISEL	A7	I	OV_{DD}	—
Clocks				
PCI_CLK_OUT[0:2]	Y1, W3, W2	O	OV_{DD}	—
PCI_CLK_OUT[3]/ $\overline{\text{LCS}}[6]$	W1	O	OV_{DD}	—
PCI_CLK_OUT[4]/ $\overline{\text{LCS}}[7]$	V3	O	OV_{DD}	—
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV_{DD}	—
PCI_SYNC_OUT	U5	O	OV_{DD}	3
RTC/PIT_CLOCK	E9	I	OV_{DD}	—
CLKIN	W5	I	OV_{DD}	—
JTAG				
TCK	H27	I	OV_{DD}	—
TDI	H28	I	OV_{DD}	4
TDO	M24	O	OV_{DD}	3
TMS	J27	I	OV_{DD}	4
$\overline{\text{TRST}}$	K26	I	OV_{DD}	4
Test				
TEST	F28	I	OV_{DD}	6
TEST_SEL	T3	I	OV_{DD}	7
PMC				
$\overline{\text{QUIESCE}}$	K27	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	K28	I	OV_{DD}	—
$\overline{\text{HRESET}}$	M25	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	L27	I/O	OV_{DD}	2
Thermal Management				
THERM0	B15	I	—	8

19 Clocking

Figure 37 shows the internal distribution of the clocks.

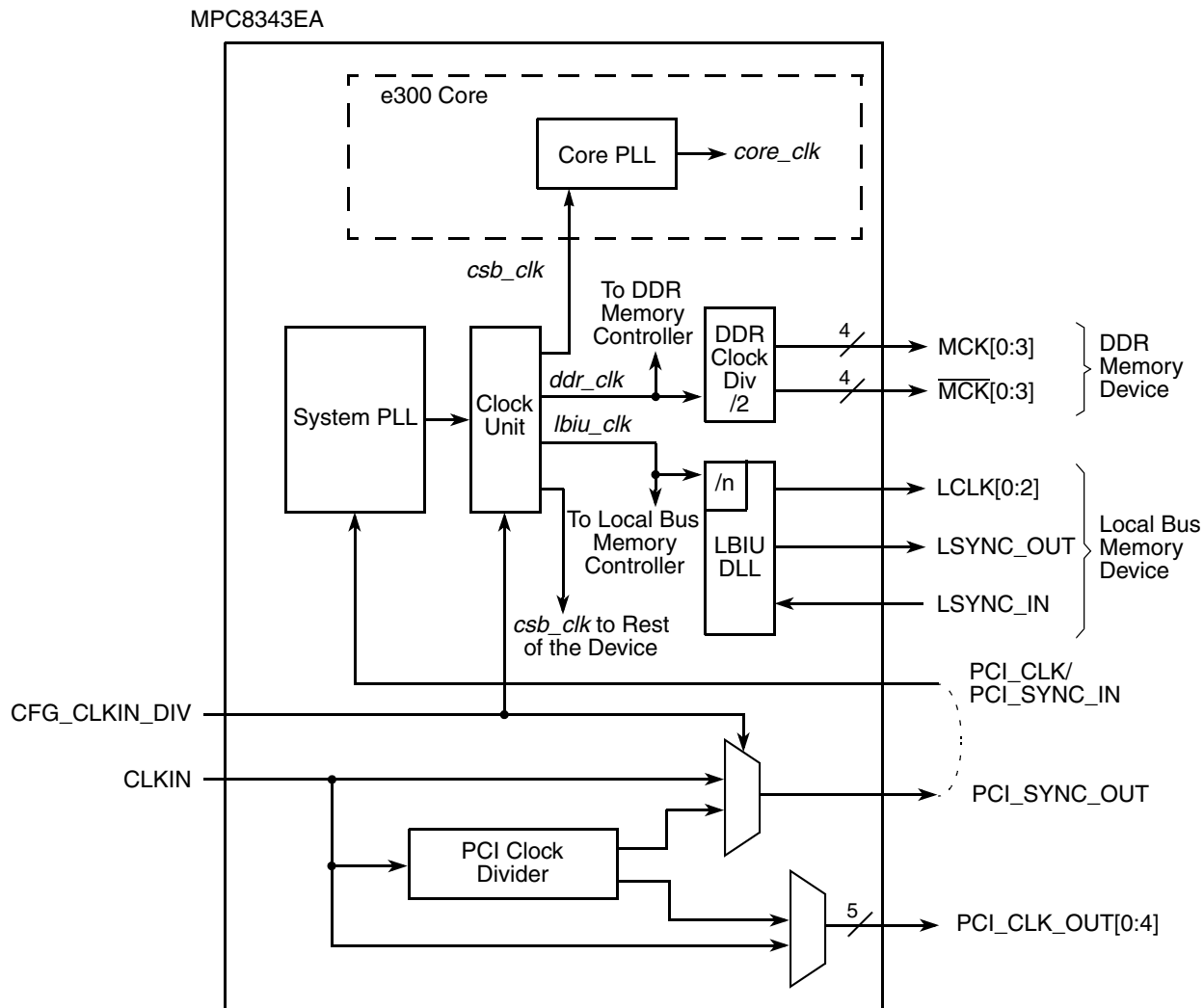


Figure 37. MPC8343EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8343EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider ($\div 2$) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8343EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

Table 58. Suggested PLL Configurations (continued)

Ref No. ¹	RCWL		266 MHz Device			333 MHz Device			400 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
326	0011	0100110	—			33	100	300	33	100	300
623	0110	0100011	—			33	200	300	33	200	300
922	1001	0100010	—			33	300	300	33	300	300
425	0100	0100101	—			33	133	333	33	133	333
524	0101	0100100	—			33	166	333	33	166	333
A22	1010	0100010	—			33	333	333	33	333	333
723	0111	0100011	—			—			33	233	350
604	0110	0000100	—			—			33	200	400
624	0110	0100100	—			—			33	200	400
823	1000	0100011	—			—			33	266	400
66 MHz CLKIN/PCI_CLK Options											
242	0010	1000010	66	133	133	66	133	133	66	133	133
322	0011	0100010	66	200	200	66	200	200	66	200	200
224	0010	0100100	66	133	266	66	133	266	66	133	266
422	0100	0100010	66	266	266	66	266	266	66	266	266
323	0011	0100011	—			66	200	300	66	200	300
223	0010	0100101	—			66	133	333	66	133	333
522	0101	0100010	—			66	333	333	66	333	333
304	0011	0000100	—			—			66	200	400
324	0011	0100100	—			—			66	200	400
403	0100	0000011	—			—			66	266	400
423	0100	0100011	—			—			66	266	400

¹ The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

² The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 62. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	Part Identifier	Encryption Acceleration	Temperature ¹ Range	Package ²	Processor Frequency ³	Platform Frequency	Revision Level
MPC	8343	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400	D = 266	B = 3.1

Notes:

1. For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266 and up to with a platform frequency of 333
2. See [Section 18, “Package and Pin Listings,”](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

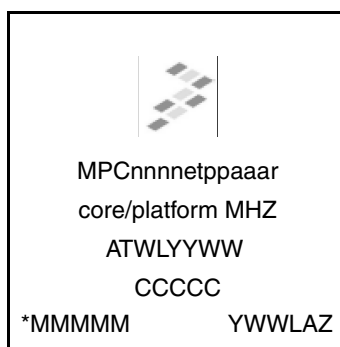
[Table 63](#) shows the SVR settings by device and package type.

Table 63. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8343EA	PBGA	8056_0030
MPC8343A	PBGA	8057_0030

22.2 Part Marking

Parts are marked as in the example shown in [Figure 40](#).



PBGA

Notes:

- ATWLYYWW is the traceability code.
- CCCCC is the country code.
- MMMMM is the mask number.
- YWWLAZ is the assembly traceability code.

Figure 40. Freescale Part Marking for PBGA Devices

23 Document Revision History

This table provides a revision history of this document.

Table 64. Document Revision History

Rev. Number	Date	Substantive Change(s)
11	09/2011	<ul style="list-style-type: none"> In Section 2.2, "Power Sequencing," added Section 2.2.1, "Power-Up Sequencing" and Figure 4. In Table 25, Table 29, and Table 27, removed the GTX_CLK125. In Table 30, updated t_{MDKHDX} Max value from 170ns to 70ns.
10	11/2010	<ul style="list-style-type: none"> In Table 51, added overbar to $\overline{LCS}[4]$ and $\overline{LCS}[5]$ signals. In Table 51 added note for pin LGPL4. In Section 21.7, "Pull-Up Resistor Requirements, updated the list of open drain type pins.
9	05/2010	<ul style="list-style-type: none"> In Table 25 through Table 26, changed $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$ to (20%–80%). Added Table 8, "EC_GTX_CLK125 AC Timing Specifications."
8	5/2009	<ul style="list-style-type: none"> In Section 18.1, "Package Parameters for the MPC8343EA PBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. In Table 53, added two columns for the DDR1 and DDR2 memory bus frequency. In Table 62, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.
7	2/2009	<ul style="list-style-type: none"> Added footnote 6 to Table 7. In Section 9.2, "USB AC Electrical Specifications, clarified that AC table is for ULPI only. In Table 35, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 18, Figure 20, and Figure 21 for output signals. Added footnote 10 to Table 51. In Table 51, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net." In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2)" from bulleted list. In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." In Table 62, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266."
6	4/2007	<ul style="list-style-type: none"> In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. In Section 21.7, "Pull-Up Resistor Requirements," deleted last two paragraphs and after first paragraph, added a new paragraph. Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
5	3/2007	<ul style="list-style-type: none"> Page 1, updated first paragraph to reflect PowerQUICC II Pro information. In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. In Figure 38, "JTAG Interface Connection," updated with new figure. In Figure 38, "JTAG Interface Connection," updated with new figure. In Section 23, "Ordering Information," replaced first paragraph and added a note. In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
4	12/2006	<p>Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T_{ddkhdS} for 333 MHz from 900 ps to 775 ps.</p>

Table 64. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
3	11/2006	<ul style="list-style-type: none"> Updated note in introduction. In the features list in Section 1, "Overview," updated DDR data rate to show 266 MHz for PBGA parts for all silicon revisions. In Table 57, "Suggested PLL Configurations," added the following row: Ref No: 823, SPMF: 1000, Core PLL: 0100011, 400-MHz Device Input Clock Freq: 33, CSB Freq: 266, and Core Freq: 400. In Section 23, "Ordering Information," replicated note from document introduction.
2	8/2006	<ul style="list-style-type: none"> Changed all references to revision 2.0 silicon to revision 3.0 silicon. Changed number of general purpose parallel I/O pins to 39 in Section 1, "Overview." Changed VIH minimum value in Table 35, "JTAG Interface DC Electrical Characteristics," to $OV_{DD} - 0.3$. In Table 40, "PCI DC Electrical Characteristics," changed high-level input voltage values to min = 2 and max = $OV_{DD} + 0.3$; changed low-level input voltage values to min = (-0.3) and max = 0.8. In Table 44, "PCI DC Electrical Characteristics," changed high-level input voltage values to min = 2 and max = $OV_{DD} + 0.3$; changed low-level input voltage values to min = (-0.3) and max = 0.8. In Table 44, "PCI DC Electrical Characteristics," changed high-level input voltage values to min = 2 and max = $OV_{DD} + 0.3$; changed low-level input voltage values to min = (-0.3) and max = 0.8. Updated DDR2 I/O power values in Table 5, "MPC8347EA Typical I/O Power Dissipation."
1	4/2006	<ul style="list-style-type: none"> Removed Table 20, "Timing Parameters for DDR2-400." Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, "DDR and DDR2 SDRAM Output AC Timing Specifications," rows 2 and 3, and in Figure 2, "DDR SDRAM Output Timing Diagram." Changed Min and Max values for V_{IH} and V_{IL} in Table 40Table 44, "PCI DC Electrical Characteristics." In Table 58, "MPC8343EA (PBGA) Pinout Listing," and Table 52, "MPC8347EA (PBGA) Pinout Listing," modified rows for MDICO and MDIC1 signals and added note 'It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor.' Table 58, "MPC8343EA (PBGA) Pinout Listing," in row AVDD3 changed power supply from "AVDD3" to '—.'
0	3/2006	Initial public release