Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8343ezqagdb

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8343EA.

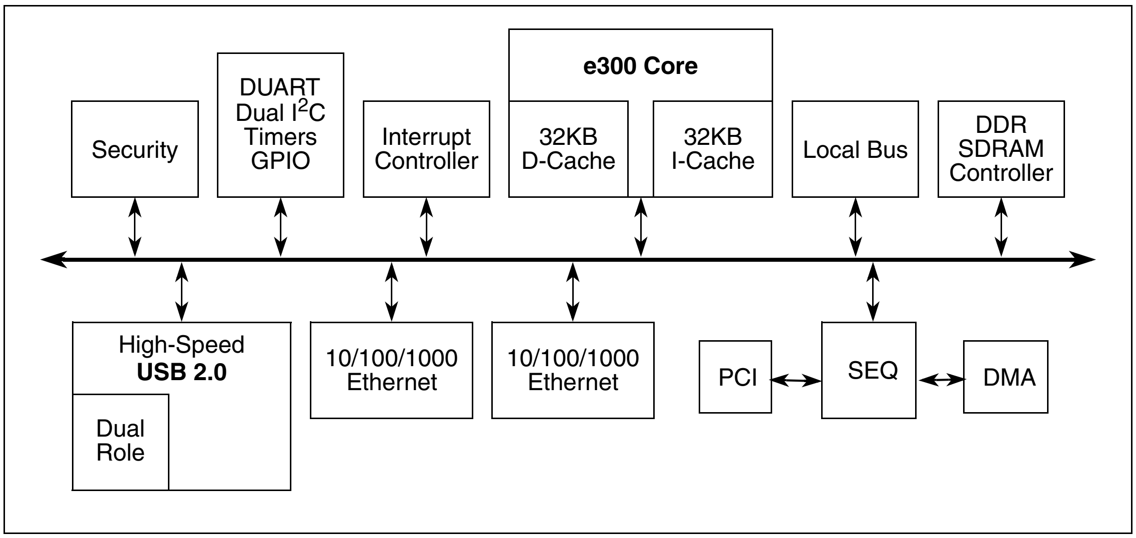


Figure 1. MPC8343EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 400 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- bit data interface, up to 266 MHz data rate

- Can operate as a stand-alone USB host controller
  - USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
  - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)

- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects for eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8343EA for the 3.3-V signals, respectively.

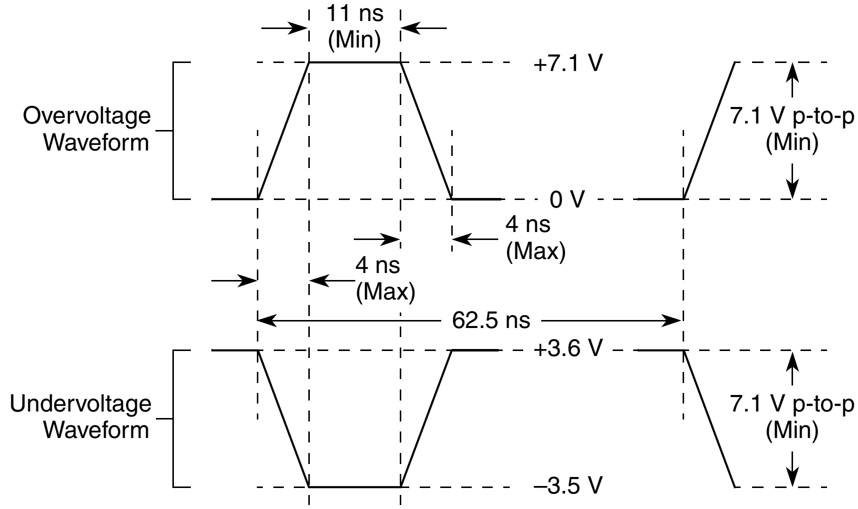


Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV_{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV_{DD} = 1.8 V
TSEC/10/100 signals	40	LV_{DD} = 2.5/3.3 V
DUART, system control, I^2C, JTAG, USB	40	OV_{DD} = 3.3 V
GPIO signals	40	OV_{DD} = 3.3 V, LV_{DD} = 2.5/3.3 V

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8343EA.

2.2.1 Power-Up Sequencing

MPC8343EAdoes not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

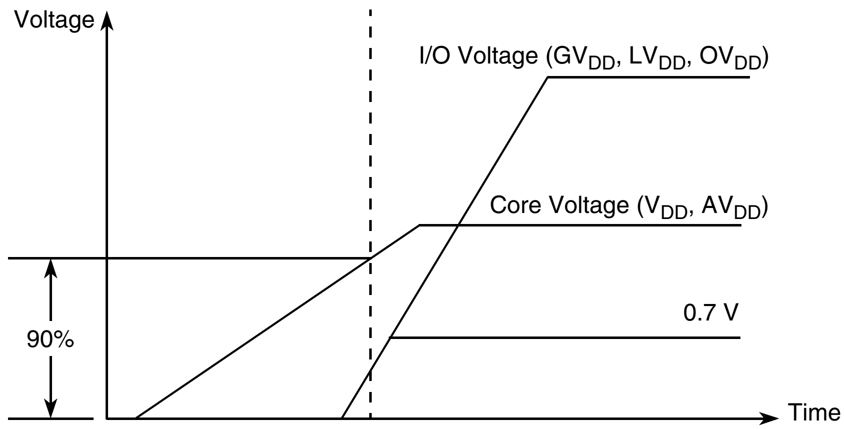


Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

3 Power Characteristics

The estimated typical power dissipation for the MPC8343EA device is shown in Table 4.

Table 4. MPC8343EA Power Dissipation[1]

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T_J = 65	Typical[2,3]	Maximum[4]	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W

1 The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.
2 Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
3 Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.
4 Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

Figure 12 shows the RBMII and RTBI AC timing and multiplexing diagrams.

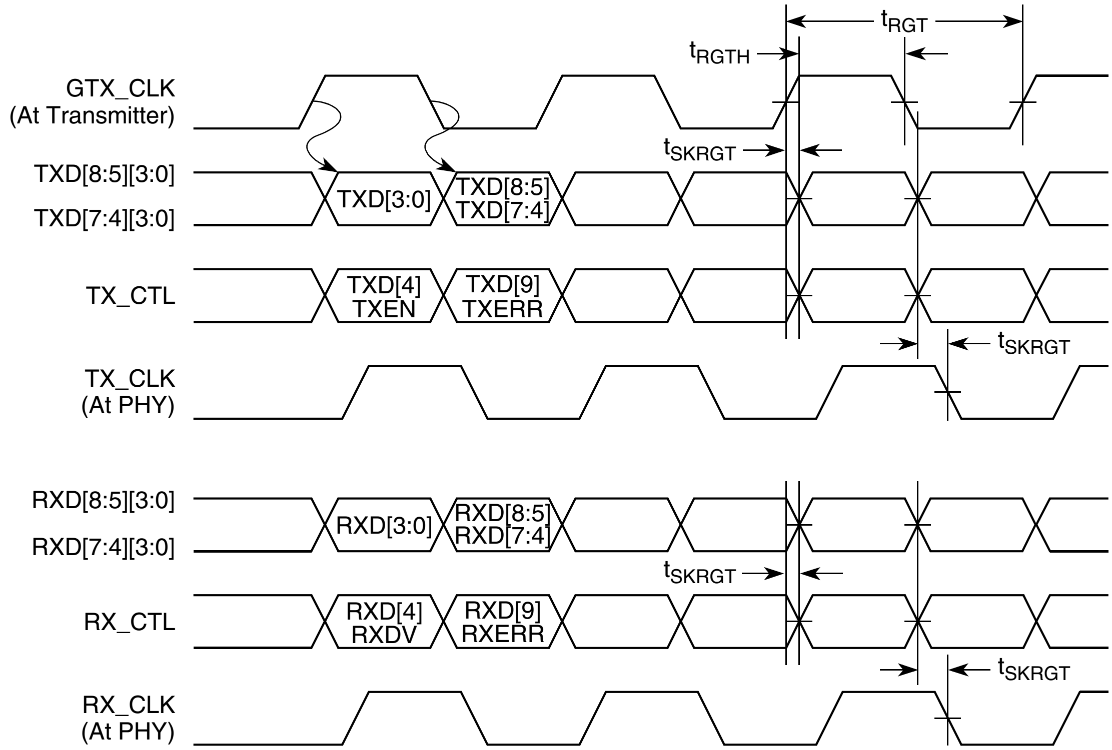


Figure 12. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC)—MII/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28 and Table 29.

Table 28. MII Management DC Electrical Characteristics Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	—	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V

Table 28. MII Management DC Electrical Characteristics Powered at 2.5 V (continued)

Parameter	Symbol	Conditions	Min	Max	Unit
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}	—	10	μA
Input low current	I_{IL}	$V_{IN} = LV_{DD}$	–15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 29. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	LV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.10	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	LV_{DD} = Max	V_{IN}[1] = 2.1 V	—	40	μA
Input low current	I_{IL}	LV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 30 provides the MII management AC timing specifications.

Table 30. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8343EA.

9.1 USB DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the USB interface.

Table 31. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 32 describes the general timing parameters of the USB interface of the MPC8343EA.

Table 32. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2–5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2–5

Notes:
1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from OV_{DD}/2 of the rising edge of the USB clock to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 14 and Figure 15 provide the AC test load and signals for the USB, respectively.

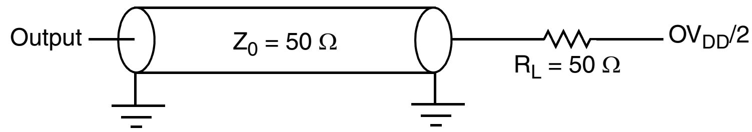


Figure 14. USB AC Test Load

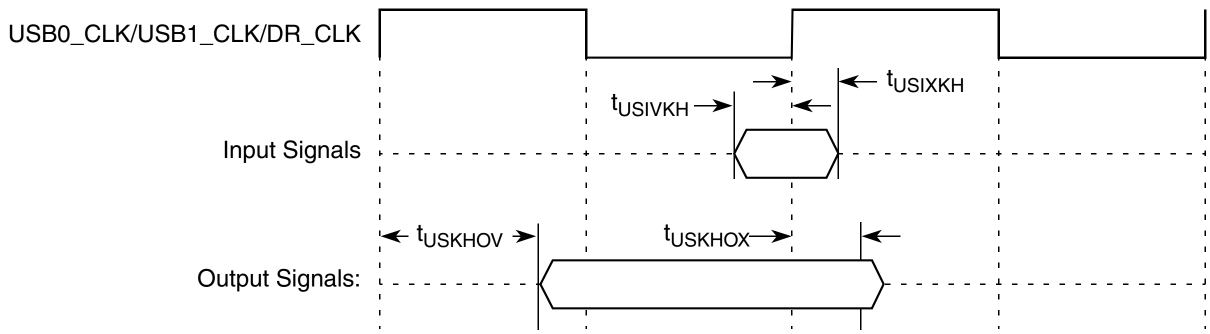


Figure 15. USB Signals

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8343EA.

10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

Table 33. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 23 provides the AC test load for TDO and the boundary-scan outputs of the MPC8343EA.

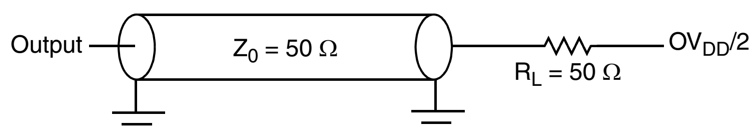


Figure 23. AC Test Load for the JTAG Interface

Figure 24 provides the JTAG clock input timing diagram.

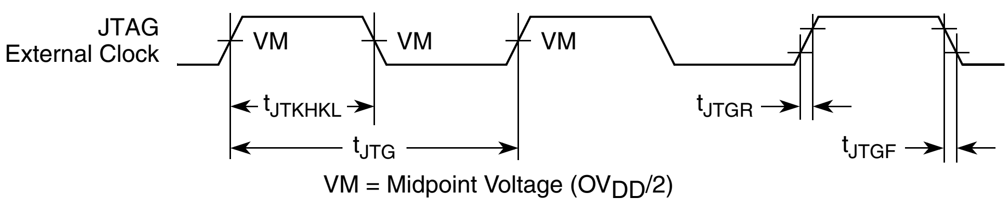


Figure 24. JTAG Clock Input Timing Diagram

Figure 25 provides the $\overline{\text{TRST}}$ timing diagram.

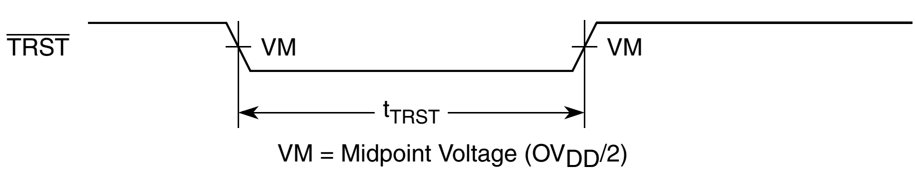


Figure 25. $\overline{\text{TRST}}$ Timing Diagram

12 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the MPC8343EA.

12.1 I^2C DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the I^2C interface of the MPC8343EA.

Table 38. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max))	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8349EA Integrated Host Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I^2C AC Electrical Specifications

Table 39 provides the AC timing parameters for the I^2C interface of the MPC8343EA. Note that all values refer to V_{IH}(min) and V_{IL}(max) levels (see Table 38).

Table 39. I^2C AC Electrical Specifications

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time:CBUS compatible masters I^2C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	μs

Table 39. I^2C AC Electrical Specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5.)The device does not follow the "I2C-BUS Specifications" version 2.1 regarding the t_{I2CF} AC parameter.

Figure 28 provides the AC test load for the I^2C.

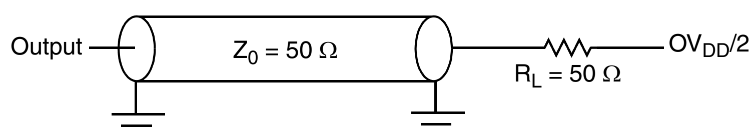


Figure 28. I^2C AC Test Load

Figure 29 shows the AC timing diagram for the I^2C bus.

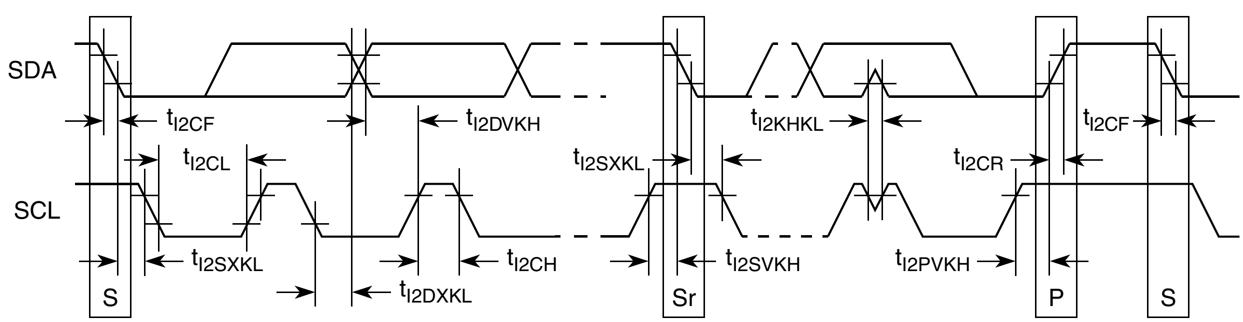
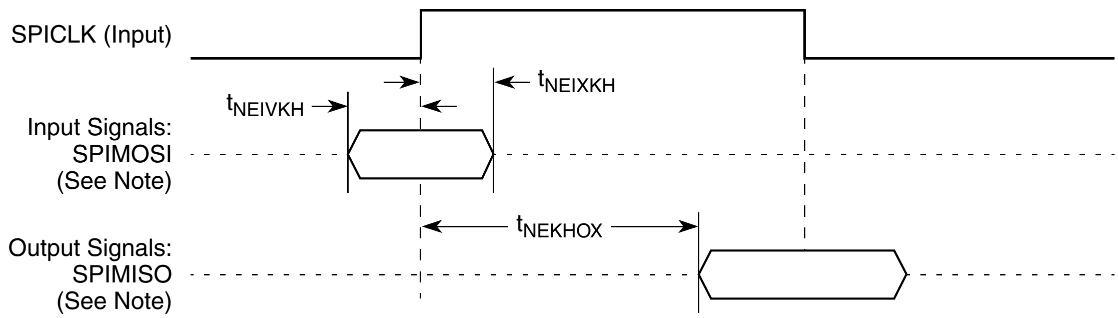


Figure 29. I^2C Bus AC Timing Diagram

Figure 34 and Figure 35 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

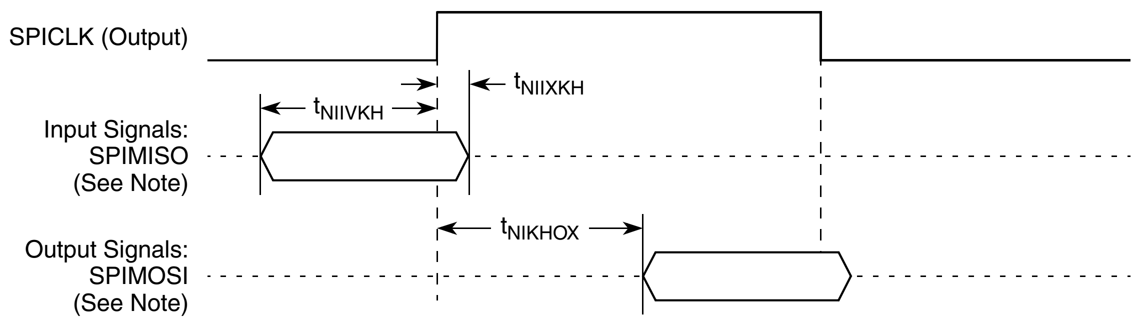
Figure 34 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 35 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8343EA is available in a plastic ball grid array (PBGA). See Section 18.1, “Package Parameters for the MPC8343EA PBGA,” and Section 18.2, “Mechanical Dimensions for the MPC8343EA PBGA.”

18.1 Package Parameters for the MPC8343EA PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm

Table 55. CSB Frequency Options for Host Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

[1] CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.
[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Table 56. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266

Table 56. CSB Frequency Options for Agent Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

1 CFG_CLKIN_DIV doubles csb_clk if set high.
2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 57 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 57 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

Table 57. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider[1]
0–1	2–5	6		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
11	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
11	**0001**	1	1.5:1	8

Table 58. Suggested PLL Configurations (continued)

Ref No.[1]	RCWL		266 MHz Device			333 MHz Device			400 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
326	0011	0100110	—			33	100	300	33	100	300
623	0110	0100011	—			33	200	300	33	200	300
922	1001	0100010	—			33	300	300	33	300	300
425	0100	0100101	—			33	133	333	33	133	333
524	0101	0100100	—			33	166	333	33	166	333
A22	1010	0100010	—			33	333	333	33	333	333
723	0111	0100011	—			—			33	233	350
604	0110	0000100	—			—			33	200	400
624	0110	0100100	—			—			33	200	400
823	1000	0100011	—			—			33	266	400
66 MHz CLKIN/PCI_CLK Options											
242	0010	1000010	66	133	133	66	133	133	66	133	133
322	0011	0100010	66	200	200	66	200	200	66	200	200
224	0010	0100100	66	133	266	66	133	266	66	133	266
422	0100	0100010	66	266	266	66	266	266	66	266	266
323	0011	0100011	—			66	200	300	66	200	300
223	0010	0100101	—			66	133	333	66	133	333
522	0101	0100010	—			66	333	333	66	333	333
304	0011	0000100	—			—			66	200	400
324	0011	0100100	—			—			66	200	400
403	0100	0000011	—			—			66	266	400
423	0100	0100011	—			—			66	266	400

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.
2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J – T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8343EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8343EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8343EA.

21.5 Output Buffer DC Impedance

The MPC8343EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 39). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals

Table 64. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
3	11/2006	• Updated note in introduction. • In the features list in Section 1, “Overview,” updated DDR data rate to show 266 MHz for PBGA parts for all silicon revisions. • In Table 57, “Suggested PLL Configurations,” added the following row: • Ref No: 823, SPMF: 1000, Core PLL: 0100011, 400-MHz Device Input Clock Freq: 33, CSB Freq: 266, and Core Freq: 400. • In Section 23, “Ordering Information,” replicated note from document introduction.
2	8/2006	• Changed all references to revision 2.0 silicon to revision 3.0 silicon. • Changed number of general purpose parallel I/O pins to 39 in Section 1, “Overview.” • Changed VIH minimum value in Table 35, “JTAG Interface DC Electrical Characteristics,” to OV_{DD} – 0.3. • In Table 40, “PCI DC Electrical Characteristics,” changed high-level input voltage values to min = 2 and max = OV_{DD} + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8. • In Table 44, “PCI DC Electrical Characteristics,” changed high-level input voltage values to min = 2 and max = OV_{DD} + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8. • In Table 44, “PCI DC Electrical Characteristics,” changed high-level input voltage values to min = 2 and max = OV_{DD} + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8. • Updated DDR2 I/O power values in Table 5, “MPC8347EA Typical I/O Power Dissipation.” •
1	4/2006	• Removed Table 20, “Timing Parameters for DDR2-400.” • Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, “DDR and DDR2 SDRAM Output AC Timing Specifications,” rows 2 and 3, and in Figure 2, “DDR SDRAM Output Timing Diagram. • Changed Min and Max values for V_{IH} and VIL in Table 40Table 44,“PCI DC Electrical Characteristics.” • In Table 58, “MPC8343EA (PBGA) Pinout Listing,” and Table 52, “MPC8347EA (PBGA) Pinout Listing,” modified rows for MDICO and MDIC1 signals and added note ‘It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor.’ • Table 58, “MPC8343EA (PBGA) Pinout Listing,” in row AVDD3 changed power supply from “AVDD3” to ‘—.’
0	3/2006	Initial public release

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