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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (3)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8343zqagdb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8343E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8343EA.



Figure 1. MPC8343EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 400 MHz
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
 - Programmable timing supporting DDR1 and DDR2 SDRAM
 - 32- bit data interface, up to 266 MHz data rate



Overview

- Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- DRAM chip configurations from 64 Mbits to 1 Gbit with $\times 8/\times 16$ data ports
- Full error checking and correction (ECC) support
- Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep-mode support for SDRAM self refresh
- Auto refresh
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3TM, 802.3uTM, 820.3xTM, 802.3zTM, 802.3acTM standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 RGMII, IEEE Std. 802.3z RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- PCI interface
 - Designed to comply with PCI Specification Revision 2.3
 - Data bus width:
 - 32-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities
 - PCI agent mode on PCI interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration supporting five masters on PCI
 - Accesses to all PCI address spaces
 - Parity supported
 - Selectable hardware-enforced coherency





- Can operate as a stand-alone USB host controller
 - USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects for eight external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
 - Three protocol engines on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user-programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
 - Programmable highest priority request
 - Four groups of interrupts with programmable priority
 - External and internal interrupts directed to host processor
 - Redirects interrupts to external INTA pin in core disable mode.
 - Unique vector number for each interrupt source
- Dual industry-standard I²C interfaces
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
 - System initialization data optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - Handshaking (external control) signals for all channels: DMA_DREQ[0:3], DMA_DACK[0:3], DMA_DDONE[0:3]
 - All channels accessible to local core and remote PCI masters



Electrical Characteristics

- Misaligned transfer capability
- Data chaining and direct mode
- Interrupt on completed segment and chain
- DUART
 - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
 - 39 parallel I/O pins multiplexed on various chip interfaces
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1[™], JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8343EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Parameter	Symbol	Max Value	Unit	Notes
Core supply voltage	V _{DD}	-0.3 to 1.32	V	_
PLL supply voltage	AV _{DD}	-0.3 to 1.32	V	_
DDR and DDR2 DRAM I/O voltage	GV _{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage	LV _{DD}	-0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C , and JTAG I/O voltage	OV _{DD}	-0.3 to 3.63	V	—

Table 1. Absolute Maximum Ratings¹



	Parameter	Symbol	Max Value	Unit	Notes
Input voltage	DDR DRAM signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV _{IN}	–0.3 to (LV _{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I ² C, and JTAG signals	OV _{IN}	–0.3 to (OV _{DD} + 0.3)	V	3, 5
	PCI	OV _{IN}	–0.3 to (OV _{DD} + 0.3)	V	6
Storage temperature ra	ange	T _{STG}	–55 to 150	°C	—

Table 1. Absolute Maximum Ratings¹ (continued)

Notes:

- ¹ Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- ² Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- ³ **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- ⁴ **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- ⁵ (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- 6 OVIN on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8343EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Parameter	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V _{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV _{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	LV _{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	LV _{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—

 Table 2. Recommended Operating Conditions



Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8343EA for the 3.3-V signals, respectively.



Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV _{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV _{DD} = 1.8 V
TSEC/10/100 signals	40	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, JTAG, USB	40	OV _{DD} = 3.3 V
GPIO signals	40	OV _{DD} = 3.3 V, LV _{DD} = 2.5/3.3 V

Table 3. Output Drive Capability

2.2 **Power Sequencing**

This section details the power sequencing considerations for the MPC8343EA.

2.2.1 Power-Up Sequencing

MPC8343EAdoes not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power



RESET Initialization

5.2 **RESET AC Electrical Characteristics**

Table 10 provides the reset initialization AC timing specifications of the MPC8343EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of HRESET or SRESET (input) to activate reset flow	32	—	t _{PCI_SYNC_IN}	1
Required assertion time of PORESET with stable clock applied to CLKIN when the MPC8343EA is in PCI host mode	32	—	t _{CLKIN}	2
Required assertion time of $\overrightarrow{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8343EA is in PCI agent mode	32	—	t _{PCI_SYNC_IN}	1
HRESET/SRESET assertion (output)	512	—	t _{PCI_SYNC_IN}	1
HRESET negation to SRESET negation (output)	16	—	t _{PCI_SYNC_IN}	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8343EA is in PCI host mode	4	_	t _{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8343EA is in PCI agent mode	4	—	t _{PCI_SYNC_IN}	1
Input hold time for POR configuration signals with respect to negation of HRESET	0	—	ns	—
Time for the MPC8343EA to turn off POR configuration signals with respect to the assertion of $\overrightarrow{\text{HRESET}}$	—	4	ns	3
Time for the MPC8343EA to turn on POR configuration signals with respect to the negation of HRESET	1		t _{PCI_SYNC_IN}	1, 3

Notes:

1. t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual.

3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."



DDR and DDR2 SDRAM

Table 13 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	_
Output leakage current	I _{OZ}	-9.9	-9.9	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	—	mA	_
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	—	mA	_

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Figure 14 and Figure 15 provide the AC test load and signals for the USB, respectively.



10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8343EA.

10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

 Table 33. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current	I _{IN}	_	±5	μA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	_	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	_	0.2	V



Local Bus



Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)



PCI

Table 41. PCI AC Timing Specifications at 66 MHz¹ (continued)

Parameter	Symbol ²	Min	Мах	Unit	Notes
Input hold from clock	t _{PCIXKH}	0	—	ns	3, 5

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.}
- 3. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

Table 42. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output valid	^t PCKHOV	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	—	ns	2
Clock to output high impedance	t _{PCKHOZ}	-	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	_	ns	2, 4

Notes:

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

Figure 30 provides the AC test load for PCI.



Figure 30. PCI AC Test Load

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>



GPIO

14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

Table 44. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8343EA GPIO.

Table 45. GPIO	DC Electrical	Characteristics
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PArameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	_	_	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 46 provides the GPIO input and output AC timing specifications.

Table 46. GPIO Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

 GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.



Figure 34 and Figure 35 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 34 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 35 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8343EA is available in a plastic ball grid array (PBGA). See Section 18.1, "Package Parameters for the MPC8343EA PBGA," and Section 18.2, "Mechanical Dimensions for the MPC8343EA PBGA."

18.1 Package Parameters for the MPC8343EA PBGA

The package parameters are as provided in the following list. The package type is $29 \text{ mm} \times 29 \text{ mm}$, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm



Package and Pin Listings

Module height (typical) Module height (minimum) Solder balls

Ball diameter (typical)

2.23 mm 2.00 mm 62 Sn/36 Pb/2 Ag (ZQ package) 96.5 Sn/3.5Ag (VR package) 0.60 mm



Package and Pin Listings

Table 51. MPC8343EA	(PBGA) Pinout	Listing	(continued))
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	AG13, AE14, AH12, AH10, AE15	I/O	GV _{DD}	—
MECC[5]/MDVAL	AH14	I/O	GV _{DD}	—
MECC[6:7]	AE13, AH11	I/O	GV _{DD}	—
MDM[0:3]	AG28, AG24, AF20, AG17	0	GV _{DD}	—
MDM[8]	AG12	0	GV _{DD}	—
MDQS[0:3]	AE27, AE26, AE20, AH18	I/O	GV _{DD}	—
MDQS[8]	AH13	I/O	GV _{DD}	—
MBA[0:1]	AF10, AF11	0	GV _{DD}	—
MA[0:14]	AF13, AF15, AG16, AD16, AF17, AH20, AH19, AH21, AD18, AG21, AD13, AF21, AF22, AE1, AA5	0	GV _{DD}	_
MWE	AD10	0	GV _{DD}	—
MRAS	AF7	0	GV _{DD}	—
MCAS	AG6	0	GV _{DD}	—
MCS[0:3]	AE7, AH7, AH4, AF2	0	GV _{DD}	—
MCKE[0:1]	AG23, AH23	0	GV _{DD}	3
MCK[0:3]	AH15, AE24, AE2, AF14	0	GV _{DD}	—
MCK[0:3]	AG15, AD23, AE3, AG14	0	GV _{DD}	—
MODT[0:3]	AG5, AD4, AH6, AF4	0	GV _{DD}	—
MBA[2]	AD22	0	GV _{DD}	—
MDIC0	AG11	I/O	—	9
MDIC1	AF12	I/O	—	9
	Local Bus Controller Interface			
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	H1	I/O	OV _{DD}	—
LDP[1]/CKSTOP_IN	К5	I/O	OV _{DD}	—
LDP[2]/LCS[4]	H2	I/O	OV _{DD}	—
LDP[3]/ LCS [5]	G1	I/O	OV _{DD}	—
LA[27:31]	J4, H3, G2, F1, G3	0	OV _{DD}	—
LCS[0:3]	J5, H4, F2, E1	0	OV _{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	F3, G4, D1, E2	0	OV _{DD}	—



Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	Power and Ground Signals			
AV _{DD} 1	C15	Power for e300 PLL (1.2 V)	AV _{DD} 1	—
AV _{DD} 2	U1	Power for system PLL (1.2 V)	AV _{DD} 2	
AV _{DD} 3	AF9	Power for DDR DLL (1.2 V)	_	
AV _{DD} 4	U2	Power for LBIU DLL (1.2 V)	AV _{DD} 4	—
GND	 A2, B1, B2, D10, D18, E6, E14, E22, F9, F12, F15, F18, F21, F24, G5, H6, J23, L4, L6, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, M16, M17, M18, M23, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, P24, R5, R23, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U6, U11, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V23, V25, W4, Y6, AA23, AB24, AC5, AC8, AC11, AC14, AC17, AC20, AD9, AD15, AD21, AE12, AE18, AF3, AF26 	_	_	
GV _{DD}	U9, V9, W10, W19, Y11, Y12, Y14, Y15, Y17, Y18, AA6, AB5, AC9, AC12, AC15, AC18, AC21, AC24, AD6, AD8, AD14, AD20, AE5, AE11, AE17, AG2, AG27	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}	
LV _{DD1}	U20, W25	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5V, 3.3V)	LV _{DD1}	_
LV _{DD2}	V20, Y23	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD2}	
V _{DD}	J11, J12, J15, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L18, L19, M10, M19, N10, N19, P9, P10, P19, R10, R19, R20, T10, T19, U10, U19, V10, V11, V18, V19, W11, W12, W13, W14, W15, W16, W17, W18	Power for core (1.2 V)	V _{DD}	_

Table 51. MPC8343EA (PBGA) Pinout Listing (continued)

RCWL[SPMF]	System PLL Multiplication Factor
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

Table 54. Sy	ystem PLL	Multiplication	Factors ((continued))
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As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 55 and Table 56 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

			Ir	put Clock Fre	quency (MHz) ²
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
				<i>csb_clk</i> Freq	uency (MHz)	
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			

Table 55. CSB Frequency Options for Host Mode



Thermal

that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W) $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 60 shows heat sink thermal resistance for PBGA of the MPC8343EA.

Table 60. Heat Sink and Thermal Resistance of MPC8343EA (PBGA)

Heat Sink Assuming Thermal Grease	Air Flow	29 $ imes$ 29 mm PBGA
neat Sink Assuming merinal Grease	AITTOW	Thermal Resistance
AAVID $30 \times 30 \times 9.4$ mm pin fin	Natural convection	13.5
AAVID $30 \times 30 \times 9.4$ mm pin fin	1 m/s	9.6
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	8.8
AAVID 31 \times 35 \times 23 mm pin fin	Natural convection	11.3
AAVID 31 \times 35 \times 23 mm pin fin	1 m/s	8.1
AAVID 31 \times 35 \times 23 mm pin fin	2 m/s	7.5
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	9.1
Wakefield, $53\times53\times25$ mm pin fin	1 m/s	7.1
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	6.5
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	10.1



Heat Sink Assuming Thermal Grease	Air Flow	29 $ imes$ 29 mm PBGA
Theat Onix Assuming Thermal Grease		Thermal Resistance
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	1 m/s	7.7
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	2 m/s	6.6
MEI, 75 \times 85 \times 12 mm, adjacent board, 40 mm side bypass	1 m/s	6.9

Table 60. Heat Sink and Thermal Resistance of MPC8343EA (PBGA) (continued)

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy	603-224-9988
80 Commercial St.	
Concord, NH 03301	
Internet: www.aavidthermalloy.com	
Alpha Novatech	408-567-8082
473 Sapena Ct. #12	
Santa Clara, CA 95054	
Internet: www.alphanovatech.com	
International Electronic Research Corporation (IERC)	818-842-7277
413 North Moss St.	
Burbank, CA 91502	
Internet: www.ctscorp.com	
Millennium Electronics (MEI)	408-436-8770
Loroco Sites	
671 East Brokaw Road	
San Jose, CA 95112	
Internet: www.mei-thermal.com	
Tyco Electronics	800-522-2800
Chip Coolers TM	
P.O. Box 3668	
Harrisburg, PA 17105-3668	
Internet: www.chipcoolers.com	
Wakefield Engineering	603-635-5102
33 Bridge St.	
Pelham, NH 03076	
Internet: www.wakefield.com	



Document Revision History

23 Document Revision History

This table provides a revision history of this document.

Table 64.	Document	Revision	History
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Rev. Number	Date	Substantive Change(s)
11	09/2011	 In Section 2.2, "Power Sequencing," added Section 2.2.1, "Power-Up Sequencing" and Figure 4. In Table 25, Table 29, and Table 27, removed the GTX_CLK125. In Table 30, updated t_{MDKHDX} Max value from 170ns to 70ns.
10	11/2010	 In Table 51, added overbar to LCS[4] and LCS[5] signals. In Table 51 added note for pin LGPL4. In Section 21.7, "Pull-Up Resistor Requirements, updated the list of open drain type pins.
9	05/2010	 In Table 25 through Table 26, changed V_{IL}(min) to V_{IH}(max) to (20%–80%). Added Table 8, "EC_GTX_CLK125 AC Timing Specifications."
8	5/2009	 In Section 18.1, "Package Parameters for the MPC8343EA PBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. In Table 53, added two columns for the DDR1 and DDR2 memory bus frequency. In Table 62, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.
7	2/2009	 Added footnote 6 to Table 7. In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. In Table 35, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 18, Figure 20, and Figure 21 for output signals. Added footnote 10 to Table 51. In Table 51, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net." In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the four AVDD pins." In Table 62, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266."
6	4/2007	 In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. In Section 21.7, "Pull-Up Resistor Requirements,"deleted last two paragraphs and after first paragraph, added a new paragraph. Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
5	3/2007	 Page 1, updated first paragraph to reflect PowerQUICC II Pro information. In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. In Figure 38, "JTAG Interface Connection," updated with new figure. In Figure 38, "JTAG Interface Connection," updated with new figure. In Section 23, "Ordering Information," replaced first paragraph and added a note. In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T _{ddkhds} for 333 MHz from 900 ps to 775 ps.