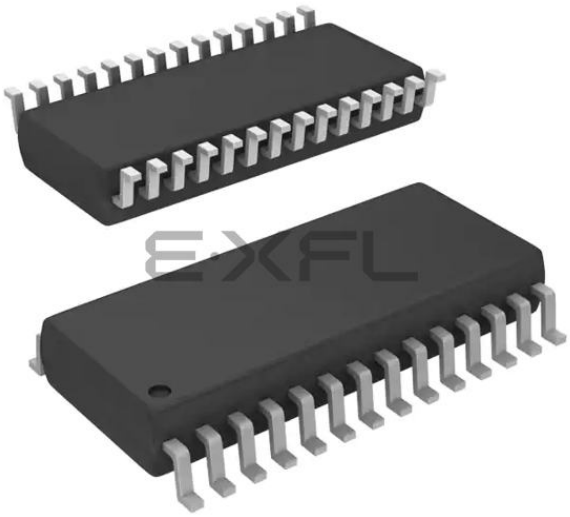

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21345-24sxit

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[2]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94[2]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A[2]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45[2]	up to 38	2	8	up to 38	0	4	6[3]	1 K	16 K
CY8C21x45[2]	up to 24	1	4	up to 24	0	4	6[3]	512	8 K
CY8C21x34[2]	up to 28	1	4	up to 28	0	2	4[3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[3]	256	4 K
CY8C20x34[2]	up to 28	0	0	up to 28	0	0	3[3,4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[3,4]	up to 2 K	up to 32 K

Getting Started

For in-depth information, along with detailed programming details, see the *CY8C22x45, CY8C21345: PSoC® Programmable System-on-Chip™ Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs. Use PSoC 1 Application note finder to search application notes or example projects for a specific application and/or family.

Development Kits

PSoC 1 kits are available online from Cypress and also available through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. The kit selector guide available in cypress website offers the list of all available development kits, programming and debugging kits for each PSoC 1 family.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Notes
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense® block.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

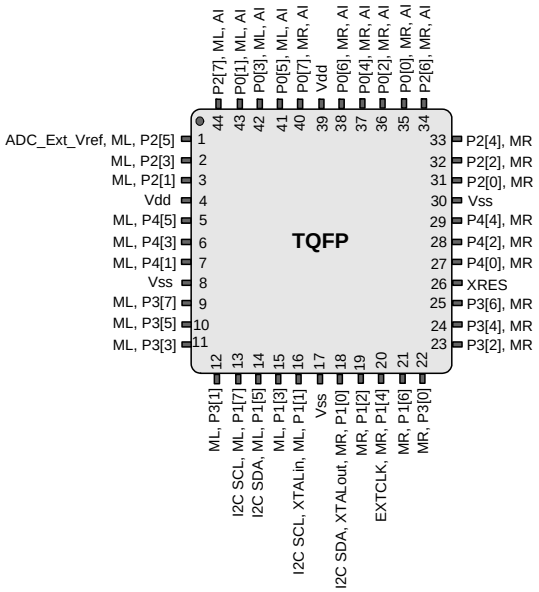
CY8C22545 44-pin TQFP

Table 3. Pin Definitions [7]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	ML	P2[5]	Optional ADC External Vref
2	I/O	ML	P2[3]	
3	I/O	ML	P2[1]	
4	Power		Vdd	Supply Voltage
5	I/O	ML	P4[5]	
6	I/O	ML	P4[3]	
7	I/O	ML	P4[1]	
8	Power		Vss	Ground Connection
9	I/O	ML	P3[7]	
10	I/O	ML	P3[5]	
11	I/O	ML	P3[3]	
12	I/O	ML	P3[1]	
13	I/O	ML	P1[7]	I2C serial clock (SCL)
14	I/O	ML	P1[5]	I2C serial data (SDA)
15	I/O	ML	P1[3]	
16	I/O	ML	P1[1]	Crystal (XTALin), I2C SCL, ISSP SCLK[6]
17	Power		Vss	Ground Connection
18	I/O	MR	P1[0]	Crystal (XTALout), I2C SDA, ISSP SDATA[6]
19	I/O	MR	P1[2]	
20	I/O	MR	P1[4]	Optional external clock input (EXTCLK)
21	I/O	MR	P1[6]	
22	I/O	MR	P3[0]	
23	I/O	MR	P3[2]	
24	I/O	MR	P3[4]	
25	I/O	MR	P3[6]	
26	Input		XRES	Active High Pin Reset with Internal Pull Down
27	I/O	MR	P4[0]	
28	I/O	MR	P4[2]	
29	I/O	MR	P4[4]	
30	Power		Vss	Ground Connection
31	I/O	MR	P2[0]	
32	I/O	MR	P2[2]	
33	I/O	MR	P2[4]	
34	I/O	I, MR	P2[6]	To Compare Column 1
35	I/O	I, MR	P0[0]	
36	I/O	I, MR	P0[2]	
37	I/O	I, MR	P0[4]	
38	I/O	I, MR	P0[6]	
39	Power		Vdd	Supply Voltage
40	I/O	I, MR	P0[7]	Integration Capacitor for MR
41	I/O	I, ML	P0[5]	Integration Capacitor for ML
42	I/O	I, ML	P0[3]	
43	I/O	I, ML	P0[1]	
44	I/O	I, ML	P2[7]	To Compare Column 0

LEGEND: A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input.

Figure 4. Pin Diagram



Note
7. All V_{SS} pins should be brought out to one common GND plane.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40	#	ASC10CR0*	80*	RW		C0	RW
PRT0IE	01	RW		41	W		81	RW		C1	RW
PRT0GS	02	RW		42	RW		82	RW		C2	RW
PRT0DM2	03	RW		43	#		83	RW		C3	RW
PRT1DR	04	RW		44	#	ASD11CR0*	84*	RW		C4	RW
PRT1IE	05	RW		45	W		85	RW		C5	RW
PRT1GS	06	RW		46	RW		86	RW		C6	RW
PRT1DM2	07	RW		47	#		87	RW		C7	RW
PRT2DR	08	RW		48	#		88	RW	PWMVREF0	C8	#
PRT2IE	09	RW		49	W		89	RW	PWMVREF1	C9	#
PRT2GS	0A	RW		4A	RW		8A	RW	IDAC_MODE	CA	RW
PRT2DM2	0B	RW		4B	#		8B	RW	PWM_SRC	CB	#
PRT3DR	0C	RW		4C	#		8C	RW	TS_CR0	CC	RW
PRT3IE	0D	RW		4D	W		8D	RW	TS_CMPH	CD	RW
PRT3GS	0E	RW		4E	RW		8E	RW	TS_CMPL	CE	RW
PRT3DM2	0F	RW		4F	#		8F	RW	TS_CR1	CF	RW
PRT4DR	10	RW	CSD0_DR0_L	50	R		90	RW	CUR PP	D0	RW
PRT4IE	11	RW	CSD0_DR1_L	51	W		91	RW	STK_PP	D1	RW
PRT4GS	12	RW	CSD0_CNT_L	52	R		92	RW	PRV PP	D2	RW
PRT4DM2	13	RW	CSD0_CR0	53	#		93	RW	IDX_PP	D3	RW
	14	RW	CSD0_DR0_H	54	R		94	RW	MVR_PP	D4	RW
	15	RW	CSD0_DR1_H	55	W		95	RW	MVW_PP	D5	RW
	16	RW	CSD0_CNT_H	56	R		96	RW	I2C0_CFG	D6	RW
	17	RW	CSD0_CR1	57	RW		97	RW	I2C0_SCR	D7	#
	18	RW	CSD1_DR0_L	58	R		98	RW	I2C0_DR	D8	RW
	19	RW	CSD1_DR1_L	59	W		99	RW	I2C0_MSCR	D9	#
	1A	RW	CSD1_CNT_L	5A	R		9A	RW	INT_CLR0	DA	RW
	1B	RW	CSD1_CR0	5B	#		9B	RW	INT_CLR1	DB	RW
	1C	RW	CSD1_DR0_H	5C	R		9C	RW	INT_CLR2	DC	RW
	1D	RW	CSD1_DR1_H	5D	W		9D	RW	INT_CLR3	DD	RW
	1E	RW	CSD1_CNT_H	5E	R		9E	RW	INT_MSK3	DE	RW
	1F	RW	CSD_CR1	5F	RW		9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW		A1		INT_MSK1	E1	RW
DBC00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RW
DBC01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RW
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0*	E6	RW
DBC01CR0	27	#		67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#	ADC0_CR	68	#		A8	W	MUL0_X	E8	W
DCC02DR1	29	W	ADC1_CR	69	#		A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW		AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW		AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW		AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW		AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW		AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW		AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70	RW	RDI0RI	B0	RW	CPU A	F0	#
DBC10DR1	31	W		71	RW	RDI0SYN	B1	RW	CPU_T1	F1	#
DBC10DR2	32	RW	ACB00CR1*	72*	RW	RDI0IS	B2	RW	CPU_T2	F2	#
DBC10CR0	33	#	ACB00CR2*	73*	RW	RDI0LT0	B3	RW	CPU_X	F3	#
DBC11DR0	34	#		74	RW	RDI0LT1	B4	RW	CPU PCL	F4	#
DBC11DR1	35	W		75	RW	RDI0RO0	B5	RW	CPU_PCH	F5	#
DBC11DR2	36	RW	ACB01CR1*	76*	RW	RDI0RO1	B6	RW	CPU_SP	F6	#
DBC11CR0	37	#	ACB01CR2*	77*	RW	RDI0DSM	B7	RW	CPU_F	F7	I
DCC12DR0	38	#		78	RW	RDI1RI	B8	RW	CPU_TST0	F8	RW
DCC12DR1	39	W		79	RW	RDI1SYN	B9	RW	CPU_TST1	F9	RW
DCC12DR2	3A	RW		7A	RW	RDI1IS	BA	RW	CPU_TST2	FA	RW
DCC12CR0	3B	#		7B	RW	RDI1LT0	BB	RW	CPU TST3	FB	#
DCC13DR0	3C	#		7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Shaded fields are Reserved and must not be accessed. **# Access is bit specific. * has a different meaning.**

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduce data retention time
$T_{BAKETEMP}$	Bake temperature	–	125	See Package label	°C	
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
Vdd	Supply voltage on Vdd relative to Vss	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOz}	DC voltage applied to tristate	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electr static discharge voltage	2000	–	–	V	Human Body Model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 30 on page 28. The user must limit the power consumption to comply with this requirement.

DC GPIO Specifications

Table 10 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only, unless otherwise specified.

Table 10. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD} [9]	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	Vdd – 1.0	–	–	V	I_{OH} = 10 mA, Vdd = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, Vdd = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = Vdd – 1.0 V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL} [9]	Input Low level	–	–	0.8	V	Vdd = 3.0 to 5.25
V_{IH} [9]	Input High level	2.1	–		V	Vdd = 3.0 to 5.25
V_H [9]	Input hysterisis	–	60	–	mV	
I_{IL} [9]	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C_{IN} [9]	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C

Note
9. The DC GPIO specifications apply to the XRES pin as well.

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 20. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Min(%)	Typ	Max	Max(%)	Units	Notes
F_{IMO24} [15]	Internal Main Oscillator Frequency for 24 MHz	22.8	–	24	25.2 [16, 17, 18]	–	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 13. SLIMO mode = 0 < 85.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	8	6	6.5 [16, 17, 18]	8	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 13. SLIMO mode = 0 < 85.
F_{CPU1}	CPU Frequency (5 V Nominal)	0.089	–	24	24.6 [16, 17]	–	MHz	24 MHz only for SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3 V Nominal)	0.089	–	12	12.3 [17, 18]	–	MHz	SLIMO mode = 0.
F_{BLK5}	Digital PSoC Block Frequency (5 V Nominal)	0	–	48	49.2 [16, 17, 19]	–	MHz	Refer to Table 24 on page 23.
F_{BLK33}	Digital PSoC Block Frequency (3.3 V Nominal)	0	–	24	24.6 [17, 19]	–	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	–	32	85	–	kHz	
F_{32KU}	Untrimmed Internal Low Speed Oscillator Frequency	5	–	–	100	–	kHz	The ILO is not adjusted with the factory trim values until after the CPU starts running. See the “System Resets” section in the Technical Reference Manual.
T_{XRES}	External Reset Pulse Width	10	–	–	–	–	µs	This specification refers to the minimum pulse width required to achieve complete device Reset. Shorter pulse widths may cause undefined chip behavior.
DC24M	24 MHz Duty Cycle	40	–	50	60	–	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	–	50	80	–	%	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	–	12.3	–	MHz	
$SR_{POWERUP}$	Power supply slew rate	–	–	–	250	–	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	–	–	100	–	ms	
tjit_IMO[20]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	–	200	700	–	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	–	300	900	–	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	–	100	400	–	ps	
tjit_PLL [20]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	–	200	800	–	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	–	300	1200	–	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	–	100	700	–	ps	

Notes

15. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see “Errata” on page 35.
16. Valid only for 4.75 V < Vdd < 5.25 V.
17. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
18. 3.0 V < Vdd < 3.6 V.
19. Refer to the individual user module data sheets for information on maximum frequencies for user modules.
20. Refer to Cypress Jitter Specifications, Understanding Datasheet Jitter Specifications for Cypress Timing Products for more information.

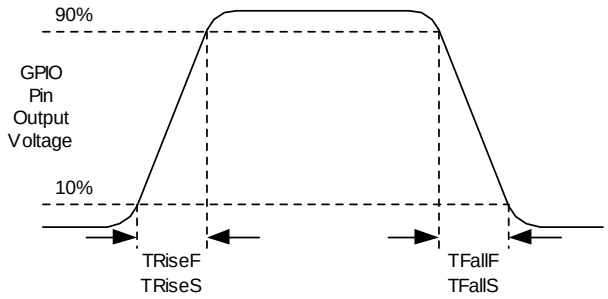
AC GPIO Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 21. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25 V, 10% to 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25 V, 10% to 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	7	27	–	ns	Vdd = 3 to 5.25 V, 10% to 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	7	22	–	ns	Vdd = 3 to 5.25 V, 10% to 90%

Figure 6. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 22. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Mode Response Time, 50 mV			100	ns	Vdd ≥ 3.0 V

AC Low Power Comparator Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 23. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V, at 25 °C and are for design guidance only.

Table 24. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block Input Clock Frequency					
	Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
Timer	Input Clock Frequency					
	No Capture, Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	No Capture, Vdd < 4.75 V	–	–	25.2[21]	MHz	
	With Capture	–	–	25.2[21]	MHz	
	Capture Pulse Width	50[22]	–	–	ns	
Counter	Input Clock Frequency					
	No Enable Input, Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	No Enable Input, Vdd < 4.75 V	–	–	25.2[21]	MHz	
	With Enable Input	–	–	25.2[21]	MHz	
	Enable Input Pulse Width	50[22]	–	–	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[22]	–	–	ns	
	Disable Mode	50[22]	–	–	ns	
	Input Clock Frequency					
	Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
CRCPRS (PRS Mode)	Input Clock Frequency					
	Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	–	–	25.2[21]	MHz	
SPIM	Input Clock Frequency	–	–	8.4[21]	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.2[21]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50[22]	–	–	ns	
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	Vdd ≥ 4.75 V, 2 Stop Bits	–	–	50.4[21]	MHz	
	Vdd ≥ 4.75 V, 1 Stop Bit	–	–	25.2[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	Vdd ≥ 4.75 V, 2 Stop Bits	–	–	50.4[21]	MHz	
	Vdd ≥ 4.75 V, 1 Stop Bit	–	–	25.2[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	

Notes
21. Accuracy derived from IMO with appropriate trim for V_{DD} range.
22. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Programming Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, or 3.3 V at 25 °C and are for design guidance only.

Table 28. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
F_{SCLK3}	Frequency of SCLK3	0	–	6	MHz	V_{DD} < 3.6 V
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	40	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	3.6 < Vdd; at 30 pF Load
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	65	ns	3.0 ≤ Vdd ≤ 3.6; at 30 pF Load
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ns	
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100	ms	
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200	ms	

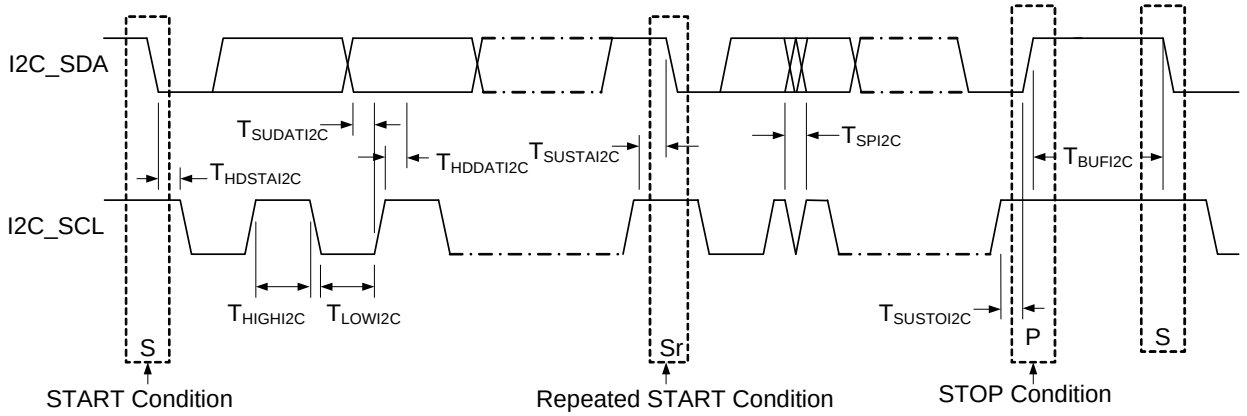
AC I²C Specifications

Table 29 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, and 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 29. AC Characteristics of the I²C SDA and SCL Pins for Vdd ≥ 3.0 V

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[23]	–	ns	
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the Input Filter	–	–	0	50	ns	

Figure 7. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

23. A Fast-Mode I2C-bus device may be used in a Standard-Mode I2C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Thermal Impedances

Table 30. Thermal Impedances per Package

Package	Typical θ_{JA} [25]
28-pin SOIC	68 °C/W
44-pin TQFP	61 °C/W

Solder Reflow Specifications

Table 31 shows the solder reflow temperature limits that must not be exceeded.

Table 31. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds

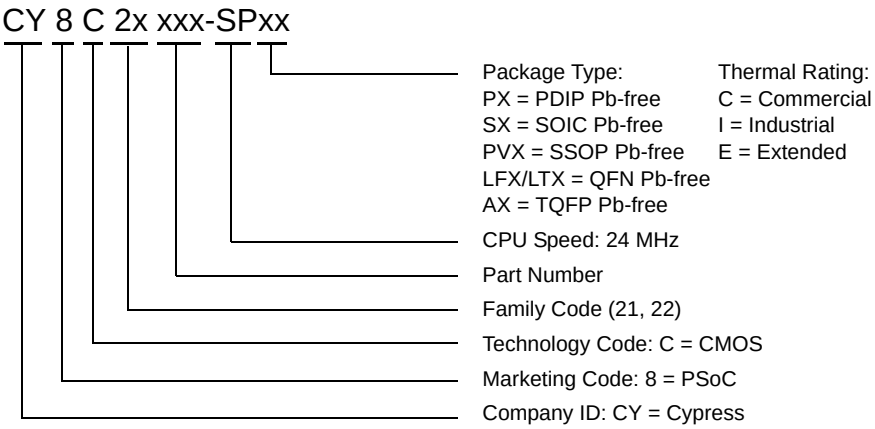
Ordering Information

The following table lists the key package features and ordering codes of this PSoC device family.

Table 32. PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin SOIC	CY8C21345-24SXI	8	512B	–40 °C to +85 °C	4	6	24	24[24]	0	Y
28-pin SOIC (Tape and Reel)	CY8C21345-24SXIT	8	512B	–40 °C to +85 °C	4	6	24	24[24]	0	Y
28-pin SOIC	CY8C22345-24SXI	16	1K	–40 °C to +85 °C	8	6	24	24[24]	0	Y
28-pin SOIC (Tape and Reel)	CY8C22345-24SXIT	16	1K	–40 °C to +85 °C	8	6	24	24[24]	0	Y
44-pin TQFP	CY8C22545-24AXI	16	1K	–40 °C to +85 °C	8	6	38	38[24]	0	Y
44-pin TQFP (Tape and Reel)	CY8C22545-24AXIT	16	1K	–40 °C to +85 °C	8	6	38	38[24]	0	Y

Ordering Code Definitions



Note
24. Ten direct inputs.
25. $T_J = T_A + POWER \times \theta_{JA}$

Acronyms

Table 33 lists the acronyms that are used in this document.

Table 33. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MAC	multiply-accumulate
ADC	analog-to-digital converter	MCU	microcontroller unit
API	application programming interface	MIPS	million instructions per second
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CSD	CapSense sigma delta	POR	power on reset
CT	continuous time	PPOR	precision power on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DNL	differential nonlinearity	PWM	pulse width modulator
ECO	external crystal oscillator	QFN	quad flat no leads
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
FSK	frequency-shift keying	SAR	successive approximation
GPIO	general-purpose I/O	SC	switched capacitor
I/O	input/output	SLIMO	slow IMO
ICE	in-circuit emulator	SOIC	small-outline integrated circuit
IDE	integrated development environment	SPI™	serial peripheral interface
IDAC	current DAC	SRAM	static random access memory
ILO	internal low speed oscillator	SROM	supervisory read only memory
IMO	internal main oscillator	SSOP	shrink small-outline package
INL	integral nonlinearity	TQFP	thin quad flat pack
IrDA	infrared data association	UART	universal asynchronous receiver / transmitter
ISSP	in-system serial programming	USB	universal serial bus
LPC	low power comparator	WDT	watchdog timer
LSB	least-significant bit	XRES	external reset
LVD	low voltage detect		

Reference Documents

CY8C22x45 and CY8C21345 PSoC® Programmable System-on-Chip™ *Technical Reference Manual (TRM)* (001-48461)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses Vdd and provides an interrupt to the system when Vdd falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand.
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ Problem Definition

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ Parameters Affected

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ Trigger Condiiton(S)

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

■ Workaround

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ Fix Status

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.

Document History Page (continued)

Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip Document Number: 001-43084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*M	3231771	BOBH / ECU	04/18/11	Updated analog inputs column in Table 32 on page 28 and included reference to Note 24. Updated the following sections: Getting Started, Development Tools, and Designing with PSoC Designer as all the System level designs have been de-emphasized. Updated Table 31, “Solder Reflow Specifications,” on page 28. Updated package diagrams: 51-85026 to *F 51-85064 to *E
*N	3578757	PMAD	04/11/2012	Removed reference to AN2012 as the document is in obsolete status. Updated template. No technical updates. Completing sunset review.
*O	3598230	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*P	3915358	SAMP	02/27/2013	Updated Electrical Specifications (Updated DC Electrical Characteristics (Updated DC GPIO Specifications (Updated Table 10 (Updated Notes for V_{OH} and V_{OL} parameters)))).
*Q	3959550	SAMP	04/09/2013	Added Errata.
*R	4081559	PMAD	07/30/2013	Added Errata footnotes (Note 1, 11, 15). Updated Features: Added Note 1 and referred the same note in ±5% under “Precision, programmable clocking”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated SAR10 ADC DC Specifications: Added Note 11 and referred the same note in SPS parameter. Updated AC Electrical Characteristics: Updated AC Chip Level Specifications: Added Note 15 and referred the same note in F_{IMO24} parameter. Updated Packaging Information: spec 51-85026 – Changed revision from *F to *G. Updated Errata. Updated in new template.
*S	4416752	RAHU	06/26/2014	Updated Pinouts: Updated CY8C22345, CY8C21345 28-pin SOIC: Updated Note 6. Updated CY8C22545 44-pin TQFP: Updated Table 3: Replaced “TC” with “ISSP” in description of pin 16 and pin 18. Updated Packaging Information: spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F.

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