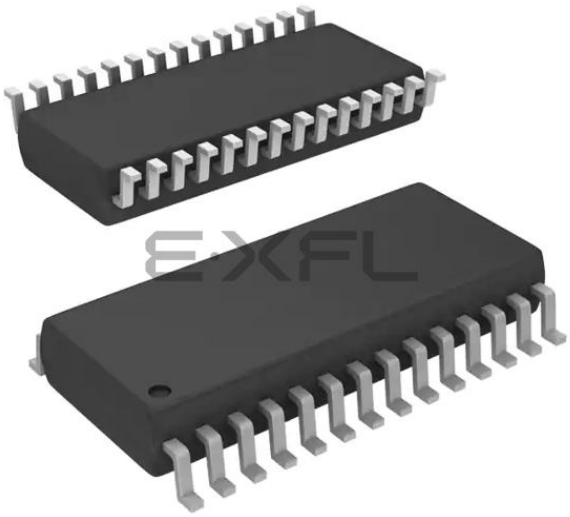

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c22345-24sxi

Contents

PSoC Functional Overview

The PSoC family consists of many On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with one low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in Figure 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows the combining of all the device resources into a complete custom system. The PSoC family can have up to five I/O ports connecting to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general-purpose I/O (GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 21 vectors, to simplify the programming of real time embedded events.

Program execution is timed and protected using the included Sleep and watchdog timers (WDT).

Memory encompasses 16 KB of Flash for program storage, 1 K bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

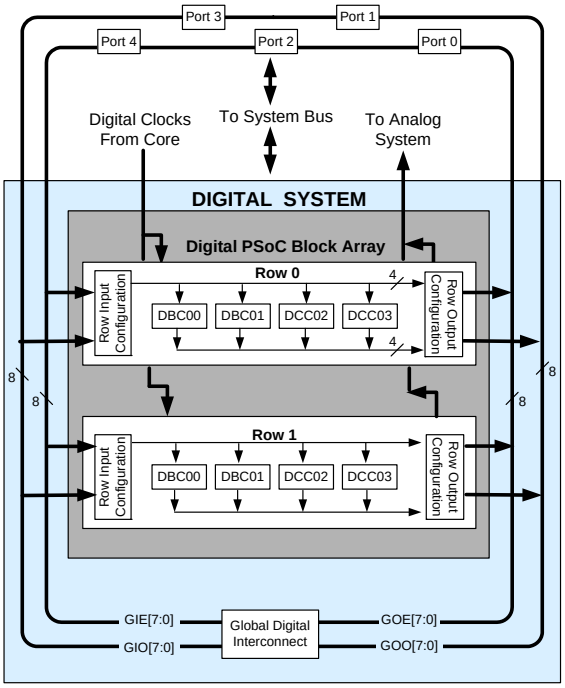
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator). The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the Sleep timer and WDT. If crystal accuracy is required, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC), and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin can also generate a system interrupt on high level, low level, and change from last read.

Digital System

The Digital System is composed of eight digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations are:

- PWMs (8- and 16-Bit)
- PWMs with Dead band (8- and 16-Bit)
- Counters (8 to 32-Bit)
- Timers (8 to 32-Bit)
- UART 8 Bit with Selectable Parity (Up to Two)
- SPI Master and Slave (Up to Two)
- Shift Register (1 to 32-Bit)
- I2C Slave and Master (One Available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32-Bit)
- IrDA (Up to Two)
- Pseudo Random Sequence Generators (8 to 32-Bit)

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in Table 1 on page 5.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[2]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94[2]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A[2]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45[2]	up to 38	2	8	up to 38	0	4	6[3]	1 K	16 K
CY8C21x45[2]	up to 24	1	4	up to 24	0	4	6[3]	512	8 K
CY8C21x34[2]	up to 28	1	4	up to 28	0	2	4[3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[3]	256	4 K
CY8C20x34[2]	up to 28	0	0	up to 28	0	0	3[3,4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[3,4]	up to 2 K	up to 32 K

Getting Started

For in-depth information, along with detailed programming details, see the *CY8C22x45, CY8C21345: PSoC® Programmable System-on-Chip™ Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs. Use PSoC 1 Application note finder to search application notes or example projects for a specific application and/or family.

Development Kits

PSoC 1 kits are available online from Cypress and also available through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. The kit selector guide available in cypress website offers the list of all available development kits, programming and debugging kits for each PSoC 1 family.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Notes
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense® block.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

Pinouts

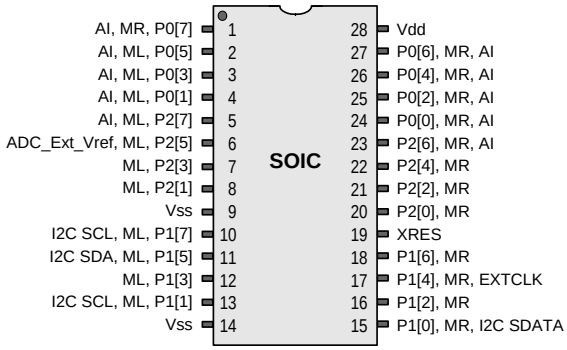
This PSoC device family is available in a variety of packages that are listed in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

CY8C22345, CY8C21345 28-pin SOIC

Table 2. Pin Definitions

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Integration Capacitor for MR
2	I/O	I, ML	P0[5]	Integration Capacitor for ML
3	I/O	I, ML	P0[3]	
4	I/O	I, ML	P0[1]	
5	I/O	I, ML	P2[7]	To Compare Column 0
6	I/O	ML	P2[5]	Optional ADC External Vref
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		Vss	Ground Connection [5]
10	I/O	ML	P1[7]	I2C serial clock (SCL)
11	I/O	ML	P1[5]	I2C serial data (SDA)
12	I/O	ML	P1[3]	
13	I/O	ML	P1[1]	I2C serial clock (SCL), ISSP-SCLK [6]
14	Power		Vss	Ground Connection [5]
15	I/O	MR	P1[0]	I2C serial Clock (SCL), ISSP-SDATA [6]
16	I/O	MR	P1[2]	
17	I/O	MR	P1[4]	Optional external clock input (EXT-CLK)
18	I/O	MR	P1[6]	
19	Input		XRES	Active High Pin Reset with Internal Pull Down
20	I/O	MR	P2[0]	
21	I/O	MR	P2[2]	
22	I/O	MR	P2[4]	
23	I/O	I, MR	P2[6]	To Compare Column 1
24	I/O	I, MR	P0[0]	
25	I/O	I, MR	P0[2]	
26	I/O	I, MR	P0[4]	
27	I/O	I, MR	P0[6]	
28	Power		Vdd	Supply Voltage

Figure 3. Pin Diagram



LEGEND: A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input.

Notes
5. All V_{SS} pins should be brought out to one common GND plane.
6. If ISSP is not used, pins P1[0] and P1[1] will respond differently to a POR or XRES event. After a POR or XRES event, both pins are pulled down to ground by going into the resistive zero Drive mode, before reaching the High Z Drive mode.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40	#	ASC10CR0*	80*	RW		C0	RW
PRT0IE	01	RW		41	W		81	RW		C1	RW
PRT0GS	02	RW		42	RW		82	RW		C2	RW
PRT0DM2	03	RW		43	#		83	RW		C3	RW
PRT1DR	04	RW		44	#	ASD11CR0*	84*	RW		C4	RW
PRT1IE	05	RW		45	W		85	RW		C5	RW
PRT1GS	06	RW		46	RW		86	RW		C6	RW
PRT1DM2	07	RW		47	#		87	RW		C7	RW
PRT2DR	08	RW		48	#		88	RW	PWMVREF0	C8	#
PRT2IE	09	RW		49	W		89	RW	PWMVREF1	C9	#
PRT2GS	0A	RW		4A	RW		8A	RW	IDAC_MODE	CA	RW
PRT2DM2	0B	RW		4B	#		8B	RW	PWM_SRC	CB	#
PRT3DR	0C	RW		4C	#		8C	RW	TS_CR0	CC	RW
PRT3IE	0D	RW		4D	W		8D	RW	TS_CMPH	CD	RW
PRT3GS	0E	RW		4E	RW		8E	RW	TS_CMPL	CE	RW
PRT3DM2	0F	RW		4F	#		8F	RW	TS_CR1	CF	RW
PRT4DR	10	RW	CSD0_DR0_L	50	R		90	RW	CUR PP	D0	RW
PRT4IE	11	RW	CSD0_DR1_L	51	W		91	RW	STK_PP	D1	RW
PRT4GS	12	RW	CSD0_CNT_L	52	R		92	RW	PRV PP	D2	RW
PRT4DM2	13	RW	CSD0_CR0	53	#		93	RW	IDX_PP	D3	RW
	14	RW	CSD0_DR0_H	54	R		94	RW	MVR_PP	D4	RW
	15	RW	CSD0_DR1_H	55	W		95	RW	MVW_PP	D5	RW
	16	RW	CSD0_CNT_H	56	R		96	RW	I2C0_CFG	D6	RW
	17	RW	CSD0_CR1	57	RW		97	RW	I2C0_SCR	D7	#
	18	RW	CSD1_DR0_L	58	R		98	RW	I2C0_DR	D8	RW
	19	RW	CSD1_DR1_L	59	W		99	RW	I2C0_MSCR	D9	#
	1A	RW	CSD1_CNT_L	5A	R		9A	RW	INT_CLR0	DA	RW
	1B	RW	CSD1_CR0	5B	#		9B	RW	INT_CLR1	DB	RW
	1C	RW	CSD1_DR0_H	5C	R		9C	RW	INT_CLR2	DC	RW
	1D	RW	CSD1_DR1_H	5D	W		9D	RW	INT_CLR3	DD	RW
	1E	RW	CSD1_CNT_H	5E	R		9E	RW	INT_MSK3	DE	RW
	1F	RW	CSD_CR1	5F	RW		9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW		A1		INT_MSK1	E1	RW
DBC00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RW
DBC01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RW
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0*	E6	RW
DBC01CR0	27	#		67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#	ADC0_CR	68	#		A8	W	MUL0_X	E8	W
DCC02DR1	29	W	ADC1_CR	69	#		A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW		AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW		AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW		AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW		AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW		AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW		AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70	RW	RDI0RI	B0	RW	CPU A	F0	#
DBC10DR1	31	W		71	RW	RDI0SYN	B1	RW	CPU_T1	F1	#
DBC10DR2	32	RW	ACB00CR1*	72*	RW	RDI0IS	B2	RW	CPU_T2	F2	#
DBC10CR0	33	#	ACB00CR2*	73*	RW	RDI0LT0	B3	RW	CPU_X	F3	#
DBC11DR0	34	#		74	RW	RDI0LT1	B4	RW	CPU PCL	F4	#
DBC11DR1	35	W		75	RW	RDI0RO0	B5	RW	CPU_PCH	F5	#
DBC11DR2	36	RW	ACB01CR1*	76*	RW	RDI0RO1	B6	RW	CPU_SP	F6	#
DBC11CR0	37	#	ACB01CR2*	77*	RW	RDI0DSM	B7	RW	CPU_F	F7	I
DCC12DR0	38	#		78	RW	RDI1RI	B8	RW	CPU_TST0	F8	RW
DCC12DR1	39	W		79	RW	RDI1SYN	B9	RW	CPU_TST1	F9	RW
DCC12DR2	3A	RW		7A	RW	RDI1IS	BA	RW	CPU_TST2	FA	RW
DCC12CR0	3B	#		7B	RW	RDI1LT0	BB	RW	CPU TST3	FB	#
DCC13DR0	3C	#		7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Shaded fields are Reserved and must not be accessed. **# Access is bit specific. * has a different meaning.**

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	0	RW		40	RW	ASC10CR0*	80*	RW		C0	RW
PRT0DM1	1	RW		41	RW		81	RW		C1	RW
PRT0IC0	2	RW		42	RW		82	RW		C2	RW
PRT0IC1	3	RW		43			83	RW		C3	RW
PRT1DM0	4	RW		44	RW	ASD11CR0*	84*	RW		C4	RW
PRT1DM1	5	RW		45	RW		85	RW		C5	RW
PRT1IC0	6	RW		46	RW		86	RW		C6	RW
PRT1IC1	7	RW		47			87	RW		C7	RW
PRT2DM0	8	RW		48	RW		88	RW		C8	#
PRT2DM1	9	RW		49	RW		89	RW		C9	RW
PRT2IC0	0A	RW		4A	RW		8A	RW		CA	RW
PRT2IC1	0B	RW		4B			8B	RW		CB	RW
PRT3DM0	0C	RW		4C	RW		8C	RW		CC	#
PRT3DM1	0D	RW		4D	RW		8D	RW		CD	RW
PRT3IC0	0E	RW		4E	RW		8E	RW		CE	RW
PRT3IC1	0F	RW		4F			8F	RW		CF	RW
PRT4DM0	10	RW	CMP0CR1	50	RW		90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52	RW		92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93	RW	GDI_E_OU	D3	RW
	14	RW	CMP1CR1	54	RW		94	RW		D4	RW
	15	RW	CMP1CR2	55	RW		95	RW		D5	RW
	16	RW		56	RW		96	RW		D6	RW
	17	RW	VDAC51CR0	57	RW		97	RW		D7	RW
	18	RW	CSCMPCR0	58	#		98	RW	MUX_CR0	D8	RW
	19	RW	CSCMPGOEN	59	RW		99	RW	MUX_CR1	D9	RW
	1A	RW	CSLUTCR0	5A	RW		9A	RW	MUX_CR2	DA	RW
	1B	RW	CMPCOLMUX	5B	RW		9B	RW	MUX_CR3	DB	RW
	1C	RW	CMPPWMCR	5C	RW		9C	RW	DAC_CR1#	DC	RW
	1D	RW	CMPFLTCR	5D	RW		9D	RW	OSC_GO_EN	DD	RW
	1E	RW	CMPCLK1	5E	RW		9E	RW	OSC_CR4	DE	RW
	1F	RW	CMPCLK0	5F	RW		9F	RW	OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR*	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR*	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW		6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE	RW	MUX_CR6	EE	RW
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF	RW	MUX_CR7	EF	RW
DBC10FN	30	RW		70	RW	RDI0RI	B0	RW	CPU_A	F0	#
DBC10IN	31	RW		71	RW	RDI0SYN	B1	RW	CPU_T1	F1	#
DBC10OU	32	RW	ACB00CR1*	72	RW	RDI0IS	B2	RW	CPU_T2	F2	#
DBC10CR1	33	RW	ACB00CR2*	73	RW	RDI0LT0	B3	RW	CPU_X	F3	#
DBC11FN	34	RW		74	RW	RDI0LT1	B4	RW	CPU_PCL	F4	#
DBC11IN	35	RW		75	RW	RDI0RO0	B5	RW	CPU_PCH	F5	#
DBC11OU	36	RW	ACB01CR1*	76*	RW	RDI0RO1	B6	RW	CPU_SP	F6	#
DBC11CR1	37	RW	ACB01CR2*	77*	RW	RDI0DSM	B7	RW	CPU_F	F7	I
DCC12FN	38	RW		78	RW	RDI1RI	B8	RW	FLS_PR0	F8	RW
DCC12IN	39	RW		79	RW	RDI1SYN	B9	RW	FLS_TR	F9	W
DCC12OU	3A	RW		7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C	RW	RDI1LT1	BC	RW	FAC_CR0	FC	SW
DCC13IN	3D	RW		7D	RW	RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Shaded fields are Reserved and must not be accessed. **# Access is bit specific. * has a different meaning.**

DC Programming Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply Current during Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage during Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage during Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] during Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] during Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage during Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage during Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)[13]	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[12]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

DC I^2C Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 19. DC I^2C Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}[14]	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}[14]	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Note
12. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
13. The 50,000 cycle Flash endurance per block is guaranteed only if the Flash operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V
14. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections.The I^2C GPIO pins also meet the above specs.

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 20. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Min(%)	Typ	Max	Max(%)	Units	Notes
F_{IMO24} [15]	Internal Main Oscillator Frequency for 24 MHz	22.8	–	24	25.2 [16, 17, 18]	–	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 13. SLIMO mode = 0 < 85.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	8	6	6.5 [16, 17, 18]	8	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 13. SLIMO mode = 0 < 85.
F_{CPU1}	CPU Frequency (5 V Nominal)	0.089	–	24	24.6 [16, 17]	–	MHz	24 MHz only for SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3 V Nominal)	0.089	–	12	12.3 [17, 18]	–	MHz	SLIMO mode = 0.
F_{BLK5}	Digital PSoC Block Frequency (5 V Nominal)	0	–	48	49.2 [16, 17, 19]	–	MHz	Refer to Table 24 on page 23.
F_{BLK33}	Digital PSoC Block Frequency (3.3 V Nominal)	0	–	24	24.6 [17, 19]	–	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	–	32	85	–	kHz	
F_{32KU}	Untrimmed Internal Low Speed Oscillator Frequency	5	–	–	100	–	kHz	The ILO is not adjusted with the factory trim values until after the CPU starts running. See the “System Resets” section in the Technical Reference Manual.
T_{XRES}	External Reset Pulse Width	10	–	–	–	–	µs	This specification refers to the minimum pulse width required to achieve complete device Reset. Shorter pulse widths may cause undefined chip behavior.
DC24M	24 MHz Duty Cycle	40	–	50	60	–	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	–	50	80	–	%	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	–	12.3	–	MHz	
$SR_{POWERUP}$	Power supply slew rate	–	–	–	250	–	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	–	–	100	–	ms	
tjit_IMO[20]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	–	200	700	–	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	–	300	900	–	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	–	100	400	–	ps	
tjit_PLL [20]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	–	200	800	–	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	–	300	1200	–	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	–	100	700	–	ps	

Notes

15. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see “Errata” on page 35.
16. Valid only for 4.75 V < Vdd < 5.25 V.
17. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
18. 3.0 V < Vdd < 3.6 V.
19. Refer to the individual user module data sheets for information on maximum frequencies for user modules.
20. Refer to Cypress Jitter Specifications, Understanding Datasheet Jitter Specifications for Cypress Timing Products for more information.

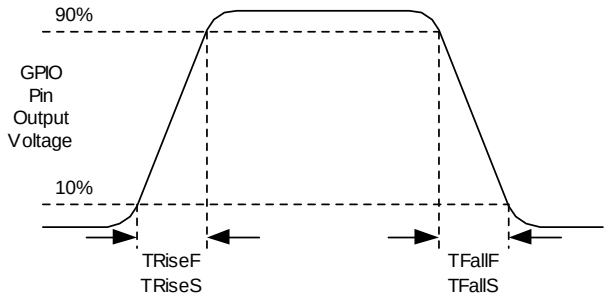
AC GPIO Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 21. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25 V, 10% to 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25 V, 10% to 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	7	27	–	ns	Vdd = 3 to 5.25 V, 10% to 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	7	22	–	ns	Vdd = 3 to 5.25 V, 10% to 90%

Figure 6. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 22. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Mode Response Time, 50 mV			100	ns	Vdd ≥ 3.0 V

AC Low Power Comparator Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 23. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 25. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 26. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

SAR10 ADC AC Specifications

Table 27 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. SAR10 ADC AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$Freq_3$	Input clock frequency 3 V	–	–	2.7	MHz	
$Freq_5$	Input clock frequency 5 V	–	–	2.7	MHz	

Thermal Impedances

Table 30. Thermal Impedances per Package

Package	Typical θ_{JA} [25]
28-pin SOIC	68 °C/W
44-pin TQFP	61 °C/W

Solder Reflow Specifications

Table 31 shows the solder reflow temperature limits that must not be exceeded.

Table 31. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds

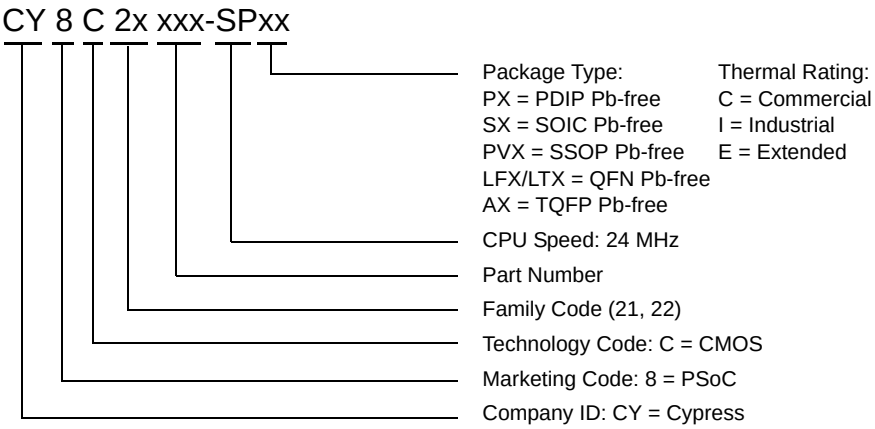
Ordering Information

The following table lists the key package features and ordering codes of this PSoC device family.

Table 32. PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin SOIC	CY8C21345-24SXI	8	512B	–40 °C to +85 °C	4	6	24	24[24]	0	Y
28-pin SOIC (Tape and Reel)	CY8C21345-24SXIT	8	512B	–40 °C to +85 °C	4	6	24	24[24]	0	Y
28-pin SOIC	CY8C22345-24SXI	16	1K	–40 °C to +85 °C	8	6	24	24[24]	0	Y
28-pin SOIC (Tape and Reel)	CY8C22345-24SXIT	16	1K	–40 °C to +85 °C	8	6	24	24[24]	0	Y
44-pin TQFP	CY8C22545-24AXI	16	1K	–40 °C to +85 °C	8	6	38	38[24]	0	Y
44-pin TQFP (Tape and Reel)	CY8C22545-24AXIT	16	1K	–40 °C to +85 °C	8	6	38	38[24]	0	Y

Ordering Code Definitions



Note
24. Ten direct inputs.
25. $T_J = T_A + POWER \times \theta_{JA}$

Acronyms

Table 33 lists the acronyms that are used in this document.

Table 33. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MAC	multiply-accumulate
ADC	analog-to-digital converter	MCU	microcontroller unit
API	application programming interface	MIPS	million instructions per second
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CSD	CapSense sigma delta	POR	power on reset
CT	continuous time	PPOR	precision power on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DNL	differential nonlinearity	PWM	pulse width modulator
ECO	external crystal oscillator	QFN	quad flat no leads
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
FSK	frequency-shift keying	SAR	successive approximation
GPIO	general-purpose I/O	SC	switched capacitor
I/O	input/output	SLIMO	slow IMO
ICE	in-circuit emulator	SOIC	small-outline integrated circuit
IDE	integrated development environment	SPI™	serial peripheral interface
IDAC	current DAC	SRAM	static random access memory
ILO	internal low speed oscillator	SROM	supervisory read only memory
IMO	internal main oscillator	SSOP	shrink small-outline package
INL	integral nonlinearity	TQFP	thin quad flat pack
IrDA	infrared data association	UART	universal asynchronous receiver / transmitter
ISSP	in-system serial programming	USB	universal serial bus
LPC	low power comparator	WDT	watchdog timer
LSB	least-significant bit	XRES	external reset
LVD	low voltage detect		

Reference Documents

CY8C22x45 and CY8C21345 PSoC® Programmable System-on-Chip™ *Technical Reference Manual (TRM)* (001-48461)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products

Document Conventions

Units of Measure

Table 34 lists the units of measures.

Table 34. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	mV	millivolts
°C	degree Celsius	nA	nanoampere
kHz	kilohertz	ns	nanosecond
kΩ	kilohm	W	ohm
LSB	least significant bit	%	percent
MHz	megahertz	pF	picofarad
µA	microampere	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolt	pA	pikoampere
mA	milliampere	V	volts
mm	millimeter	µW	microwatts
ms	millisecond	W	watt

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY8C21345	All Variants
CY8C22345	All Variants
CY8C22545	All Variants

CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

Errata Summary

The following table defines the errata applicable for this PSoC family device.

Items	Part Number	Silicon Revision	Fix Status
1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.
2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.

1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

■ Problem Definition

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

■ Parameters Affected

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

■ Trigger Condition(S)

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

■ Scope of Impact

Inaccurate output is possible.

■ Workaround

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- ❒ Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- ❒ Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

■ Fix Status

No silicon fix is planned.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ Problem Definition

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ Parameters Affected

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ Trigger Condiiton(S)

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

■ Workaround

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ Fix Status

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.

Document History Page

Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip Document Number: 001-43084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2251907	PMP / AESA	See ECN	New data sheet.
*A	2506377	EIJ / AESA	See ECN	Changed data sheet status to “Preliminary”. Changed part numbers to CY8C22x45. Updated data sheet template. Added 56-Pin OCD information. Added: “You must put filters on intended ADC input channels for anti-aliasing. This ensures that any out-of-band content is not folded into the Input Signal Band." To Section Analog System on page 4. Corrected Minimum Electro Static Discharge Voltage in Table 7 on page 14.
*B	2558750	PMP / AESA	08/28/2008	Updated Features on page 1, PSoC Core on page 3, Analog System on page 4. Changed DBB to DBC, and DCB to DCC in Register Tables Table 5 on page 11 and Table 6 on page 12. Removed INL at 8 bit reference in Table 15 on page 18. Changed IDD3 value Table 17 on page 19 Typ:3.3 mA, Max 6 mA Added “3.0 V < Vdd < 3.6 V and -40C < T_A < 85C, IMO can guarantee 5% accuracy only” to Table 20 on page 21. Updated data sheet template.
*C	2606793	NUQ / AESA	11/19/2008	Updated data sheet status to “Final”. Updated block diagram on page 1. Removed CY8C22045 56-Pin OCD information. Added part numbers CY8C21345, CY8C22345, and CY8C22545. For more details, see CDT 31271.
*D	2615697	PMP / AESA	12/03/2008	Confirmed CY8C22345 and CY8C21345 have same pinout on page 8. Confirmed that IMO has 5% accuracy in Table 20 on page 21.
*E	2631733	PMP / PYRS	01/07/2009	Updated Table 16. SAR10 ADC DC Specifications and Table 29 AC Programming Specifications. Title changed to “CY8C21345, CY8C22345, CY8C22545 PSoC® Programmable System-on-Chip™”
*F	2648800	JHU / AESA	01/28/2009	Updated INL, DNL information in Table 15 on page 18, Development Tools on page 6, and T_{DSCLK} parameter in Table 28 on page 25.
*G	2658078	HMI / AESA	02/11/2009	Updated section Features on page 1.
*H	2667311	JHU / AESA	03/16/2009	Added parameter “F_{32KU}” and added Min% and Max % to parameter “F_{IMO6}” in Table 20 on page 21, according to updated SLIMO spec.
*I	2748976	JZHU / PYRS	08/06/2009	Updated F_{32K1} max rating in Table 20 on page 21.
*J	2786560	JZHU	10/23/2009	Added DC_{ILO}, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, $T_{PROGRAM\_COLD}$, $SR_{POWERUP}$, I_{OH}, and I_{OL} parameters. Added Tape and Reel parts in Ordering Information table
*K	2901653	NJF	03/30/2010	Updated PSoC Designer Software Subsystems. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Modified Note 6 on page 17. Added F_{OUT48M} parameter in 5 V and 3.3 V AC Chip-Level Specifications. Removed AC Analog Mux Bus Specifications. Updated Ordering Code Definitions. Updated links in Sales, Solutions, and Legal Information.
*L	3114978	NJF	12/19/10	Added DC I^2C Specifications. Added Tjit_IMO specification, removed existing jitter specifications. Updated DC Programming Specifications. Updated AC Digital Block Specifications. Updated I^2C Timing Diagram. Added Solder Reflow Peak Temperature table. Updated Units of Measure, Acronyms, Glossary, and References sections.

Document History Page (continued)

Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip Document Number: 001-43084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*M	3231771	BOBH / ECU	04/18/11	Updated analog inputs column in Table 32 on page 28 and included reference to Note 24. Updated the following sections: Getting Started, Development Tools, and Designing with PSoC Designer as all the System level designs have been de-emphasized. Updated Table 31, “Solder Reflow Specifications,” on page 28. Updated package diagrams: 51-85026 to *F 51-85064 to *E
*N	3578757	PMAD	04/11/2012	Removed reference to AN2012 as the document is in obsolete status. Updated template. No technical updates. Completing sunset review.
*O	3598230	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*P	3915358	SAMP	02/27/2013	Updated Electrical Specifications (Updated DC Electrical Characteristics (Updated DC GPIO Specifications (Updated Table 10 (Updated Notes for V_{OH} and V_{OL} parameters)))).
*Q	3959550	SAMP	04/09/2013	Added Errata.
*R	4081559	PMAD	07/30/2013	Added Errata footnotes (Note 1, 11, 15). Updated Features: Added Note 1 and referred the same note in ±5% under “Precision, programmable clocking”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated SAR10 ADC DC Specifications: Added Note 11 and referred the same note in SPS parameter. Updated AC Electrical Characteristics: Updated AC Chip Level Specifications: Added Note 15 and referred the same note in F_{IMO24} parameter. Updated Packaging Information: spec 51-85026 – Changed revision from *F to *G. Updated Errata. Updated in new template.
*S	4416752	RAHU	06/26/2014	Updated Pinouts: Updated CY8C22345, CY8C21345 28-pin SOIC: Updated Note 6. Updated CY8C22545 44-pin TQFP: Updated Table 3: Replaced “TC” with “ISSP” in description of pin 16 and pin 18. Updated Packaging Information: spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F.

Document History Page (continued)

Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip Document Number: 001-43084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*T	4473295	MSUR	08/13/2014	Updated Getting Started: Updated description. Updated Application Notes: Updated description. Updated Development Kits: Updated description. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC GPIO Specifications: Updated Table 10: Added Note 9 and referred the same note in Table 10. Updated AC Electrical Characteristics: Updated AC Chip Level Specifications: Updated Table 20: Renamed T_{XRST} as T_{XRES} and added details in “Notes” column for the same parameter. Removed F_{OUT48M} parameter and its details.
*U	4515350	MSUR	09/26/2014	Updated Electrical Specifications: Updated DC Electrical Characteristics: Added DC IDAC Specifications. Updated DC GPIO Specifications: Updated Table 10: Removed reference of Note 9 from table caption. Referred Note 9 in R_{PD}, V_{IL}, V_{IH}, V_H, I_{IL}, C_{IN} parameters.
*V	4599794	DIMA	12/17/2014	Updated Pinouts: Updated CY8C22345, CY8C21345 28-pin SOIC: Updated Table 2: Added Note 5 and referred the same note in description of pin 9 and pin 14. Updated CY8C22545 44-pin TQFP: Updated Table 3: Added Note 7 and referred the same note in caption of Table 3.

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