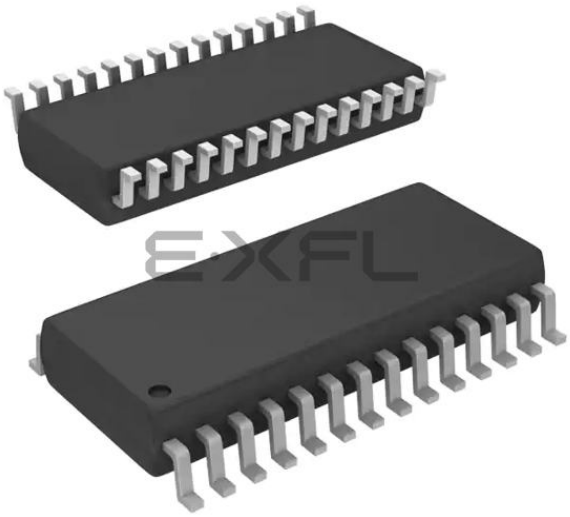

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c22345-24sxit

Contents

Analog System

The Analog System consists of a 10-bit SAR ADC and six configurable blocks.

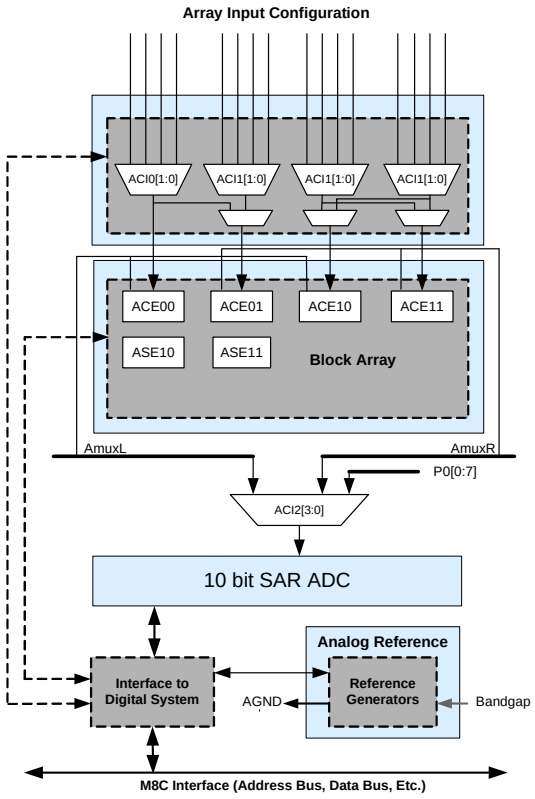
The programmable 10-bit SAR ADC is an optimized ADC that can be run up to 200 ksps with ± 1.5 LSB DNL and ± 2.5 LSB INL (true for $V_{DD} \geq 3.0$ V and Vref ≥ 3.0 V). External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-Digital converters (Single or Dual, with 8-bit resolution)
- Pin-to-pin Comparator
- Single ended comparators with absolute (1.3 V) reference or 5-bit DAC reference
- 1.3 V reference (as a System Resource)

Analog blocks are provided in columns of four, which include CT-E (Continuous Time) and SC-E (Switched Capacitor) blocks. These devices provide limited functionality Type “E” analog blocks.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Additional Digital resources and clocks optimized for CSD.
- Support “RTC” block into digital peripheral logic.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.

Pinouts

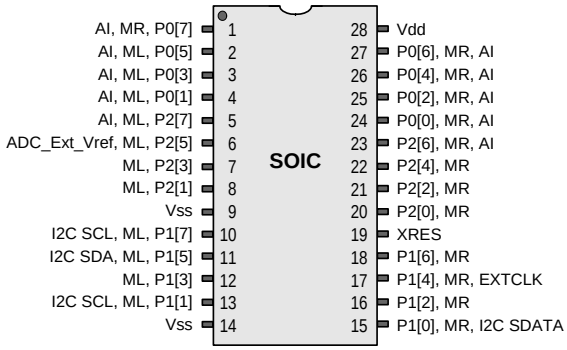
This PSoC device family is available in a variety of packages that are listed in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

CY8C22345, CY8C21345 28-pin SOIC

Table 2. Pin Definitions

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Integration Capacitor for MR
2	I/O	I, ML	P0[5]	Integration Capacitor for ML
3	I/O	I, ML	P0[3]	
4	I/O	I, ML	P0[1]	
5	I/O	I, ML	P2[7]	To Compare Column 0
6	I/O	ML	P2[5]	Optional ADC External Vref
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		Vss	Ground Connection [5]
10	I/O	ML	P1[7]	I2C serial clock (SCL)
11	I/O	ML	P1[5]	I2C serial data (SDA)
12	I/O	ML	P1[3]	
13	I/O	ML	P1[1]	I2C serial clock (SCL), ISSP-SCLK [6]
14	Power		Vss	Ground Connection [5]
15	I/O	MR	P1[0]	I2C serial Clock (SCL), ISSP-SDATA [6]
16	I/O	MR	P1[2]	
17	I/O	MR	P1[4]	Optional external clock input (EXT-CLK)
18	I/O	MR	P1[6]	
19	Input		XRES	Active High Pin Reset with Internal Pull Down
20	I/O	MR	P2[0]	
21	I/O	MR	P2[2]	
22	I/O	MR	P2[4]	
23	I/O	I, MR	P2[6]	To Compare Column 1
24	I/O	I, MR	P0[0]	
25	I/O	I, MR	P0[2]	
26	I/O	I, MR	P0[4]	
27	I/O	I, MR	P0[6]	
28	Power		Vdd	Supply Voltage

Figure 3. Pin Diagram



LEGEND: A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input.

Notes
5. All V_{SS} pins should be brought out to one common GND plane.
6. If ISSP is not used, pins P1[0] and P1[1] will respond differently to a POR or XRES event. After a POR or XRES event, both pins are pulled down to ground by going into the resistive zero Drive mode, before reaching the High Z Drive mode.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	0	RW		40	RW	ASC10CR0*	80*	RW		C0	RW
PRT0DM1	1	RW		41	RW		81	RW		C1	RW
PRT0IC0	2	RW		42	RW		82	RW		C2	RW
PRT0IC1	3	RW		43			83	RW		C3	RW
PRT1DM0	4	RW		44	RW	ASD11CR0*	84*	RW		C4	RW
PRT1DM1	5	RW		45	RW		85	RW		C5	RW
PRT1IC0	6	RW		46	RW		86	RW		C6	RW
PRT1IC1	7	RW		47			87	RW		C7	RW
PRT2DM0	8	RW		48	RW		88	RW		C8	#
PRT2DM1	9	RW		49	RW		89	RW		C9	RW
PRT2IC0	0A	RW		4A	RW		8A	RW		CA	RW
PRT2IC1	0B	RW		4B			8B	RW		CB	RW
PRT3DM0	0C	RW		4C	RW		8C	RW		CC	#
PRT3DM1	0D	RW		4D	RW		8D	RW		CD	RW
PRT3IC0	0E	RW		4E	RW		8E	RW		CE	RW
PRT3IC1	0F	RW		4F			8F	RW		CF	RW
PRT4DM0	10	RW	CMP0CR1	50	RW		90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52	RW		92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93	RW	GDI_E_OU	D3	RW
	14	RW	CMP1CR1	54	RW		94	RW		D4	RW
	15	RW	CMP1CR2	55	RW		95	RW		D5	RW
	16	RW		56	RW		96	RW		D6	RW
	17	RW	VDAC51CR0	57	RW		97	RW		D7	RW
	18	RW	CSCMPCR0	58	#		98	RW	MUX_CR0	D8	RW
	19	RW	CSCMPGOEN	59	RW		99	RW	MUX_CR1	D9	RW
	1A	RW	CSLUTCR0	5A	RW		9A	RW	MUX_CR2	DA	RW
	1B	RW	CMPCOLMUX	5B	RW		9B	RW	MUX_CR3	DB	RW
	1C	RW	CMPPWMCR	5C	RW		9C	RW	DAC_CR1#	DC	RW
	1D	RW	CMPFLTCR	5D	RW		9D	RW	OSC_GO_EN	DD	RW
	1E	RW	CMPCLK1	5E	RW		9E	RW	OSC_CR4	DE	RW
	1F	RW	CMPCLK0	5F	RW		9F	RW	OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR*	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR*	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW		6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE	RW	MUX_CR6	EE	RW
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF	RW	MUX_CR7	EF	RW
DBC10FN	30	RW		70	RW	RDI0RI	B0	RW	CPU_A	F0	#
DBC10IN	31	RW		71	RW	RDI0SYN	B1	RW	CPU_T1	F1	#
DBC10OU	32	RW	ACB00CR1*	72	RW	RDI0IS	B2	RW	CPU_T2	F2	#
DBC10CR1	33	RW	ACB00CR2*	73	RW	RDI0LT0	B3	RW	CPU_X	F3	#
DBC11FN	34	RW		74	RW	RDI0LT1	B4	RW	CPU_PCL	F4	#
DBC11IN	35	RW		75	RW	RDI0RO0	B5	RW	CPU_PCH	F5	#
DBC11OU	36	RW	ACB01CR1*	76*	RW	RDI0RO1	B6	RW	CPU_SP	F6	#
DBC11CR1	37	RW	ACB01CR2*	77*	RW	RDI0DSM	B7	RW	CPU_F	F7	I
DCC12FN	38	RW		78	RW	RDI1RI	B8	RW	FLS_PR0	F8	RW
DCC12IN	39	RW		79	RW	RDI1SYN	B9	RW	FLS_TR	F9	W
DCC12OU	3A	RW		7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C	RW	RDI1LT1	BC	RW	FAC_CR0	FC	SW
DCC13IN	3D	RW		7D	RW	RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

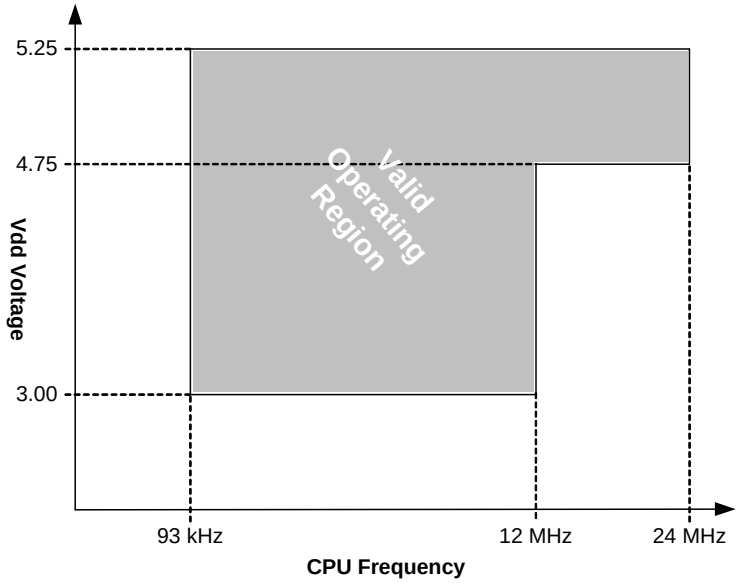
Shaded fields are Reserved and must not be accessed. **# Access is bit specific. * has a different meaning.**

Electrical Specifications

This section presents the DC and AC electrical specifications of this PSoC device family. For the latest electrical specifications, check the most recent data sheet by visiting http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40 °C ≤ T_A ≤ 70 °C and T_J ≤ 82 °C.

Figure 5. Voltage versus Operating Frequency



DC Electrical Characteristics

DC Chip Level Specifications

Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C, and are for design guidance only, unless specified otherwise.

Table 9. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply voltage	3.0	–	5.25	V	See Table 17 on page 19
I_{DD}	Supply current	–	7	12	mA	Conditions are Vdd = 5.0 V, 25°C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz VC2 = 93.75 kHz VC3 = 93.75 kHz
I_{DD3}	Supply current	–	4	7	mA	Conditions are Vdd = 3.3 V T_A = 25 °C, CPU = 3 MHz 48 MHz = Disabled VC1 = 1.5 MHz, VC2 = 93.75 kHz VC3 = 93.75 kHz
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT[8]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3 V –40°C <= T_A <= 55°C
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature[8]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3 V 55 °C < T_A <= 85 °C
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal[8]	–	4	7.5	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3 V, –40 °C <= T_A <= 55 °C
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature [8]	–	5	26	µA	Conditions are with properly loaded, 1µW max, 32.768 kHz crystal. Vdd = 3.3 V, 55 °C < T_A <= 85 °C
V_{REF}	Reference Voltage (Bandgap)	1.275	1.3	1.325	V	Trimmed for appropriate Vdd

Note
8. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 11. 5 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[10]	Input leakage current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode Voltage Range	0.0	–	Vdd - 1	V	

Table 12. 3.3 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[10]	Input leakage current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	Vdd – 1	V	

DC IDAC Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 13. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$IDAC_{GAIN}$	IDAC gain	–	75.4	218	nA/bit	IDAC gain at 1x current gain
		–	335	693	nA/bit	IDAC gain at 4x current gain
		–	1160	2410	nA/bit	IDAC gain at 16x current gain
		–	2340	5700	nA/bit	IDAC gain at 32x current gain
	Monotonicity	No	–	–	–	IDAC gain is non-monotonous at step intervals of (0x10)
$IDAC_{GAIN\_VAR}$	IDAC gain variation over temperature –40 °C to 85 °C	–	3.22	–	nA	at 1x current gain
		–	18.1	–	nA	at 4x current gain
		–	59.9	–	nA	at 16x current gain
		–	120	–	nA	at 32x current gain
I_{IDAC}	IDAC current at maximum code (0xFF)	–	19.2	–	µA	at 1x current gain
		–	85.4	–	µA	at 4x current gain
		–	295	–	µA	at 16x current gain
		–	596	–	µA	at 32x current gain

Note
10. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

DC Low Power Comparator Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd – 1	V	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

SAR10 ADC DC Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 15. SAR10 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{adcvref}$	Reference voltage at pin P2[5] when configured as ADC reference voltage	3.0	–	5.25	V	When V_{REF} is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on Vdd pin. ($V_{adcvref}$ < Vdd)
$I_{adcvref}$	Current when P2[5] is configured as ADC V_{REF}	–	–	0.5	mA	Disables the internal voltage reference buffer
INL at 10 bits	Integral Nonlinearity	–2.5	–	2.5	LSB	For V_{DD} ≥ 3.0 V and Vref ≥ 3.0 V
		–5.0	–	5.0	LSB	For V_{DD} < 3.0 V or Vref < 3.0 V
DNL at 10 bits	Differential Nonlinearity	–1.5	–	1.5	LSB	For V_{DD}≥ 3.0 V and Vref ≥ 3.0 V
		–4.0	–	4.0	LSB	For V_{DD} < 3.0 V or Vref < 3.0 V
SPS [11]	Sample per second	–	–	150	ksps	Resolution 10 bits

Note
11. Errata: When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data. For more information, see "Errata" on page 35.

DC Analog Mux Bus Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400	Ω	Vdd ≥ 3.00
R_{gnd}	Resistance of Initialization Switch to gnd	–	–	800	Ω	

DC POR and LVD Specifications

Table 17 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 17. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR1} V_{PPOR2}	Vdd Value for PPOR Trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.55	2.95 4.70	V V	Vdd must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd Value for LVD Trip VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.95 3.06 4.37 4.50 4.62 4.71	3.02 3.13 4.48 4.64 4.73 4.81	3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V	

DC Programming Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply Current during Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage during Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage during Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] during Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] during Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage during Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage during Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)[13]	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[12]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

DC I^2C Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 19. DC I^2C Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}[14]	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}[14]	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Note
12. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
13. The 50,000 cycle Flash endurance per block is guaranteed only if the Flash operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V
14. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections.The I^2C GPIO pins also meet the above specs.

AC Programming Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, or 3.3 V at 25 °C and are for design guidance only.

Table 28. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
F_{SCLK3}	Frequency of SCLK3	0	–	6	MHz	V_{DD} < 3.6 V
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	40	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	3.6 < Vdd; at 30 pF Load
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	65	ns	3.0 ≤ Vdd ≤ 3.6; at 30 pF Load
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ns	
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100	ms	
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200	ms	

Packaging Information

Figure 8. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026

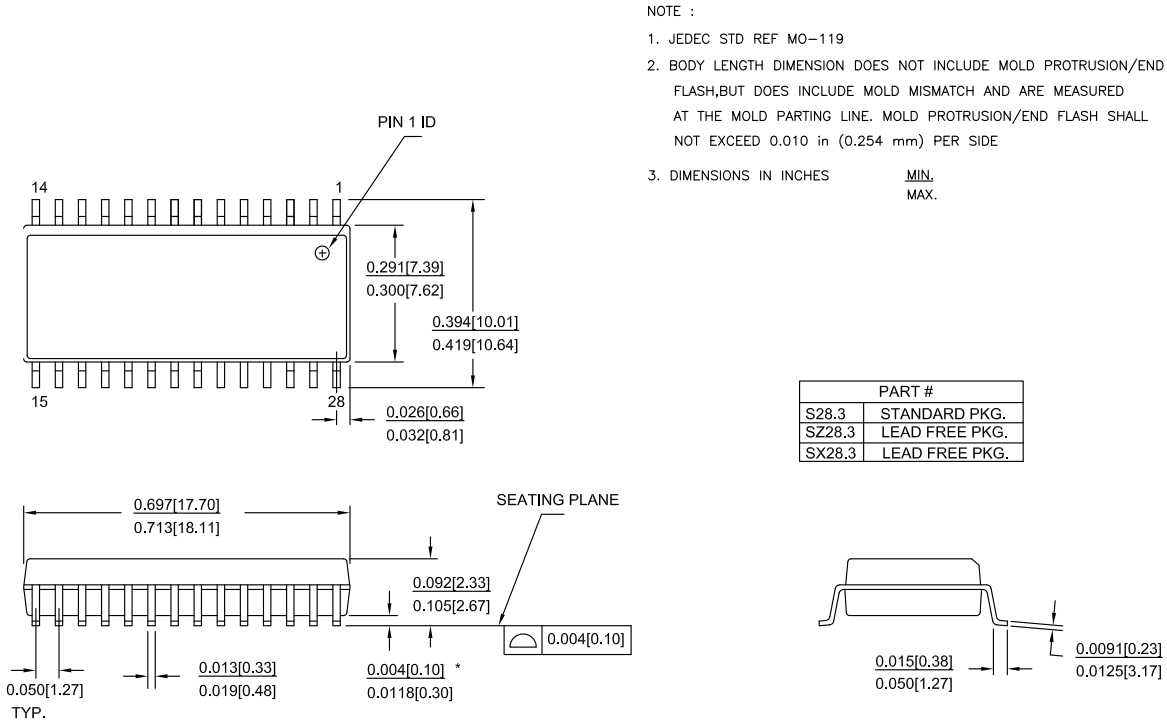
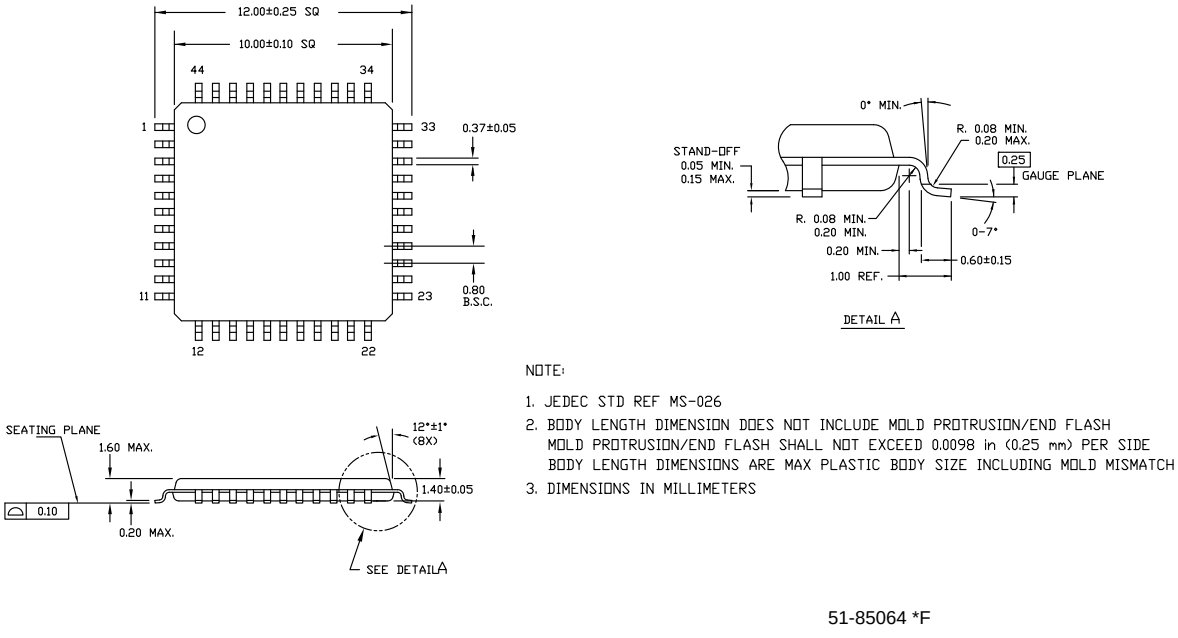


Figure 9. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064



Thermal Impedances

Table 30. Thermal Impedances per Package

Package	Typical θ_{JA} [25]
28-pin SOIC	68 °C/W
44-pin TQFP	61 °C/W

Solder Reflow Specifications

Table 31 shows the solder reflow temperature limits that must not be exceeded.

Table 31. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds

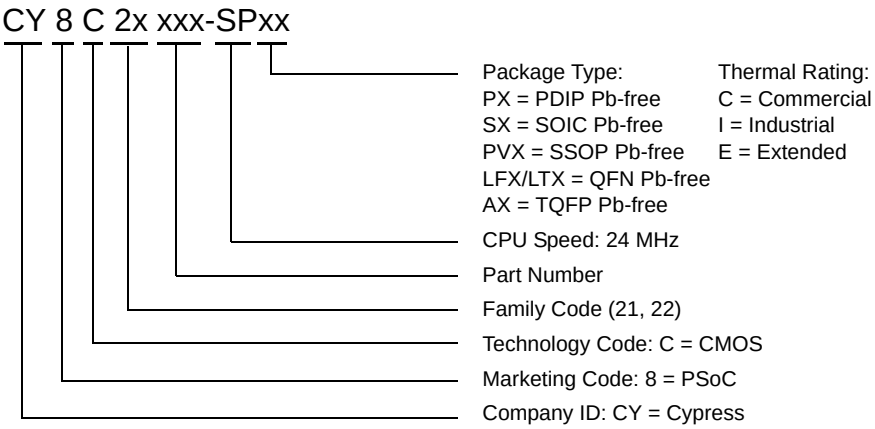
Ordering Information

The following table lists the key package features and ordering codes of this PSoC device family.

Table 32. PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin SOIC	CY8C21345-24SXI	8	512B	–40 °C to +85 °C	4	6	24	24[24]	0	Y
28-pin SOIC (Tape and Reel)	CY8C21345-24SXIT	8	512B	–40 °C to +85 °C	4	6	24	24[24]	0	Y
28-pin SOIC	CY8C22345-24SXI	16	1K	–40 °C to +85 °C	8	6	24	24[24]	0	Y
28-pin SOIC (Tape and Reel)	CY8C22345-24SXIT	16	1K	–40 °C to +85 °C	8	6	24	24[24]	0	Y
44-pin TQFP	CY8C22545-24AXI	16	1K	–40 °C to +85 °C	8	6	38	38[24]	0	Y
44-pin TQFP (Tape and Reel)	CY8C22545-24AXIT	16	1K	–40 °C to +85 °C	8	6	38	38[24]	0	Y

Ordering Code Definitions



Note
24. Ten direct inputs.
25. $T_J = T_A + POWER \times \theta_{JA}$

Acronyms

Table 33 lists the acronyms that are used in this document.

Table 33. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MAC	multiply-accumulate
ADC	analog-to-digital converter	MCU	microcontroller unit
API	application programming interface	MIPS	million instructions per second
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CSD	CapSense sigma delta	POR	power on reset
CT	continuous time	PPOR	precision power on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DNL	differential nonlinearity	PWM	pulse width modulator
ECO	external crystal oscillator	QFN	quad flat no leads
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
FSK	frequency-shift keying	SAR	successive approximation
GPIO	general-purpose I/O	SC	switched capacitor
I/O	input/output	SLIMO	slow IMO
ICE	in-circuit emulator	SOIC	small-outline integrated circuit
IDE	integrated development environment	SPI™	serial peripheral interface
IDAC	current DAC	SRAM	static random access memory
ILO	internal low speed oscillator	SROM	supervisory read only memory
IMO	internal main oscillator	SSOP	shrink small-outline package
INL	integral nonlinearity	TQFP	thin quad flat pack
IrDA	infrared data association	UART	universal asynchronous receiver / transmitter
ISSP	in-system serial programming	USB	universal serial bus
LPC	low power comparator	WDT	watchdog timer
LSB	least-significant bit	XRES	external reset
LVD	low voltage detect		

Reference Documents

CY8C22x45 and CY8C21345 PSoC® Programmable System-on-Chip™ *Technical Reference Manual (TRM)* (001-48461)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand.
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY8C21345	All Variants
CY8C22345	All Variants
CY8C22545	All Variants

CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

Errata Summary

The following table defines the errata applicable for this PSoC family device.

Items	Part Number	Silicon Revision	Fix Status
1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.
2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.

1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

■ Problem Definition

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

■ Parameters Affected

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

■ Trigger Condition(S)

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

■ Scope of Impact

Inaccurate output is possible.

■ Workaround

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- ❒ Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- ❒ Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

■ Fix Status

No silicon fix is planned.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ Problem Definition

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ Parameters Affected

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ Trigger Condiiton(S)

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

■ Workaround

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ Fix Status

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.

Document History Page

Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip Document Number: 001-43084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2251907	PMP / AESA	See ECN	New data sheet.
*A	2506377	EIJ / AESA	See ECN	Changed data sheet status to “Preliminary”. Changed part numbers to CY8C22x45. Updated data sheet template. Added 56-Pin OCD information. Added: “You must put filters on intended ADC input channels for anti-aliasing. This ensures that any out-of-band content is not folded into the Input Signal Band." To Section Analog System on page 4. Corrected Minimum Electro Static Discharge Voltage in Table 7 on page 14.
*B	2558750	PMP / AESA	08/28/2008	Updated Features on page 1, PSoC Core on page 3, Analog System on page 4. Changed DBB to DBC, and DCB to DCC in Register Tables Table 5 on page 11 and Table 6 on page 12. Removed INL at 8 bit reference in Table 15 on page 18. Changed IDD3 value Table 17 on page 19 Typ:3.3 mA, Max 6 mA Added “3.0 V < Vdd < 3.6 V and -40C < T_A < 85C, IMO can guarantee 5% accuracy only” to Table 20 on page 21. Updated data sheet template.
*C	2606793	NUQ / AESA	11/19/2008	Updated data sheet status to “Final”. Updated block diagram on page 1. Removed CY8C22045 56-Pin OCD information. Added part numbers CY8C21345, CY8C22345, and CY8C22545. For more details, see CDT 31271.
*D	2615697	PMP / AESA	12/03/2008	Confirmed CY8C22345 and CY8C21345 have same pinout on page 8. Confirmed that IMO has 5% accuracy in Table 20 on page 21.
*E	2631733	PMP / PYRS	01/07/2009	Updated Table 16. SAR10 ADC DC Specifications and Table 29 AC Programming Specifications. Title changed to “CY8C21345, CY8C22345, CY8C22545 PSoC® Programmable System-on-Chip™”
*F	2648800	JHU / AESA	01/28/2009	Updated INL, DNL information in Table 15 on page 18, Development Tools on page 6, and T_{DSCLK} parameter in Table 28 on page 25.
*G	2658078	HMI / AESA	02/11/2009	Updated section Features on page 1.
*H	2667311	JHU / AESA	03/16/2009	Added parameter “F_{32KU}” and added Min% and Max % to parameter “F_{IMO6}” in Table 20 on page 21, according to updated SLIMO spec.
*I	2748976	JZHU / PYRS	08/06/2009	Updated F_{32K1} max rating in Table 20 on page 21.
*J	2786560	JZHU	10/23/2009	Added DC_{ILO}, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, $T_{PROGRAM\_COLD}$, $SR_{POWERUP}$, I_{OH}, and I_{OL} parameters. Added Tape and Reel parts in Ordering Information table
*K	2901653	NJF	03/30/2010	Updated PSoC Designer Software Subsystems. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Modified Note 6 on page 17. Added F_{OUT48M} parameter in 5 V and 3.3 V AC Chip-Level Specifications. Removed AC Analog Mux Bus Specifications. Updated Ordering Code Definitions. Updated links in Sales, Solutions, and Legal Information.
*L	3114978	NJF	12/19/10	Added DC I^2C Specifications. Added Tjit_IMO specification, removed existing jitter specifications. Updated DC Programming Specifications. Updated AC Digital Block Specifications. Updated I^2C Timing Diagram. Added Solder Reflow Peak Temperature table. Updated Units of Measure, Acronyms, Glossary, and References sections.

Document History Page (continued)

Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip Document Number: 001-43084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*M	3231771	BOBH / ECU	04/18/11	Updated analog inputs column in Table 32 on page 28 and included reference to Note 24. Updated the following sections: Getting Started, Development Tools, and Designing with PSoC Designer as all the System level designs have been de-emphasized. Updated Table 31, “Solder Reflow Specifications,” on page 28. Updated package diagrams: 51-85026 to *F 51-85064 to *E
*N	3578757	PMAD	04/11/2012	Removed reference to AN2012 as the document is in obsolete status. Updated template. No technical updates. Completing sunset review.
*O	3598230	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*P	3915358	SAMP	02/27/2013	Updated Electrical Specifications (Updated DC Electrical Characteristics (Updated DC GPIO Specifications (Updated Table 10 (Updated Notes for V_{OH} and V_{OL} parameters)))).
*Q	3959550	SAMP	04/09/2013	Added Errata.
*R	4081559	PMAD	07/30/2013	Added Errata footnotes (Note 1, 11, 15). Updated Features: Added Note 1 and referred the same note in ±5% under “Precision, programmable clocking”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated SAR10 ADC DC Specifications: Added Note 11 and referred the same note in SPS parameter. Updated AC Electrical Characteristics: Updated AC Chip Level Specifications: Added Note 15 and referred the same note in F_{IMO24} parameter. Updated Packaging Information: spec 51-85026 – Changed revision from *F to *G. Updated Errata. Updated in new template.
*S	4416752	RAHU	06/26/2014	Updated Pinouts: Updated CY8C22345, CY8C21345 28-pin SOIC: Updated Note 6. Updated CY8C22545 44-pin TQFP: Updated Table 3: Replaced “TC” with “ISSP” in description of pin 16 and pin 18. Updated Packaging Information: spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F.

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