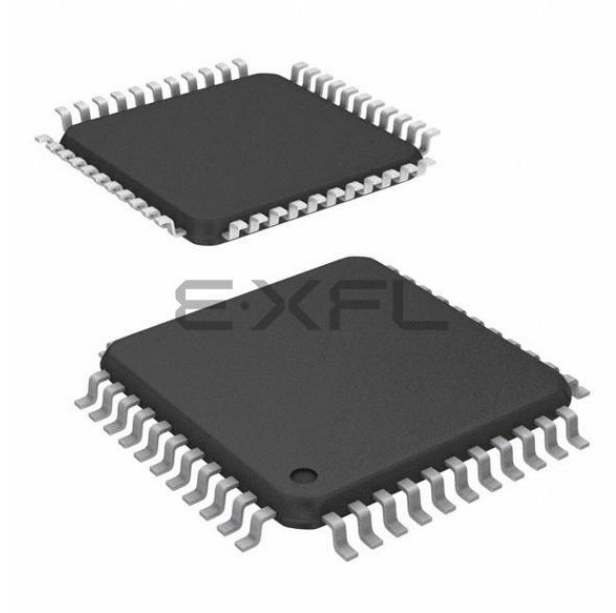

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c22545-24axit

PSoC Functional Overview

The PSoC family consists of many On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with one low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in Figure 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows the combining of all the device resources into a complete custom system. The PSoC family can have up to five I/O ports connecting to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general-purpose I/O (GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 21 vectors, to simplify the programming of real time embedded events.

Program execution is timed and protected using the included Sleep and watchdog timers (WDT).

Memory encompasses 16 KB of Flash for program storage, 1 K bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

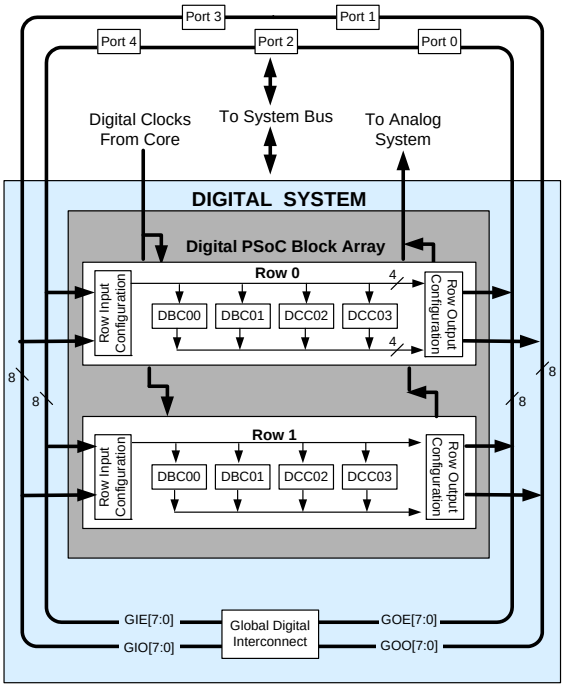
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator). The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the Sleep timer and WDT. If crystal accuracy is required, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC), and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin can also generate a system interrupt on high level, low level, and change from last read.

Digital System

The Digital System is composed of eight digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations are:

- PWMs (8- and 16-Bit)
- PWMs with Dead band (8- and 16-Bit)
- Counters (8 to 32-Bit)
- Timers (8 to 32-Bit)
- UART 8 Bit with Selectable Parity (Up to Two)
- SPI Master and Slave (Up to Two)
- Shift Register (1 to 32-Bit)
- I2C Slave and Master (One Available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32-Bit)
- IrDA (Up to Two)
- Pseudo Random Sequence Generators (8 to 32-Bit)

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Analog System

The Analog System consists of a 10-bit SAR ADC and six configurable blocks.

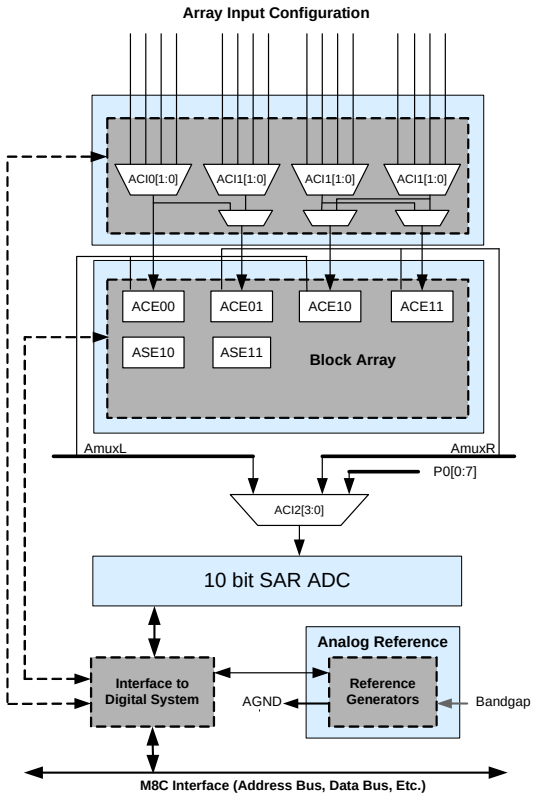
The programmable 10-bit SAR ADC is an optimized ADC that can be run up to 200 ksps with ± 1.5 LSB DNL and ± 2.5 LSB INL (true for $V_{DD} \geq 3.0$ V and Vref ≥ 3.0 V). External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-Digital converters (Single or Dual, with 8-bit resolution)
- Pin-to-pin Comparator
- Single ended comparators with absolute (1.3 V) reference or 5-bit DAC reference
- 1.3 V reference (as a System Resource)

Analog blocks are provided in columns of four, which include CT-E (Continuous Time) and SC-E (Switched Capacitor) blocks. These devices provide limited functionality Type “E” analog blocks.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Additional Digital resources and clocks optimized for CSD.
- Support “RTC” block into digital peripheral logic.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

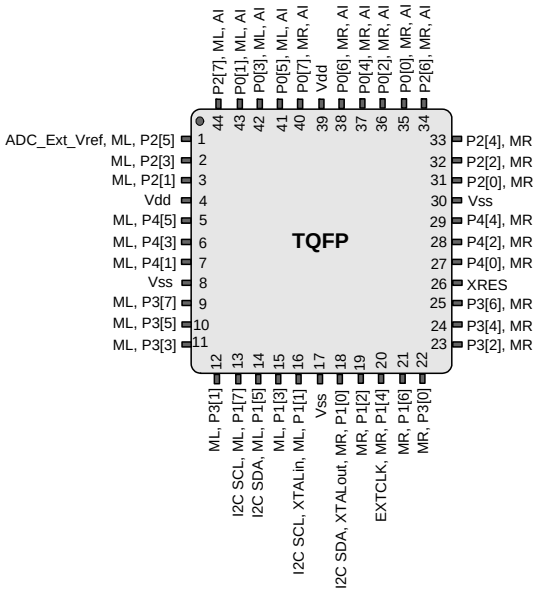
CY8C22545 44-pin TQFP

Table 3. Pin Definitions [7]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	ML	P2[5]	Optional ADC External Vref
2	I/O	ML	P2[3]	
3	I/O	ML	P2[1]	
4	Power		Vdd	Supply Voltage
5	I/O	ML	P4[5]	
6	I/O	ML	P4[3]	
7	I/O	ML	P4[1]	
8	Power		Vss	Ground Connection
9	I/O	ML	P3[7]	
10	I/O	ML	P3[5]	
11	I/O	ML	P3[3]	
12	I/O	ML	P3[1]	
13	I/O	ML	P1[7]	I2C serial clock (SCL)
14	I/O	ML	P1[5]	I2C serial data (SDA)
15	I/O	ML	P1[3]	
16	I/O	ML	P1[1]	Crystal (XTALin), I2C SCL, ISSP SCLK[6]
17	Power		Vss	Ground Connection
18	I/O	MR	P1[0]	Crystal (XTALout), I2C SDA, ISSP SDATA[6]
19	I/O	MR	P1[2]	
20	I/O	MR	P1[4]	Optional external clock input (EXTCLK)
21	I/O	MR	P1[6]	
22	I/O	MR	P3[0]	
23	I/O	MR	P3[2]	
24	I/O	MR	P3[4]	
25	I/O	MR	P3[6]	
26	Input		XRES	Active High Pin Reset with Internal Pull Down
27	I/O	MR	P4[0]	
28	I/O	MR	P4[2]	
29	I/O	MR	P4[4]	
30	Power		Vss	Ground Connection
31	I/O	MR	P2[0]	
32	I/O	MR	P2[2]	
33	I/O	MR	P2[4]	
34	I/O	I, MR	P2[6]	To Compare Column 1
35	I/O	I, MR	P0[0]	
36	I/O	I, MR	P0[2]	
37	I/O	I, MR	P0[4]	
38	I/O	I, MR	P0[6]	
39	Power		Vdd	Supply Voltage
40	I/O	I, MR	P0[7]	Integration Capacitor for MR
41	I/O	I, ML	P0[5]	Integration Capacitor for ML
42	I/O	I, ML	P0[3]	
43	I/O	I, ML	P0[1]	
44	I/O	I, ML	P2[7]	To Compare Column 0

LEGEND: A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input.

Figure 4. Pin Diagram



Note
7. All V_{SS} pins should be brought out to one common GND plane.

Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer the *PSoC Programmable System-on Chip Technical Reference Manual*.

Register Conventions

Table 4. Abbreviations

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts. The XIO bit in the Flag register determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	0	RW		40	RW	ASC10CR0*	80*	RW		C0	RW
PRT0DM1	1	RW		41	RW		81	RW		C1	RW
PRT0IC0	2	RW		42	RW		82	RW		C2	RW
PRT0IC1	3	RW		43			83	RW		C3	RW
PRT1DM0	4	RW		44	RW	ASD11CR0*	84*	RW		C4	RW
PRT1DM1	5	RW		45	RW		85	RW		C5	RW
PRT1IC0	6	RW		46	RW		86	RW		C6	RW
PRT1IC1	7	RW		47			87	RW		C7	RW
PRT2DM0	8	RW		48	RW		88	RW		C8	#
PRT2DM1	9	RW		49	RW		89	RW		C9	RW
PRT2IC0	0A	RW		4A	RW		8A	RW		CA	RW
PRT2IC1	0B	RW		4B			8B	RW		CB	RW
PRT3DM0	0C	RW		4C	RW		8C	RW		CC	#
PRT3DM1	0D	RW		4D	RW		8D	RW		CD	RW
PRT3IC0	0E	RW		4E	RW		8E	RW		CE	RW
PRT3IC1	0F	RW		4F			8F	RW		CF	RW
PRT4DM0	10	RW	CMP0CR1	50	RW		90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52	RW		92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93	RW	GDI_E_OU	D3	RW
	14	RW	CMP1CR1	54	RW		94	RW		D4	RW
	15	RW	CMP1CR2	55	RW		95	RW		D5	RW
	16	RW		56	RW		96	RW		D6	RW
	17	RW	VDAC51CR0	57	RW		97	RW		D7	RW
	18	RW	CSCMPCR0	58	#		98	RW	MUX_CR0	D8	RW
	19	RW	CSCMPGOEN	59	RW		99	RW	MUX_CR1	D9	RW
	1A	RW	CSLUTCR0	5A	RW		9A	RW	MUX_CR2	DA	RW
	1B	RW	CMPCOLMUX	5B	RW		9B	RW	MUX_CR3	DB	RW
	1C	RW	CMPPWMCR	5C	RW		9C	RW	DAC_CR1#	DC	RW
	1D	RW	CMPFLTCR	5D	RW		9D	RW	OSC_GO_EN	DD	RW
	1E	RW	CMPCLK1	5E	RW		9E	RW	OSC_CR4	DE	RW
	1F	RW	CMPCLK0	5F	RW		9F	RW	OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR*	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR*	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW		6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE	RW	MUX_CR6	EE	RW
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF	RW	MUX_CR7	EF	RW
DBC10FN	30	RW		70	RW	RDI0RI	B0	RW	CPU_A	F0	#
DBC10IN	31	RW		71	RW	RDI0SYN	B1	RW	CPU_T1	F1	#
DBC10OU	32	RW	ACB00CR1*	72	RW	RDI0IS	B2	RW	CPU_T2	F2	#
DBC10CR1	33	RW	ACB00CR2*	73	RW	RDI0LT0	B3	RW	CPU_X	F3	#
DBC11FN	34	RW		74	RW	RDI0LT1	B4	RW	CPU_PCL	F4	#
DBC11IN	35	RW		75	RW	RDI0RO0	B5	RW	CPU_PCH	F5	#
DBC11OU	36	RW	ACB01CR1*	76*	RW	RDI0RO1	B6	RW	CPU_SP	F6	#
DBC11CR1	37	RW	ACB01CR2*	77*	RW	RDI0DSM	B7	RW	CPU_F	F7	I
DCC12FN	38	RW		78	RW	RDI1RI	B8	RW	FLS_PR0	F8	RW
DCC12IN	39	RW		79	RW	RDI1SYN	B9	RW	FLS_TR	F9	W
DCC12OU	3A	RW		7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C	RW	RDI1LT1	BC	RW	FAC_CR0	FC	SW
DCC13IN	3D	RW		7D	RW	RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Shaded fields are Reserved and must not be accessed. **# Access is bit specific. * has a different meaning.**

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduce data retention time
$T_{BAKETEMP}$	Bake temperature	–	125	See Package label	°C	
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
Vdd	Supply voltage on Vdd relative to Vss	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOz}	DC voltage applied to tristate	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electr static discharge voltage	2000	–	–	V	Human Body Model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 30 on page 28. The user must limit the power consumption to comply with this requirement.

DC Low Power Comparator Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd – 1	V	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

SAR10 ADC DC Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 15. SAR10 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{adcvref}$	Reference voltage at pin P2[5] when configured as ADC reference voltage	3.0	–	5.25	V	When V_{REF} is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on Vdd pin. ($V_{adcvref}$ < Vdd)
$I_{adcvref}$	Current when P2[5] is configured as ADC V_{REF}	–	–	0.5	mA	Disables the internal voltage reference buffer
INL at 10 bits	Integral Nonlinearity	–2.5	–	2.5	LSB	For V_{DD} ≥ 3.0 V and Vref ≥ 3.0 V
		–5.0	–	5.0	LSB	For V_{DD} < 3.0 V or Vref < 3.0 V
DNL at 10 bits	Differential Nonlinearity	–1.5	–	1.5	LSB	For V_{DD}≥ 3.0 V and Vref ≥ 3.0 V
		–4.0	–	4.0	LSB	For V_{DD} < 3.0 V or Vref < 3.0 V
SPS [11]	Sample per second	–	–	150	ksps	Resolution 10 bits

Note
11. Errata: When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data. For more information, see "Errata" on page 35.

DC Analog Mux Bus Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400	Ω	Vdd ≥ 3.00
R_{gnd}	Resistance of Initialization Switch to gnd	–	–	800	Ω	

DC POR and LVD Specifications

Table 17 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 17. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR1} V_{PPOR2}	Vdd Value for PPOR Trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.55	2.95 4.70	V V	Vdd must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd Value for LVD Trip VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.95 3.06 4.37 4.50 4.62 4.71	3.02 3.13 4.48 4.64 4.73 4.81	3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V	

DC Programming Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply Current during Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage during Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage during Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] during Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] during Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage during Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage during Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)[13]	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[12]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

DC I^2C Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 19. DC I^2C Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}[14]	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}[14]	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Note
12. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
13. The 50,000 cycle Flash endurance per block is guaranteed only if the Flash operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V
14. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections.The I^2C GPIO pins also meet the above specs.

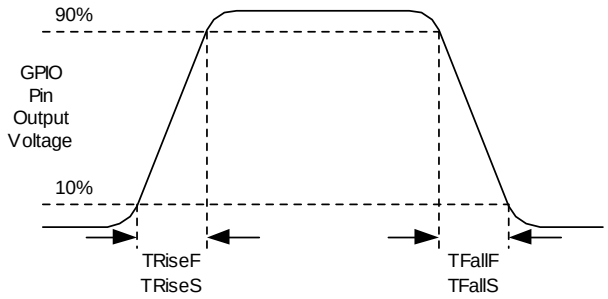
AC GPIO Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 21. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25 V, 10% to 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25 V, 10% to 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	7	27	–	ns	Vdd = 3 to 5.25 V, 10% to 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	7	22	–	ns	Vdd = 3 to 5.25 V, 10% to 90%

Figure 6. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 22. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Mode Response Time, 50 mV			100	ns	Vdd ≥ 3.0 V

AC Low Power Comparator Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 23. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V, at 25 °C and are for design guidance only.

Table 24. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block Input Clock Frequency					
	Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
Timer	Input Clock Frequency					
	No Capture, Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	No Capture, Vdd < 4.75 V	–	–	25.2[21]	MHz	
	With Capture	–	–	25.2[21]	MHz	
	Capture Pulse Width	50[22]	–	–	ns	
Counter	Input Clock Frequency					
	No Enable Input, Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	No Enable Input, Vdd < 4.75 V	–	–	25.2[21]	MHz	
	With Enable Input	–	–	25.2[21]	MHz	
	Enable Input Pulse Width	50[22]	–	–	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[22]	–	–	ns	
	Disable Mode	50[22]	–	–	ns	
	Input Clock Frequency					
	Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
CRCPRS (PRS Mode)	Input Clock Frequency					
	Vdd ≥ 4.75 V	–	–	50.4[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	–	–	25.2[21]	MHz	
SPIM	Input Clock Frequency	–	–	8.4[21]	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.2[21]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50[22]	–	–	ns	
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	Vdd ≥ 4.75 V, 2 Stop Bits	–	–	50.4[21]	MHz	
	Vdd ≥ 4.75 V, 1 Stop Bit	–	–	25.2[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	Vdd ≥ 4.75 V, 2 Stop Bits	–	–	50.4[21]	MHz	
	Vdd ≥ 4.75 V, 1 Stop Bit	–	–	25.2[21]	MHz	
	Vdd < 4.75 V	–	–	25.2[21]	MHz	

Notes
21. Accuracy derived from IMO with appropriate trim for V_{DD} range.
22. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 25. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 26. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

SAR10 ADC AC Specifications

Table 27 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. SAR10 ADC AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$Freq_3$	Input clock frequency 3 V	–	–	2.7	MHz	
$Freq_5$	Input clock frequency 5 V	–	–	2.7	MHz	

AC Programming Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, or 3.3 V at 25 °C and are for design guidance only.

Table 28. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
F_{SCLK3}	Frequency of SCLK3	0	–	6	MHz	V_{DD} < 3.6 V
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	40	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	3.6 < Vdd; at 30 pF Load
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	65	ns	3.0 ≤ Vdd ≤ 3.6; at 30 pF Load
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ns	
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100	ms	
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200	ms	

Packaging Information

Figure 8. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026

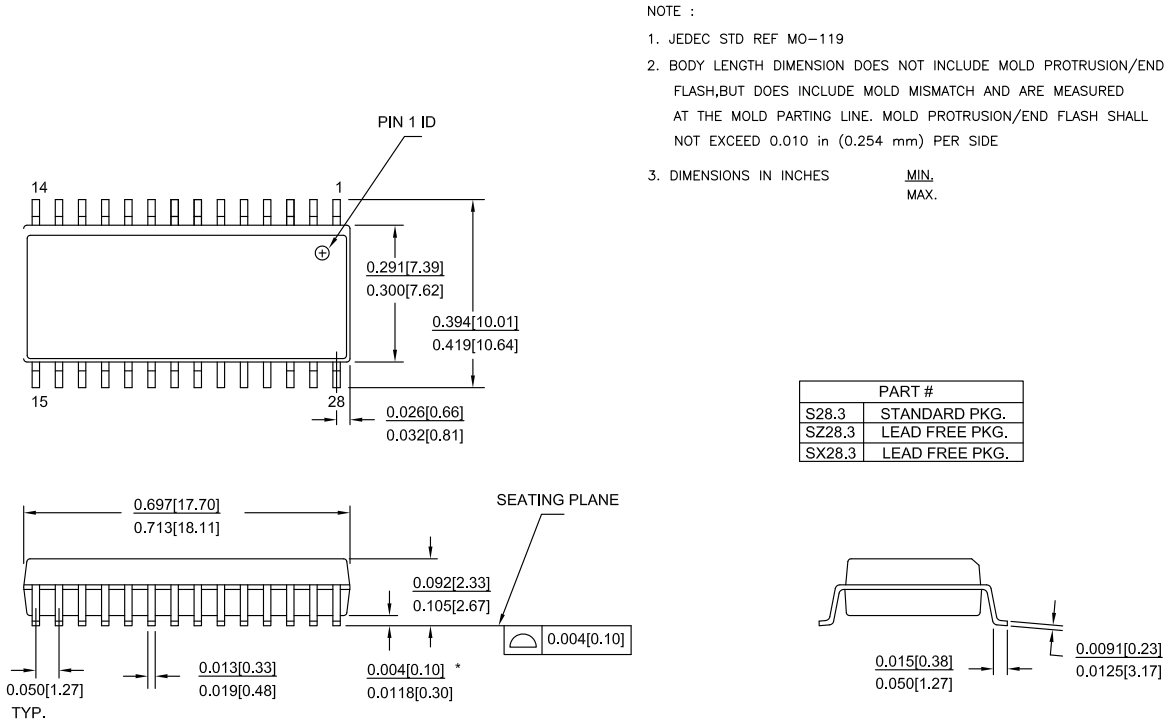
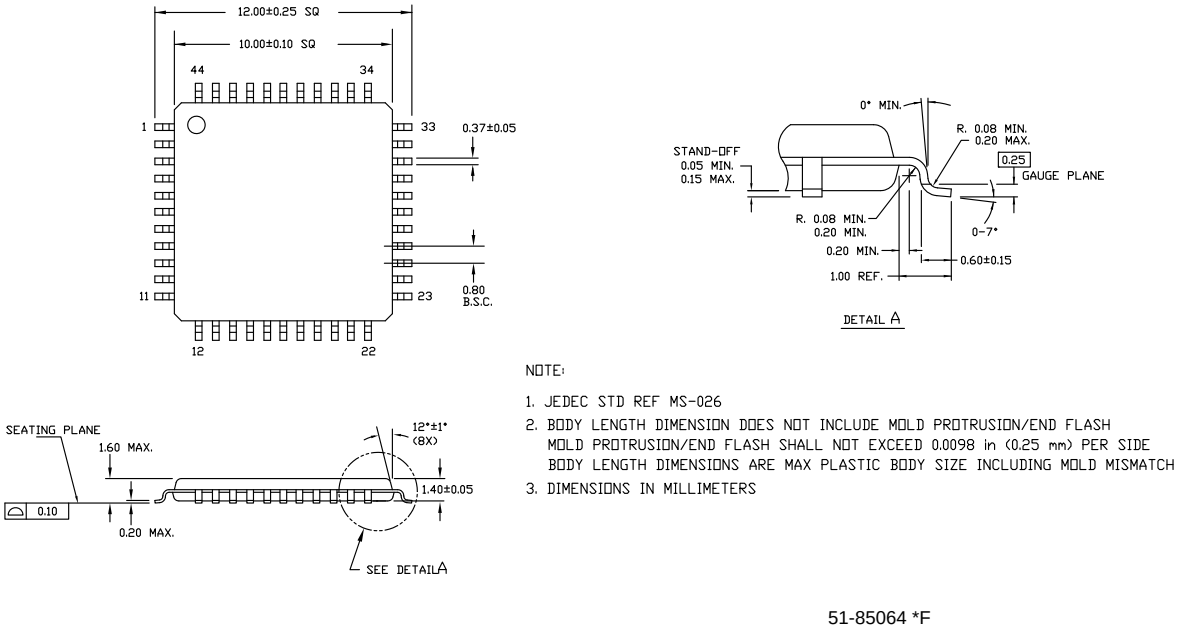


Figure 9. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064



Acronyms

Table 33 lists the acronyms that are used in this document.

Table 33. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MAC	multiply-accumulate
ADC	analog-to-digital converter	MCU	microcontroller unit
API	application programming interface	MIPS	million instructions per second
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CSD	CapSense sigma delta	POR	power on reset
CT	continuous time	PPOR	precision power on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DNL	differential nonlinearity	PWM	pulse width modulator
ECO	external crystal oscillator	QFN	quad flat no leads
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
FSK	frequency-shift keying	SAR	successive approximation
GPIO	general-purpose I/O	SC	switched capacitor
I/O	input/output	SLIMO	slow IMO
ICE	in-circuit emulator	SOIC	small-outline integrated circuit
IDE	integrated development environment	SPI™	serial peripheral interface
IDAC	current DAC	SRAM	static random access memory
ILO	internal low speed oscillator	SROM	supervisory read only memory
IMO	internal main oscillator	SSOP	shrink small-outline package
INL	integral nonlinearity	TQFP	thin quad flat pack
IrDA	infrared data association	UART	universal asynchronous receiver / transmitter
ISSP	in-system serial programming	USB	universal serial bus
LPC	low power comparator	WDT	watchdog timer
LSB	least-significant bit	XRES	external reset
LVD	low voltage detect		

Reference Documents

CY8C22x45 and CY8C21345 PSoC® Programmable System-on-Chip™ *Technical Reference Manual (TRM)* (001-48461)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products

Document Conventions

Units of Measure

Table 34 lists the units of measures.

Table 34. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	mV	millivolts
°C	degree Celsius	nA	nanoampere
kHz	kilohertz	ns	nanosecond
kΩ	kilohm	W	ohm
LSB	least significant bit	%	percent
MHz	megahertz	pF	picofarad
µA	microampere	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolt	pA	pikoampere
mA	milliampere	V	volts
mm	millimeter	µW	microwatts
ms	millisecond	W	watt

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses Vdd and provides an interrupt to the system when Vdd falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Document History Page (continued)

Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip Document Number: 001-43084				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*M	3231771	BOBH / ECU	04/18/11	Updated analog inputs column in Table 32 on page 28 and included reference to Note 24. Updated the following sections: Getting Started, Development Tools, and Designing with PSoC Designer as all the System level designs have been de-emphasized. Updated Table 31, “Solder Reflow Specifications,” on page 28. Updated package diagrams: 51-85026 to *F 51-85064 to *E
*N	3578757	PMAD	04/11/2012	Removed reference to AN2012 as the document is in obsolete status. Updated template. No technical updates. Completing sunset review.
*O	3598230	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*P	3915358	SAMP	02/27/2013	Updated Electrical Specifications (Updated DC Electrical Characteristics (Updated DC GPIO Specifications (Updated Table 10 (Updated Notes for V_{OH} and V_{OL} parameters)))).
*Q	3959550	SAMP	04/09/2013	Added Errata.
*R	4081559	PMAD	07/30/2013	Added Errata footnotes (Note 1, 11, 15). Updated Features: Added Note 1 and referred the same note in ±5% under “Precision, programmable clocking”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated SAR10 ADC DC Specifications: Added Note 11 and referred the same note in SPS parameter. Updated AC Electrical Characteristics: Updated AC Chip Level Specifications: Added Note 15 and referred the same note in F_{IMO24} parameter. Updated Packaging Information: spec 51-85026 – Changed revision from *F to *G. Updated Errata. Updated in new template.
*S	4416752	RAHU	06/26/2014	Updated Pinouts: Updated CY8C22345, CY8C21345 28-pin SOIC: Updated Note 6. Updated CY8C22545 44-pin TQFP: Updated Table 3: Replaced “TC” with “ISSP” in description of pin 16 and pin 18. Updated Packaging Information: spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F.