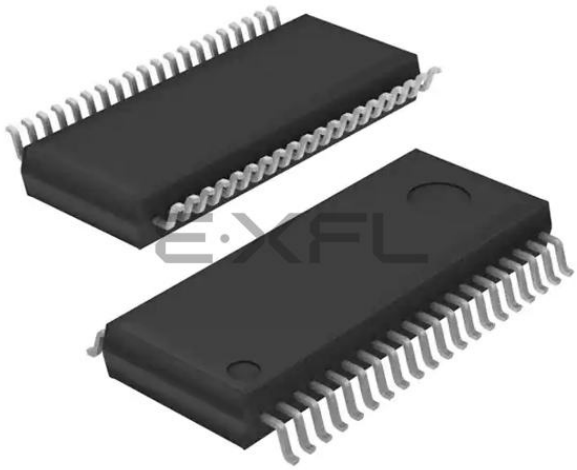

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Audio
Interface	I²C, I²S
Clock Rate	24.576MHz
Non-Volatile Memory	-
On-Chip RAM	1kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-25°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-SSOP (0.213", 5.40mm Width)
Supplier Device Package	40-SSOP-B
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/bu9409fv-e2

1-3. Control signal specification

○ Bus line, I/O stage electrical specification and timing.

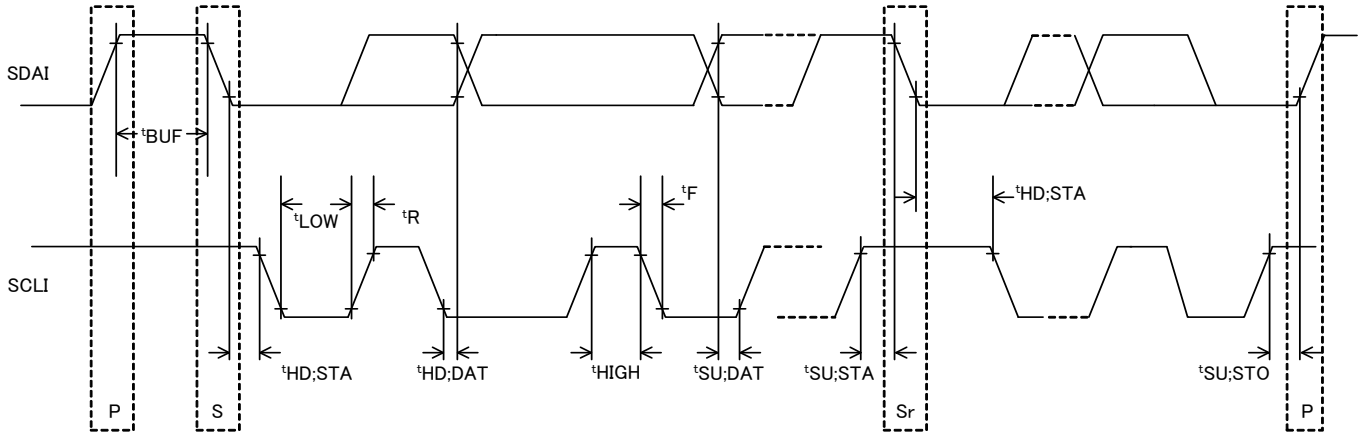


Fig.1-1: Timing chart

Table 1-1: SDAI and SCLI bus-line characteristic (Unless specified, Ta=25 , Vcc=3.3V)

Parameter		Code	High-speed mode		Unit
			Min.	Max.	
1	SCLI clock frequency	fSCL	0	400	kHz
2	Bus-free-time between "Stop" condition and "Start" condition	^{t}BUF	1.3	—	μs
3	"Start" condition of hold-time (resending). After this period, the first clock-pulse is generated.	^{t}HD;STA	0.6	—	μs
4	LOW status hold-time of SCLI clock	^{t}LOW	1.3	—	μs
5	HIGH status hold-time of SCLI clock	^{t}HIGH	0.6	—	μs
6	Setup time of resending “Start” condition	^{t}SU;STA	0.6	—	μs
7	Data-hold-time	^{t}HD;DAT	0[1)]	—	μs
8	Data-setup time	^{t}SU;DAT	500/250/150	—	ns
9	Rising time of SDAI and SCL signal	^{t}R	20+Cb	300	ns
10	Fall time of SDAI and SCL signal	^{t}F	20+Cb	300	ns
11	Setup time of "Stop" condition	^{t}SU;STO	0.6	—	μs
12	Capacitive load of each bus-line	Cb	—	400	pF

The above-mentioned numerical values are all the values corresponding to $V_{IH\ min}$ and $V_{IL\ max}$ level.

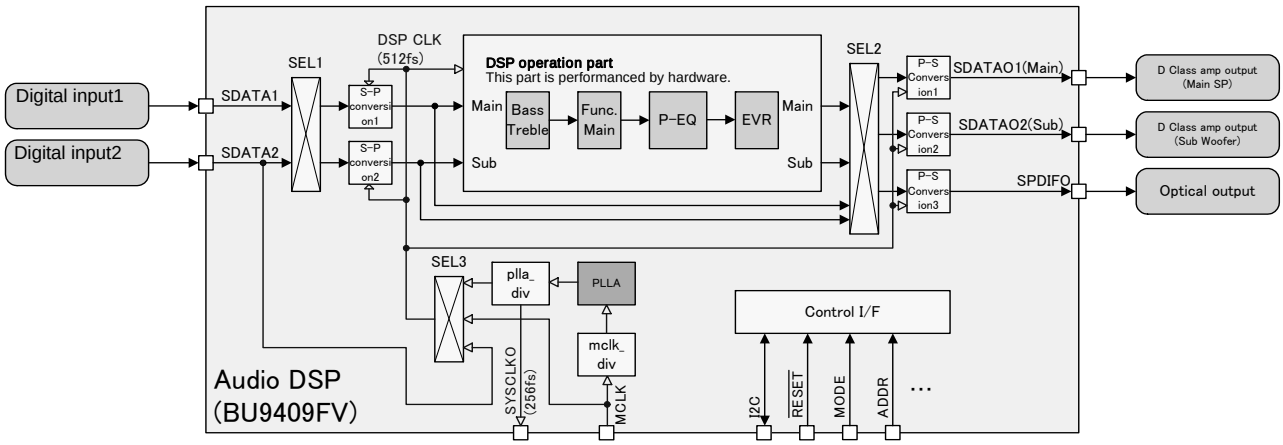
1) To exceed an undefined area on falling edged of SCLI, transmission device should internally offer the hold-time of 300ns or more for SDAI signal($V_{IH\ min}$ of SCLI signal).

2) Data-setup time changes with setup of MCLK. In MCLK=512fs, data setup time is 150ns.
In MCLK=256fs, data setup time is 250ns. In MCLK=128fs, data setup time is 500ns.

The above-mentioned characteristic is a theory value in IC design and it doesn't be guaranteed by shipment inspection.
When problem occurs by any chance, we talk in good faith and correspond.
Neither terminal SCLI nor terminal SDAI correspond to 5V tolerant. Please use it within absolute maximum rating 4.5V.

2.Switching of data and clock

I/O system chart of BU9409FV audio data is shown below.



BU9409FV has 2 digital stereo input and 3 digital stereo output with the same sampling rate.
Output from DSP operation part is converted into I^2S mode digital output or S/PDIF mode digital serial output.
System clock uses master clock input from MCLK terminal, makes 512fs multiplying clock in PLL block. Moreover, 256fs synchronous clock can be output from terminal SYSCLKO, and the clock is supplied to external DAC or D class SP amplifier.

SPDIFO and output data selection of SDATAO1 and SDATAO2 should unify the DSP processing after (post) or processing before (pre) with all outputs.

2-1. S-P conversion1 input data selection(SEL1)

Default = 0

Select Address	Value	Operating Description
&h03 [0]	0	Input data from SDATA1
	1	Input data from SDATA2

2-2. S-P conversion2 input data selection(SEL1)

Default = 0

Select Address	Value	Operating Description
&h03 [4]	0	Input data from SDATA1
	1	Input data from SDATA2

2-3. Output data selection(SEL2) to P-S conversion1 (SDATAO1 Terminal)

Default = 0

Select Address	Value	Operating Description
&h04 [1 : 0]	0	Main data output after DSP is processed.
	1	Sub data output after DSP is processed.
	2	Main data output before DSP is processed.
	3	Sub data output before DSP is processed.

3-1. Three-wire serial input's bit clock frequency setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1, S-Pconversion2 &h0B [4]	0	64fs method
	1	48fs method

3-2. Three-wire serial input's format setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1 &h0B [3 : 2]	0	IIS method
S-P conversion2 &h0C [3 : 2]	1	left-justified method
	2	right-justified method

3-3. Three-wire serial input's data bit width setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1 &h0B [1 : 0]	0	16 bit
S-P conversion2 &h0C [1 : 0]	1	20 bit
	2	24 bit

4-2. DC Cut HPF

The DC offset component of digital signal inputted to the audio DSP is cut by this HPF.
The cutoff frequency fc of HPF is 1Hz, and first-order filter is used.

Default = 0

Select Address	Value	Operational explanation
&h21 [0]	0	Not using the DC Cut HPF
	1	Using the DC Cut HPF

4-3. Channel mixer

It performs the setting of mixing the sounds of left channel & right channel of digital signal inputted to the audio DSP.
Here the stereo signal is made to be monaural.

The data inputted to Lch of DSP is mixed.

Default = 0

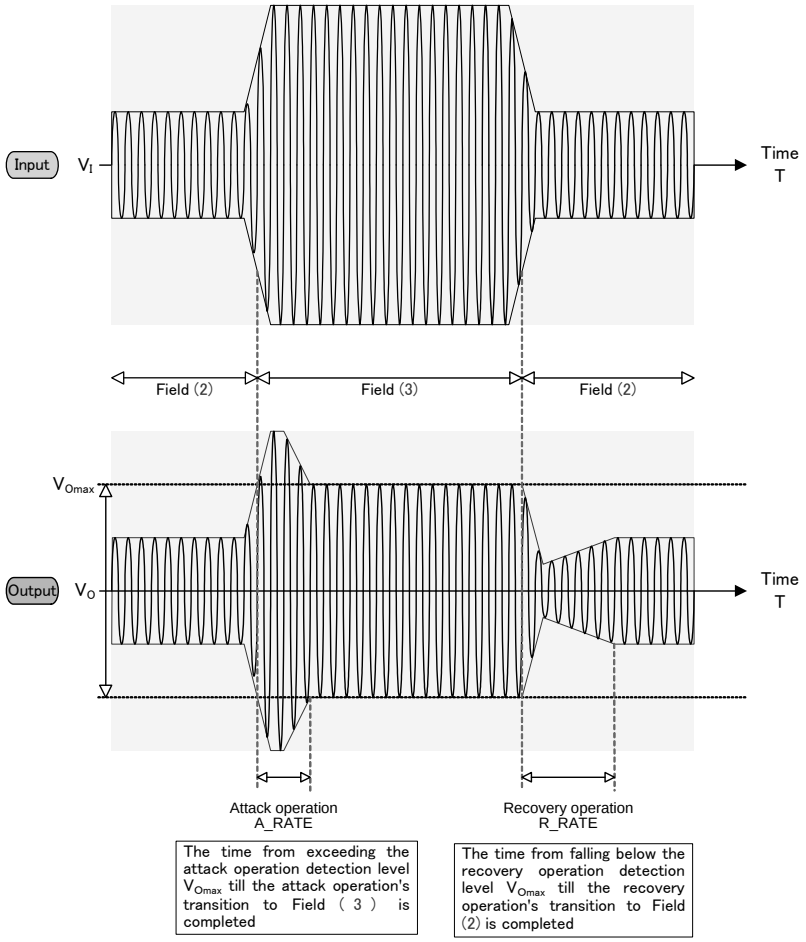
Select Address	Value	Operational explanation
&h22 [7：6]	0	Inputting the Lch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Rch data

The data inputted to Rch of DSP is mixed.

Default = 0

Select Address	Value	Operational explanation
&h22 [5：4]	0	Inputting the Rch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of（Lch + Rch） / 2
	3	Inputting the Lch data

Explanation of A_RATE,R_RATE(field transition of (2)<->(3))



Setting 1 of attack detection time

A_TIME is the setting of the initiation of P^2Volume function's transition operation. If output level at the time of transiting to (2)→(3) continues for more then A_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

Select Address	Operational explanation

command	A_TIME	command	A_TIME
0	0.5ms	4	3ms
1	1ms	5	4ms
2	1.5ms	6	5ms
3	2ms	7	6ms

&h39 [6:4]

Setting 1 of recovery detection time

R_TIME is the setting of the initiation of P^2Volume function's transition operation. If output level at the time of transiting to (3)→(2) continues for more then R_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

Select Address	Operational explanation

command	R_TIME	command	R_TIME
0	50ms	4	300ms
1	100ms	5	400ms
2	150ms	6	500ms
3	200ms	7	600ms

&h39 [2:0]

○Pulse sound detection and High-speed recovery function（functioning only at the time of transition of (2)<->(3)）

P^2Volume function makes the P^2Volume also compatible with large pulse sounds (clapping of hands, fireworks & shooting etc.) in addition to normal P^2Volume operation. When large pulse sound is inputted, attack operation (A_RATE) or recovery operation (R_RATE) is performed at 4 or 8 times the speed of normal attack operation or recovery operation.

Selection of using the pulse sound detection function.

Default = 0

Select Address	Value	Operational explanation
&h3BC[7]	0	Not using of pulse sound detection function
	1	Using of pulse sound detection function

Selection of operating times of Recovery Time (R_RATE) in the case of using the pulse sound detection function

Default = 0

Select Address	Value	Operational explanation
&h3C [3]	0	Operating at 4 times the speed corresponding to the setting time of R_RATE
	1	Operating at 8 times the speed corresponding to the setting time of R_RATE

Selection of pulse sound detection time

Default = 0

Select Address	Operational explanation
&h3C [6:4]	

Command	Detection time	Command	Detection time
0	100us	4	2ms
1	200us	5	5ms
2	400us	6	10ms
3	1ms	7	20ms

Setting of operating level of pulse sound detection function

Operation is started by the difference between the presently detected value and the last value as a standard.

Default = 0

Select Address	Operational explanation
&h3C [2:0]	

Command	Detection level	Command	Detection level
0	Over 1.002	4	Over 0.251
1	Over 0.709	5	Over 0.178
2	Over 0.502	6	Over 0.126
3	Over 0.355	7	Over 0.089

Example） Present detection level A ： -10dB → 10^(-10/20) = 0.32

The last detection level B ： -30dB → 10^(-30/20) = 0.032

A – B ： 0.32 – 0.032 = 0.288 → Operating by the setting of command ”4” to ”7”.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted directly to the coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h40 [0]	0	BASS coefficient transmission stop
	1	BASS coefficient transmission start

selection of frequency（F_0）

Default = 0Eh

Select Address	Operational explanation

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	–
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	–
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	–

Selection of quality factor （Q）

Default = 4h

Select Address	Operational explanation

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Operational explanation

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-6. MIDDLE

MIDDLE of TONE Control uses Peaking filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F, Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○MIDDLE Control

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h44 [6]	0	Using MIDDLE smooth transition function
	1	Not MIDDLE using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h44 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h44[0] command, to the coefficient RAM for smooth transition, the alteration of MIDDLE's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [1]	0	MIDDLE smooth transition stop
	1	MIDDLE smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of MIDDLE smooth transition time, from the time the MIDDLE smooth transition start （&h4C[1] = "1"） is executed until the following command is sent. Please make sure to perform the MIDDLE smooth transition stop（&h4C[1] = "0"） after the smooth transition is completed.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted to the direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h44 [0]	0	MIDDLE coefficient transmission stop
	1	MIDDLE coefficient transmission sart

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted to the direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h48 [0]	0	TREBLE coefficient transmission stop
	1	TREBLE coefficient transmission start

Selection of frequency（F_0）

Default = 0Eh

Select Address	Operational explanation

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	–
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	–
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	–

Selection of quality factor（Q）

Default = 4h

Select Address	Operational explanation

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Operational explanation

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-8. Scaler 1

Scaler adjusts the gain in order to prevent the overflow in DSP.

Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.

Scaler 1 does not incorporate the smooth transition function.

Default = 30h

Select Address	Operational explanation
&h24 [7 : 0]	Command / Gain 00 / +24dB 01 / +23.5dB ⋮ / ⋮ 30 / 0dB 31 / −0.5dB 32 / −1dB ⋮ / ⋮ FE / −103dB FF / −∞

4-9. Pseudo stereo

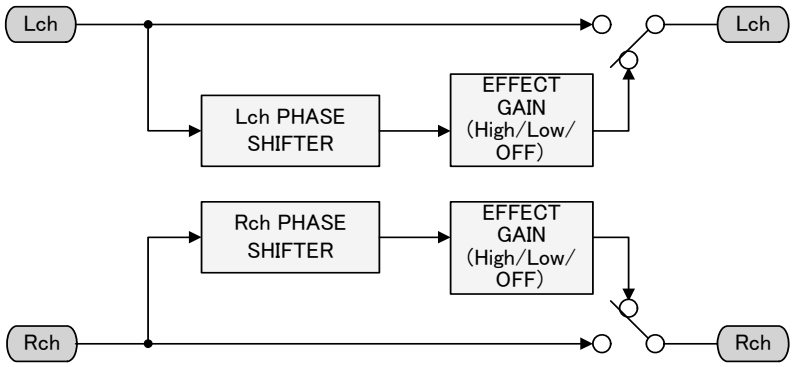
The sense of stereo is reproduced by signal processing of monaural voice.

Selection of filter effects of pseudo stereo

Default = 0

Select Address	Value	Operational explanation
&h71 [1 : 0]	0	Not using of pseudo stereo
	1	Gain is set as "high"
	2	Gain is set as "low"

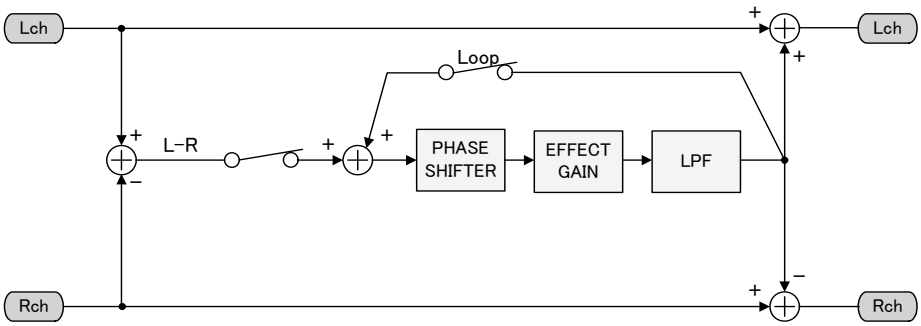
If combined with the Surround's setting of ON（&h70[7] = 1）, it will become even wider.



4-10. Surround （Matrix Surround 3D）

It realizes the Surround with little feeling of fatigue even after wide seat spot and long-time watching & listening to. It reproduces the feeling of broadening of the natural sounds in medium & high bands and realizes the sound field that do no damage to the feeling of locating of the vocal.

If loop is used, then the number of stages of phase shifter can be increased in a pseudo way.



ON/OFF of Surround function

Default = 0

Select Address	Value	Operational explanation
&h70 [7]	0	Turning the Surround effect OFF
	1	Turning the Surround effect ON

Setting of using the LOOP

Default = 0

Select Address	Value	Operational explanation
&h70 [5]	0	Not using of LOOP
	1	Using of LOOP

Setting of Surround gain

Default = Fh

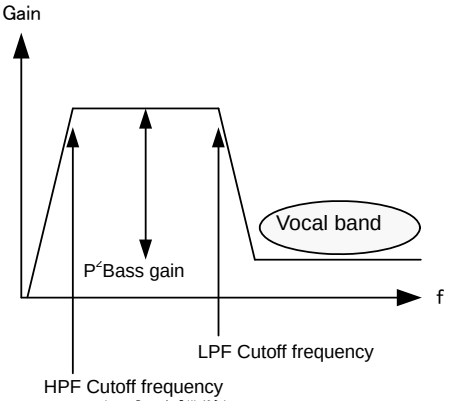
Select Address	Operational explanation

Command	Gain	Command	Gain
0	0dB	8	−8dB
1	−1dB	9	−9dB
2	−2dB	A	−10dB
3	−3dB	B	−11dB
4	−4dB	C	−12dB
5	−5dB	D	−13dB
6	−6dB	E	−14dB
7	−7dB	F	−15dB

4-11. P^{2}Bass （Perfect Pure Bass： Deep Bass Equalizer）

It is the deep bass equalizer making it possible that even thin-screen TV, by which the enclosure of speaker is restricted, can reproduce the real sound close to powerful deep bass & original sound.

Solid & clear deep bass with little feeling of distortion is realized. Even boosting of bass does not interfere with vocal band, therefore rich and natural deep band is realized.



ON/OFF of P^{2}Bass function

Default = 0

Select Address	Value	Operational explanation
&h73 [7]	0	Not using of P^{2}Bass function
	1	Using of P^{2}Bass function

Setting of P^{2}Bass smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h73 [3：2]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

P^{2}Bass smooth transition control

Default = 0

Select Address	Value	Operational explanation
&h77 [1：0]	0	P^{2}Bass smooth transition stop
	1	Setting of the values into Coefficient RAM for P^{2}Bass smooth transition
	2	P^{2}Bass smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of P^{2}Bass smooth transition time, from the time the P^{2}Bass smooth transition start（&h77[1:0] = “2”） is executed until the following command is sent. Please make sure to perform the P^{2}Bass smooth transition stop（&h77[1:0] = “0”） after the smooth transition is completed.

4-13. Scaler 2

Scaler adjusts the gain in order to prevent the overflow in DSP.

Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.

Scaler 2 does not incorporate the smooth transition function.

Default = 30h

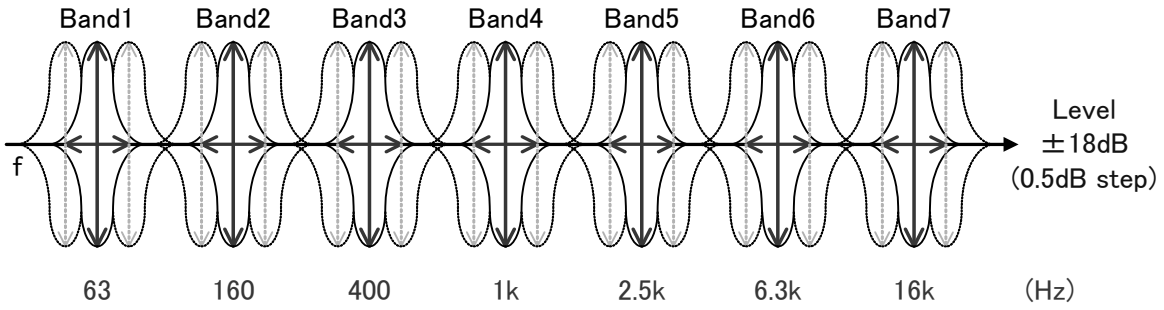
Select Address	Operational explanation
&h25 [7 : 0]	See table below

Command	Gain
00	+24dB
01	+23.5dB
⋮	⋮
30	0dB
31	−0.5dB
32	−1dB
⋮	⋮
FE	−103dB
FF	−∞

4-14. 7 band・parametric equalizer

7-band parametric equalizer can use Peaking filter, Low-shelf filter or high-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F, Q and Gain, and transmitted to coefficient RAM. There is no smooth transition function.



Selection of filter types

Default = 0

Select Address	Value	Operational explanation
bit[7:6] It sets to all band	0	Peaking filter
	1	Low-shelf filter
	2	High-shelf filter

Setting of the Start of transmitting to coefficient RAM

It is transmitted to direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
bit [0] It sets to all band	0	Coefficient transmission stop
	1	Coefficient transmission start

4-20. Sub output channel mixer

Mixing setting of sound of the left channel and the right channel of the digital signal for sub output which is input into sound DSP is done. The monaural conversion of the stereo signal is done here.

The data which is input into Lch of Sub output signal processing is mixed.

Default = 0

Select Address	Value	Operating explanation
&h22 [3 : 2]	0	Inputting the Lch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Rch data

The data which is input into Rch of Sub output signal processing is mixed.

Default = 0

Select Address	Value	Operating explanation
&h22 [1 : 0]	0	Inputting the Rch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Lch data

4-21. LPF for sub woofer output

It is the crossover filter (LPF) for sub woofer output.
LPF function ON/OFF.

Default = 0

Select Address	Value	Operating explanation
&h7A [7]	0	LPF function is not used
	1	LPF function is used

Setting of the cut off frequency (Fc) of LPF

Default = 0h

Select Address	Operating explanation
&h7A [6 : 4]	See table below

Command	Fc	Command	Fc
0	60Hz	4	160Hz
1	80Hz	5	200Hz
2	100Hz	6	240Hz
3	120Hz	7	280Hz

4-28. About the automatic renewal of five coefficients of b0, b1, b2, a1 and a2 of Bi-quad Filter

BASS, MIDDLE, TREBLE, main output 7 bands Parametric Equalizer and sub output 3 band Parametric Equalizer have used coefficient RAM. As for this coefficient RAM, because direct access is not possible from the micro-computer, it cannot refresh the register efficiently.

There is an automatic renewal function of coefficient RAM in this DSP, the automatic write-in renewal of coefficient RAM is possible by using this function. However when 4-26 「the function of direct setting a coefficient RAM」 is utilized, it is not possible to utilize automatic write-in renewal.

Selection of using the automatic write-in renewal function

Default = 0

Select Address	Value	Operating explanation
&h6D [0]	0	Automatic write-in renewal function is used
	1	Automatic write-in renewal function is not used

The separate setting of Filter of automatic write-in renewal function

Default = 00h

Select Address	Filter	Operating explanation
&h6E [0]	BASS	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [1]	MIDDLE	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [2]	TREBLE	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [4]	Sub BAND1	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [5]	Sub BAND2	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [6]	Sub BAND3	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [0]	Main MAND1	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [1]	Main MAND2	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [2]	Main MAND3	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [3]	Main MAND4	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [4]	Main MAND5	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [5]	Main MAND6	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [6]	Main MAND7	0：Automatic renewal function OFF 1：Automatic renewal function ON

5. P-S conversion 1 ,P-S conversion 2

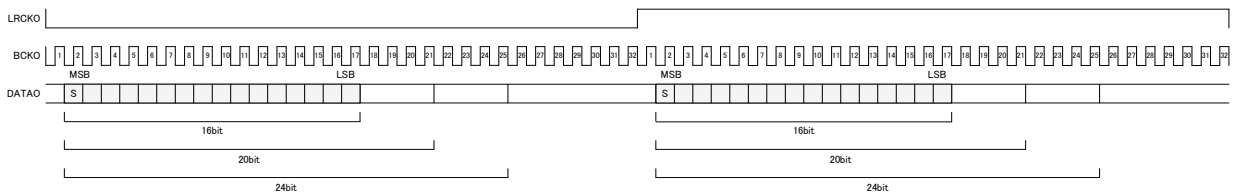
Two parallel serial conversion circuits are built in BU9409FV. (P-S conversion 1, P-S conversion 2)

P-S conversion 1 convert the Main output of DSP from SDATAO1, LRCKO, and BCKO (34,35,36pin) into three line serial data and output the data.

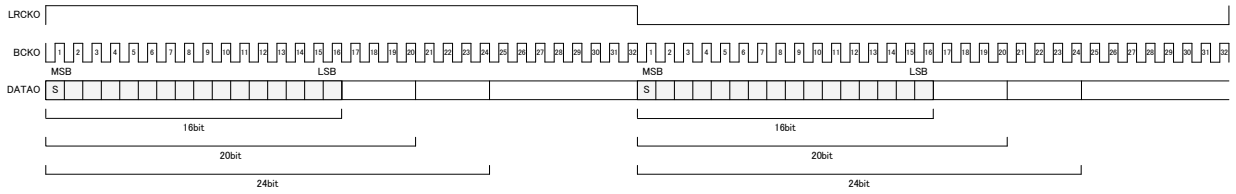
P-S conversion 2 convert the sub output of DSP from SDATAO1, LRCKO, and BCKO (33,35,36pin) into three line serial data and output the data.

Output format has the IIS mode, left-align mode, and right-align mode. 16 each bit, 20bit, and 24bit output can also be selected. The figure below shows the timing chart of each transmission mode.

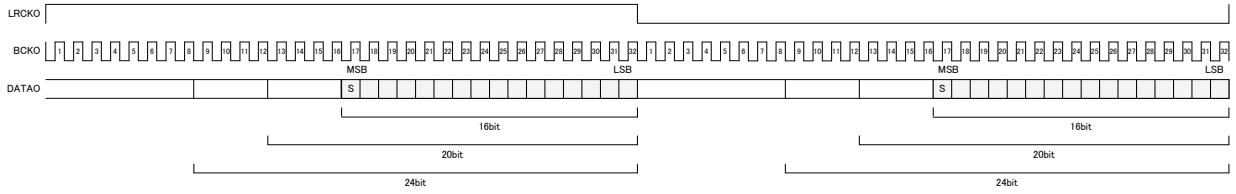
IIS mode



left-align mode



right-align mode



5-1. Format setting of three line serial output

Default = 0

Select Address	Value	Operating Description
P-S conversion 1 &h0D [3 : 2] P-S conversion 2 & h0E [3 : 2]	0	IIS mode
	1	left-align mode
	2	right-align mode

5-2. Setting data bit width of three line serial output

Default = 0

Select Address	Value	Operating Description
P-S conversion 1 &h0D [1 : 0] P-S conversion 2 & h0E [1 : 0]	0	16 bit
	1	20 bit
	2	24 bit

11-3. When the frequency more than a stop or the specification range does not enter [MCLK] at the time of a sampling rate change

When switching a sampling rate, the clock of the frequency more than the specification range does not go into MCLK, but when input data is 0, it can return with the following procedures.

1. Carry out the mute of the DAC (MUTEX_SP and MUTEX_DAC are set to L and it is a mute about BD5446.)

↓

○When the input of MCLK has stopped, please do not input a command until MCLK is inputted again.
Please perform the following setup, after MCLK is inputted on the frequency of specification within the limits.

↓

2. It is 20ms or more WAIT because of PLL stability.

↓

○When the section where MCLK stopped or the relation with I2S input had collapsed in the midst of the midst of soft transition and transmission of a coefficient exists, the coefficient may not be able to be transmitted well. When soft transition and a coefficient are transmitting, please perform a setup from 11-2 4.
Please perform the following setup, when you are not the midst of soft transition or transmission of a coefficient.

↓

3. Please cancel a DAC mute.

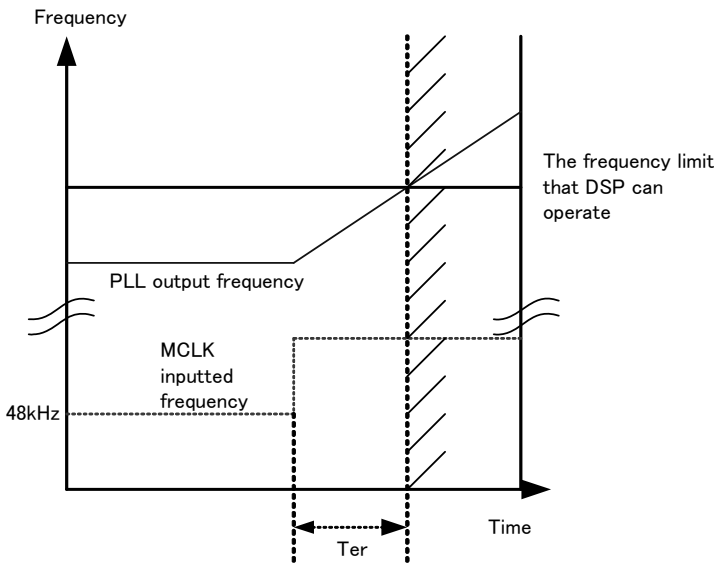
12. When the clock which exceeded the specification range from MCLK is inputted

When the frequency beyond fs=48kHz is inputted from MCLK in the state where it was set as &h08 [5:4] =1, since PLL follows inputted MCLK, as shown in the right figure, when it exceeds Time Ter, it will exceed the frequency in which DSP can operate.

In this case, an allophone may carry out irrespective of the existence of data.

When you change into such a state, please carry out the mute of the DAC immediately, apply reset (RESETB=L), and do the work after reset release of Chapter 8.

The time of Ter serves as about 70 usec.



14. Notes at the Time of Reset

Since the state of IC is not decided, please make it into RESETX=L at the time of a power supply injection, and surely apply reset.

Reset of BU9409FV is performing noise removal by MCLK.

Therefore, in order to apply reset, a MCLK clock pulse is required of the state of RESETX=L more than 10 times.

The power-on reset after a power supply injection, and when you usually apply reset at the time of operation, please be sure to carry out in the state where the clock is inputted, from MCLK.

15. Read-out of Soft Transition Flag

It is set to &hF4[0] =H when BASS, MIDDLE, TREBLE or P2Bass, and P2Treble are soft transiting.

It is possible to check whether soft transition is completed by reading &hF4 [0]

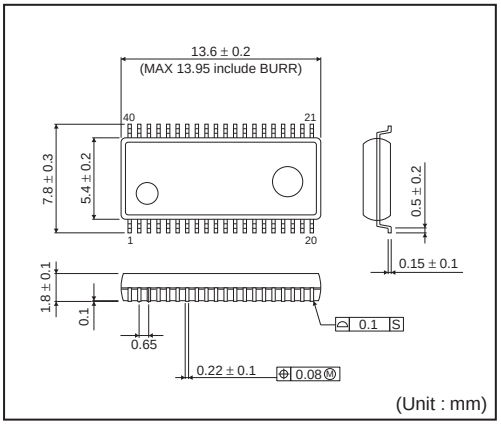
Soft transition will be completed if the read-out result of &hF4 [0] is L.

●Ordering Information

B U 9 4 0 9 F V	E2
Part Number	Package FV: SSO-B40
	Packaging and forming specification E2: Embossed tape and reel

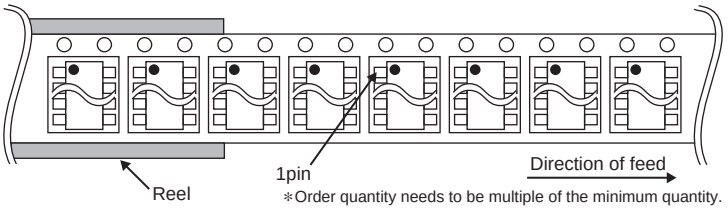
●Physical Dimension Tape and Reel Information

SSOP-B40



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram(s)(TOP VIEW)