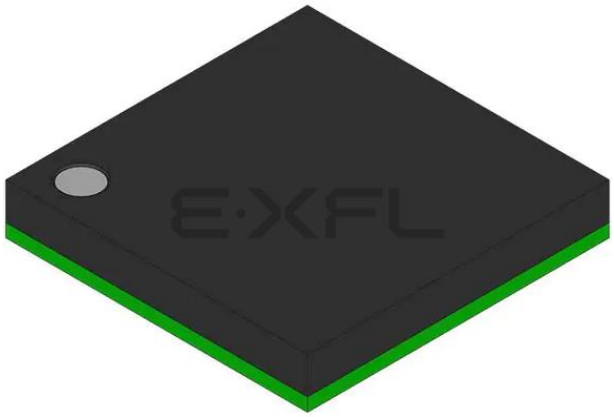

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 86 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3V |
| Data Converters | A/D 2x16b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-LFBGA |
| Supplier Device Package | 121-MAPBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk60dn512zvmc10 |

- Communication interfaces
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital host controller (SDHC)
  - I2S module

### 3.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/ pulldown current | 10 | 130 | µA |

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

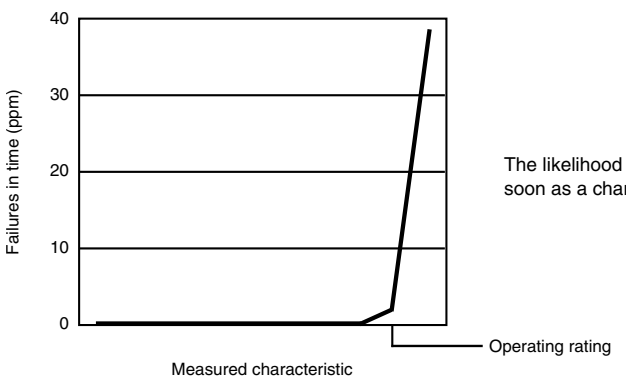
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 5.2.2 LVD and POR operating requirements

### Table 2. $V_{DD}$ supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±80 | — | mV | |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±60 | — | mV | |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| $t_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising thresholds are falling threshold + hysteresis voltage

### Table 3. VBAT power operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR\_VBAT}$ | Falling VBAT supply POR detect voltage | 0.8 | 1.1 | 1.5 | V | |

## 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — high drive strength | | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -9mA | $V_{DD}$ – 0.5 | — | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -3mA | $V_{DD}$ – 0.5 | — | — | V | |
| | Output high voltage — low drive strength | | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -2mA | $V_{DD}$ – 0.5 | — | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -0.6mA | $V_{DD}$ – 0.5 | — | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength | | | | | 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 9mA | — | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 3mA | — | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 2mA | — | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 0.6mA | — | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | — | 100 | mA | |
| $I_{INA}$ | Input leakage current, analog pins and digital pins configured as analog inputs | | | | | 3, 4 |
| | • $V_{SS}$ ≤ $V_{IN}$ ≤ $V_{DD}$ | | | | | |
| | — All pins except EXTAL32, XTAL32, EXTAL, XTAL | — | 0.002 | 0.5 | µA | |
| | — EXTAL (PTA18) and XTAL (PTA19) | — | 0.004 | 1.5 | µA | |
| | — EXTAL32, XTAL32 | — | 0.075 | 10 | µA | |
| $I_{IND}$ | Input leakage current, digital pins | | | | | 4, 5 |
| | • $V_{SS}$ ≤ $V_{IN}$ ≤ $V_{IL}$ | | | | | |
| | — All digital pins | — | 0.002 | 0.5 | µA | |
| | • $V_{IN}$ = $V_{DD}$ | | | | | |
| | — All digital pins except PTD7 | — | 0.002 | 0.5 | µA | |
| | — PTD7 | — | 0.004 | 1 | µA | |
| $I_{IND}$ | Input leakage current, digital pins | | | | | 4, 5, 6 |
| | • $V_{IL}$ < $V_{IN}$ < $V_{DD}$ | | | | | |
| | — $V_{DD}$ = 3.6 V | — | 18 | 26 | µA | |
| | — $V_{DD}$ = 3.0 V | — | 12 | 49 | µA | |
| | — $V_{DD}$ = 2.5 V | — | 8 | 13 | µA | |
| | — $V_{DD}$ = 1.7 V | — | 3 | 6 | µA | |

*Table continues on the next page...*

## Table 6. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | N/A | — | mA | 7 |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | — | N/A | — | mA | 8 |
| $I_{DD\_STOP}$ | Stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.59 | 1.4 | mA | |
| | • @ 70°C | — | 2.26 | 7.9 | mA | |
| | • @ 105°C | — | 5.94 | 19.2 | mA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 93 | 435 | µA | |
| | • @ 70°C | — | 520 | 2000 | µA | |
| | • @ 105°C | — | 1350 | 4000 | µA | |
| $I_{DD\_LLS}$ | Low leakage stop mode current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 4.8 | 20 | µA | |
| | • @ 70°C | — | 28 | 68 | µA | |
| | • @ 105°C | — | 126 | 270 | µA | |
| $I_{DD\_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 3.1 | 8.9 | µA | |
| | • @ 70°C | — | 17 | 35 | µA | |
| | • @ 105°C | — | 82 | 148 | µA | |
| $I_{DD\_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 2.2 | 5.4 | µA | |
| | • @ 70°C | — | 7.1 | 12.5 | µA | |
| | • @ 105°C | — | 41 | 125 | µA | |
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 2.1 | 7.6 | µA | |
| | • @ 70°C | — | 6.2 | 13.5 | µA | |
| | • @ 105°C | — | 30 | 46 | µA | |
| $I_{DD\_VBAT}$ | Average current with RTC and 32kHz disabled at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.33 | 0.39 | µA | |
| | • @ 70°C | — | 0.60 | 0.78 | µA | |
| | • @ 105°C | — | 1.97 | 2.9 | µA | |

*Table continues on the next page...*

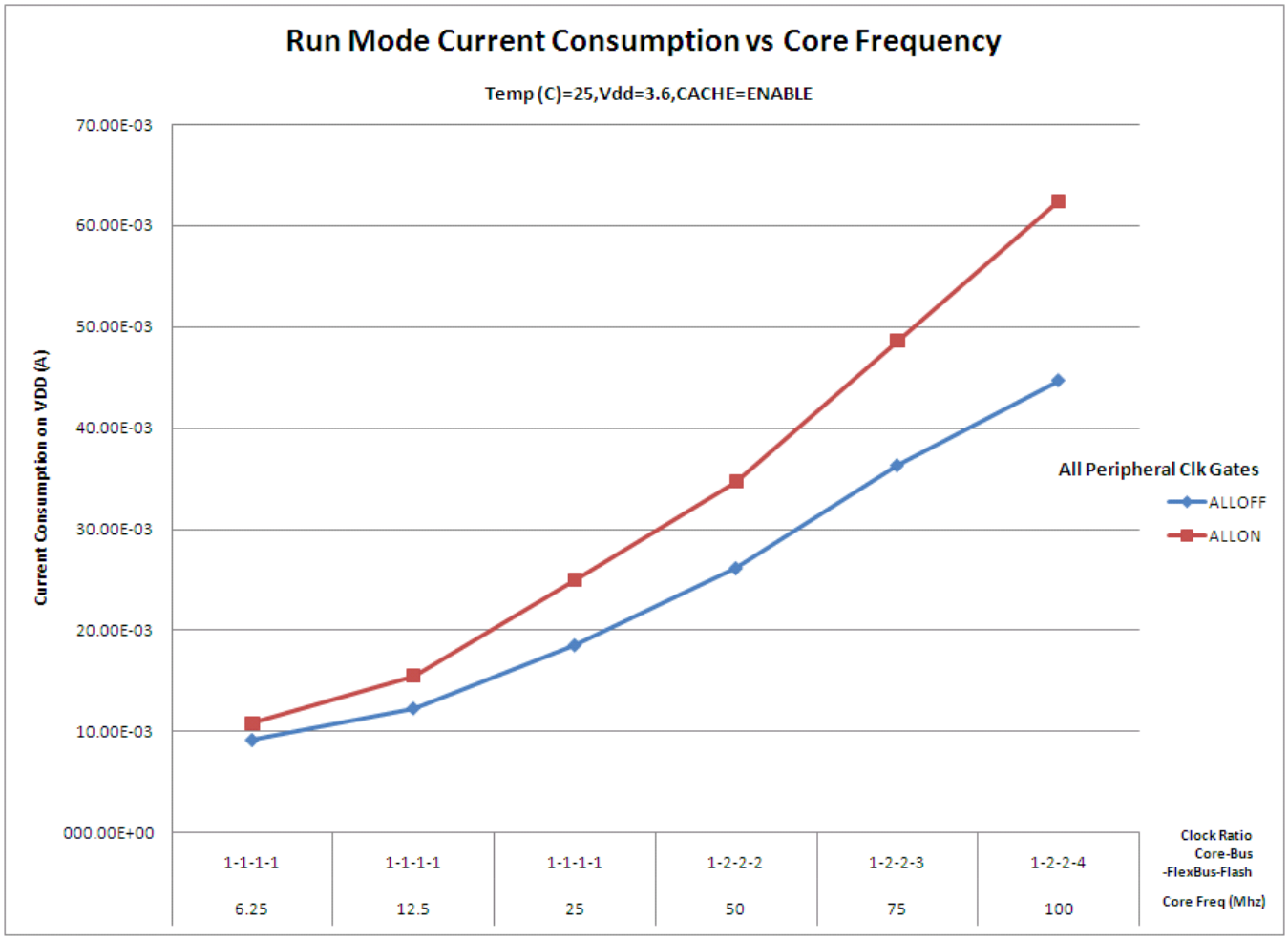



**Figure 2. Run mode supply current vs. core frequency**

## 5.2.6 EMC radiated emissions operating behaviors

**Table 7. EMC radiated emissions operating behaviors as measured on 144LQFP and 144MAPBGA packages**

| Symbol | Description | Frequency band (MHz) | 144LQFP | 144MAPBGA | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{RE1}$ | Radiated emissions voltage, band 1 | 0.15–50 | 23 | 12 | dBµV | 1 , 2 |
| $V_{RE2}$ | Radiated emissions voltage, band 2 | 50–150 | 27 | 24 | dBµV | |
| $V_{RE3}$ | Radiated emissions voltage, band 3 | 150–500 | 28 | 27 | dBµV | |
| $V_{RE4}$ | Radiated emissions voltage, band 4 | 500–1000 | 14 | 11 | dBµV | |
| $V_{RE\_IEC}$ | IEC level | 0.15–1000 | K | K | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

## 6.3.1 MCG specifications

### Table 15. MCG specifications

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed — over fixed voltage and temperature range of 0–70°C | | 31.25 | — | 38.2 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | | — | ± 4.5 | — | $\%f_{dco}$ | 1 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | | — | 4 | — | MHz | |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) 640 × $f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 2, 3 |
| | | Mid range (DRS=01) 1280 × $f_{fll\_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) 1920 × $f_{fll\_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) 2560 × $f_{fll\_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS=00) 732 × $f_{fll\_ref}$ | — | 23.99 | — | MHz | 4, 5 |
| | | Mid range (DRS=01) 1464 × $f_{fll\_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) 2197 × $f_{fll\_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) 2929 × $f_{fll\_ref}$ | — | 95.98 | — | MHz | |
| $J_{cyc\_fll}$ | FLL period jitter<br>• $f_{VCO}$ = 48 MHz<br>• $f_{VCO}$ = 98 MHz | | —<br>— | 180<br>150 | —<br>— | ps | |
| $t_{fll\_acquire}$ | FLL target frequency acquisition time | | — | — | 1 | ms | 6 |

*Table continues on the next page...*

**Table 15. MCG specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | PLL | | | | | |
| $f_{vco}$ | VCO operating frequency | 48.0 | — | 100 | MHz | |
| $I_{pll}$ | PLL operating current<br>• PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 48) | — | 1060 | — | µA | 7 |
| $I_{pll}$ | PLL operating current<br>• PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 24) | — | 600 | — | µA | 7 |
| $f_{pll\_ref}$ | PLL reference frequency range | 2.0 | — | 4.0 | MHz | |
| $J_{cyc\_pll}$ | PLL period jitter (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | <br>—<br>— | <br>120<br>50 | <br>—<br>— | <br>ps<br>ps | 8 |
| $J_{acc\_pll}$ | PLL accumulated jitter over 1µs (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | <br>—<br>— | <br>1350<br>600 | <br>—<br>— | <br>ps<br>ps | 8 |
| $D_{lock}$ | Lock entry frequency tolerance | ± 1.49 | — | ± 2.98 | % | |
| $D_{unl}$ | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | |
| $t_{pll\_lock}$ | Lock detector detection time | — | — | $150 \times 10^{-6} + 1075(1/f_{pll\_ref})$ | s | 9 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

**Table 16. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |

*Table continues on the next page...*

**Table 16. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

## 6.3.2.2 Oscillator frequency specifications

**Table 17. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

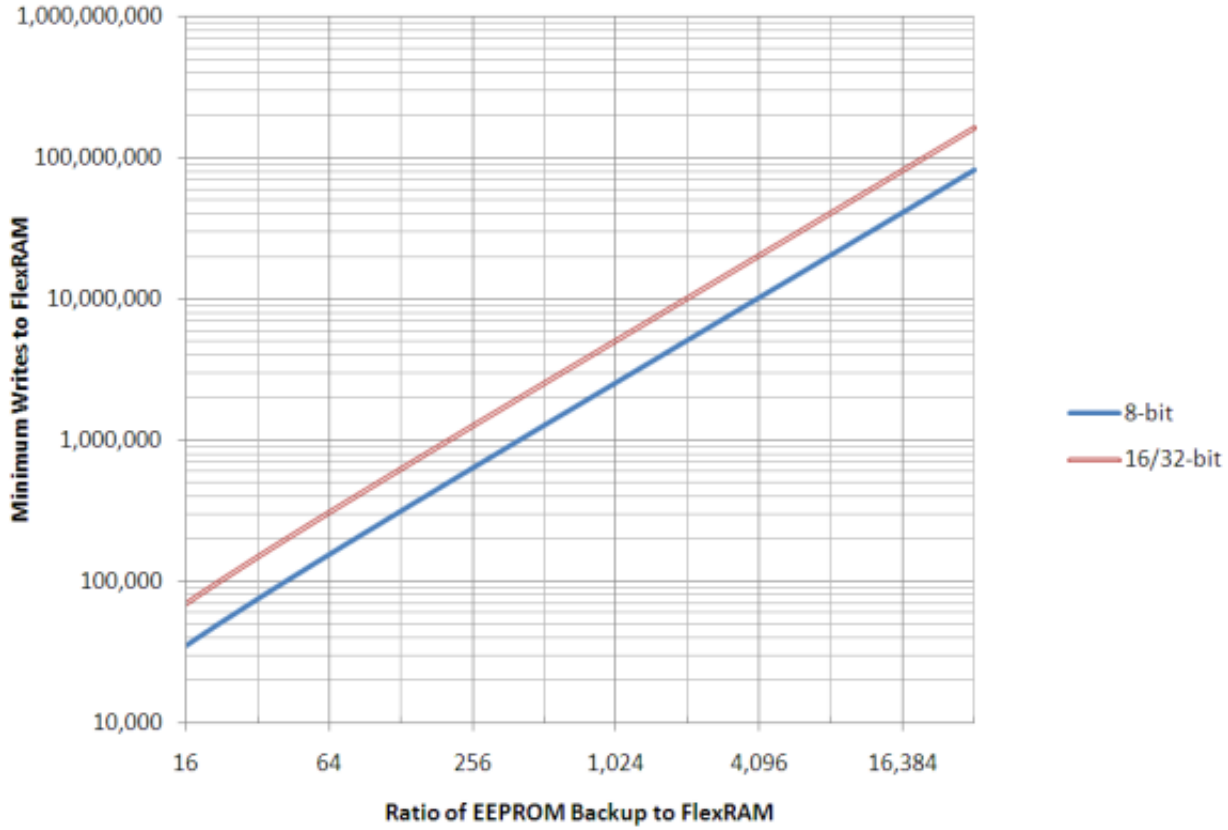



**Figure 9. EEPROM backup writes to FlexRAM**

## 6.4.2 EzPort Switching Specifications

**Table 24. EzPort switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{SYS}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{SYS}/8$ | MHz |
| EP2 | $\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion | 2 x $t_{EZP\_CK}$ | — | ns |
| EP3 | $\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup) | 5 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold) | 5 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 2 | — | ns |
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 5 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid | — | 16 | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0 | — | ns |
| EP9 | $\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

2. Specification is valid for all FB_AD[31:0] and FB_TA.

## Table 26. Flexbus full voltage range switching specifications

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 1/FB_CLK | — | ns | |
| FB2 | Address, data, and control output valid | — | 13.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0 | — | ns | 1 |
| FB4 | Data and FB_TA input setup | 13.7 | — | ns | 2 |
| FB5 | Data and FB_TA input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

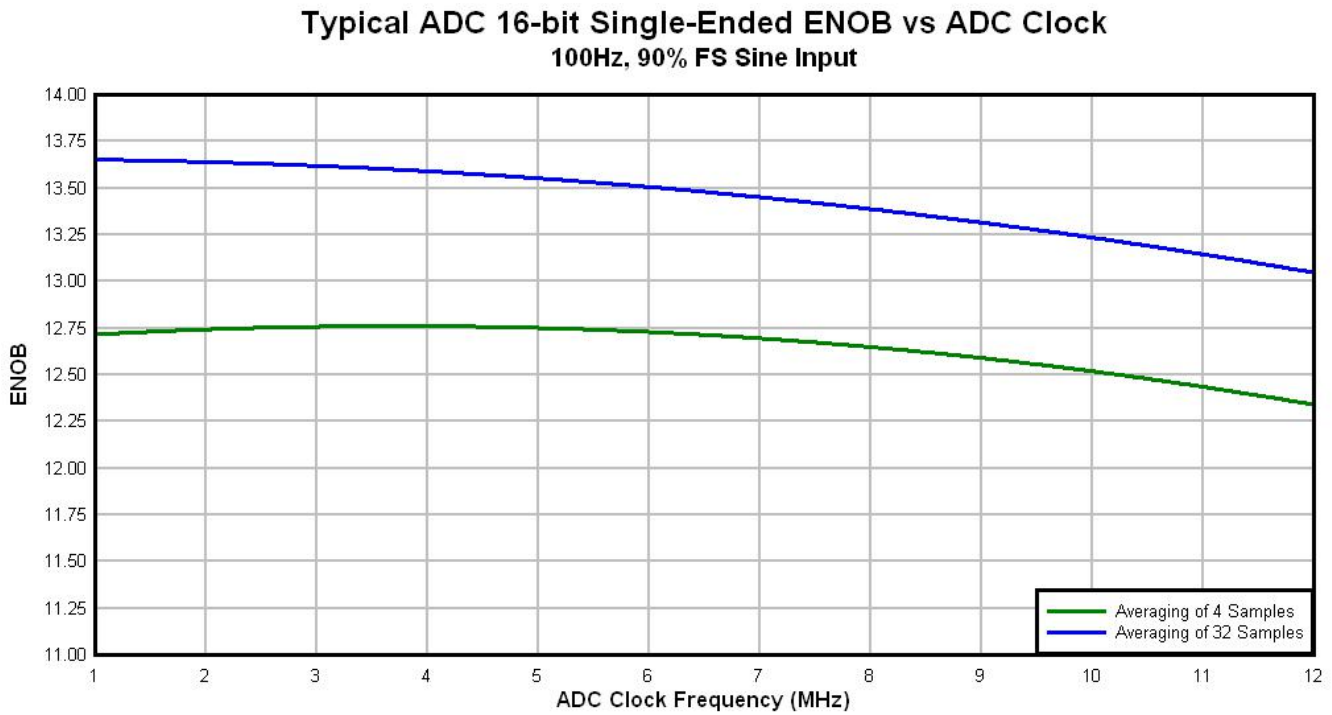



**Figure 15. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 29. 16-bit ADC with PGA operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $V_{REFPGA}$ | PGA ref voltage | | VREF_OUT | VREF_OUT | VREF_OUT | V | 2, 3 |
| $V_{ADIN}$ | Input voltage | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $V_{CM}$ | Input Common Mode range | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $R_{PGAD}$ | Differential input impedance | Gain = 1, 2, 4, 8 | — | 128 | — | kΩ | IN+ to IN-[4] |
| | | Gain = 16, 32 | — | 64 | — | | |
| | | Gain = 64 | — | 32 | — | | |
| $R_{AS}$ | Analog source resistance | | — | 100 | — | Ω | 5 |
| $T_S$ | ADC sampling time | | 1.25 | — | — | μs | 6 |

*Table continues on the next page...*

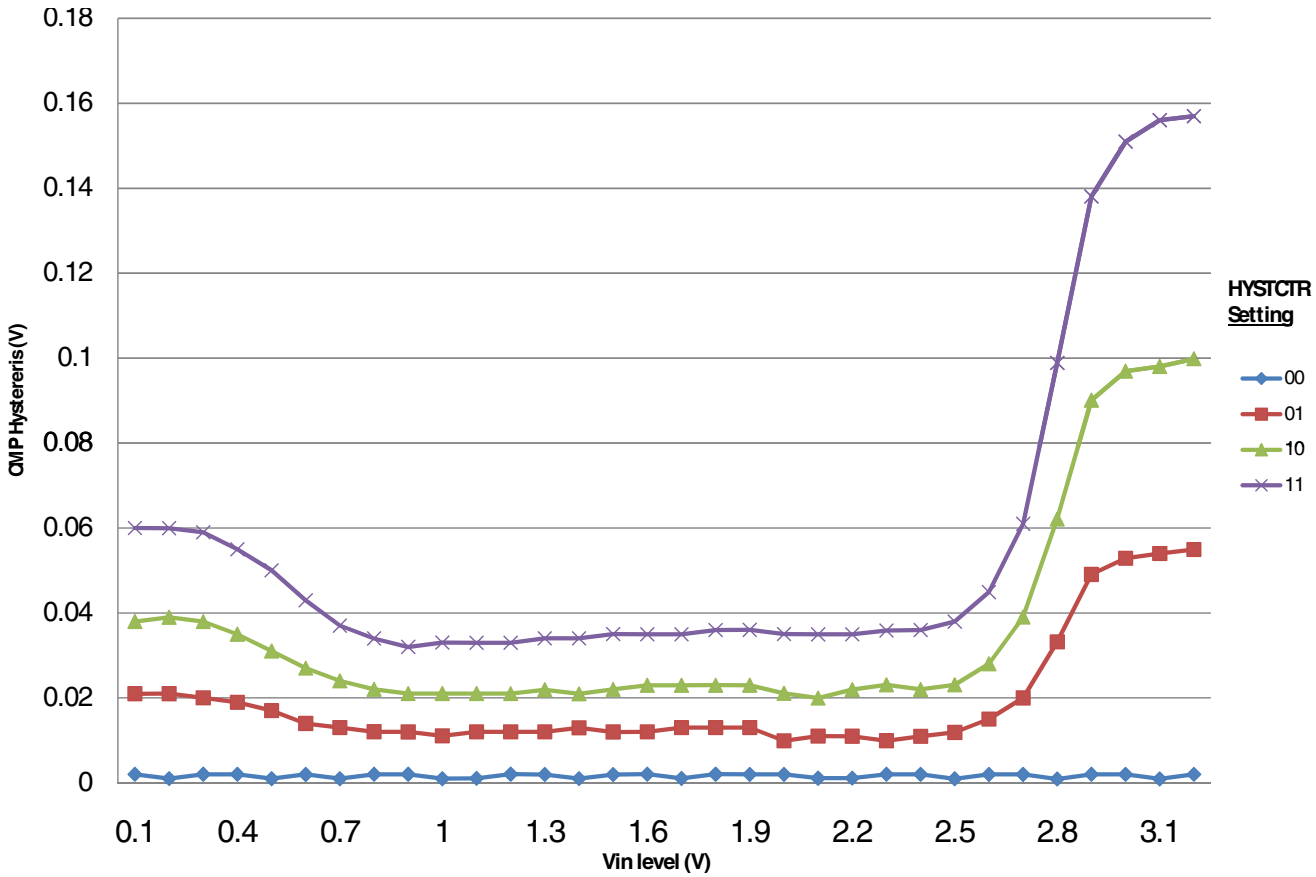



**Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)**

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

**Table 32. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

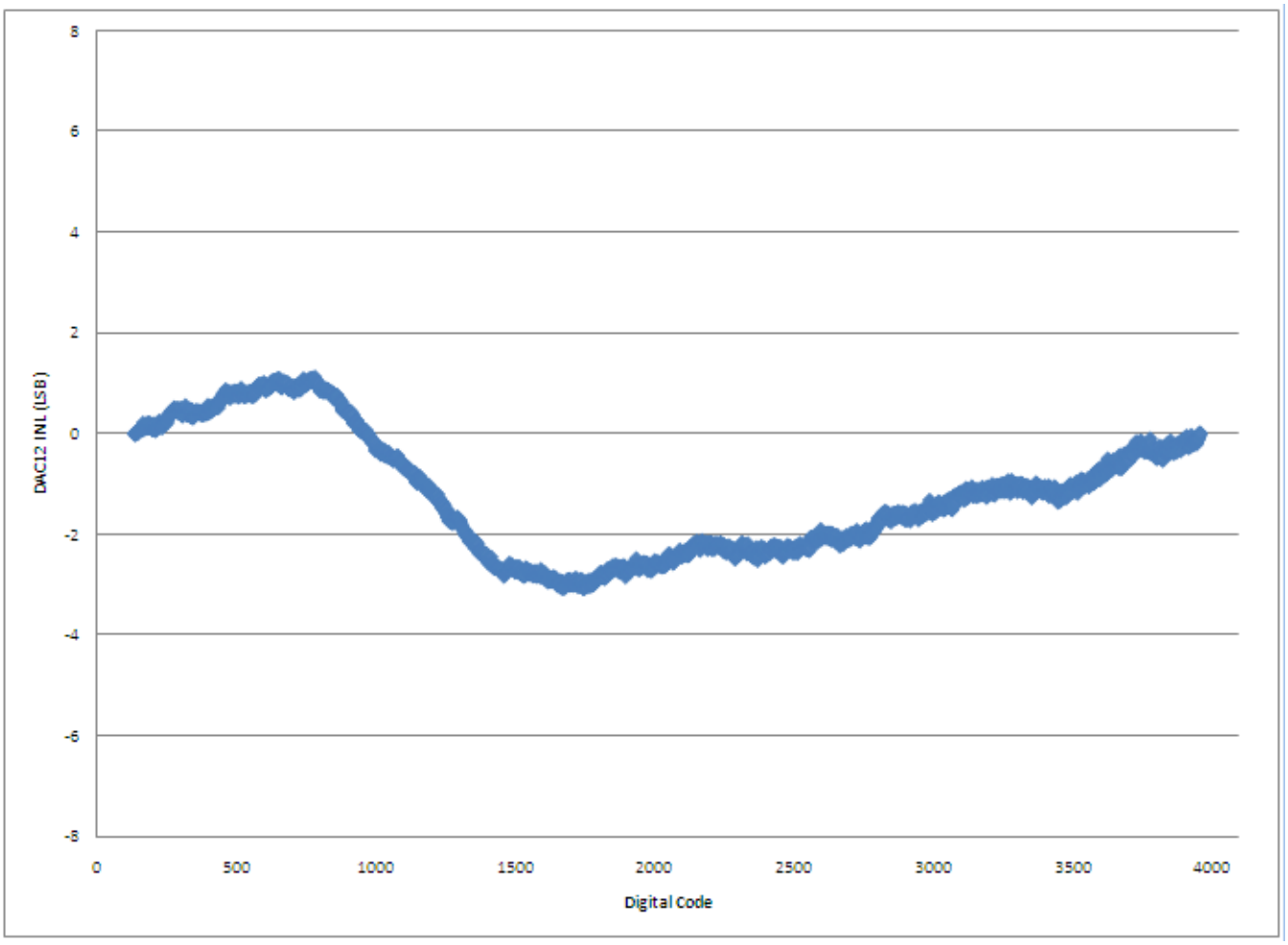



**Figure 18. Typical INL error vs. digital code**

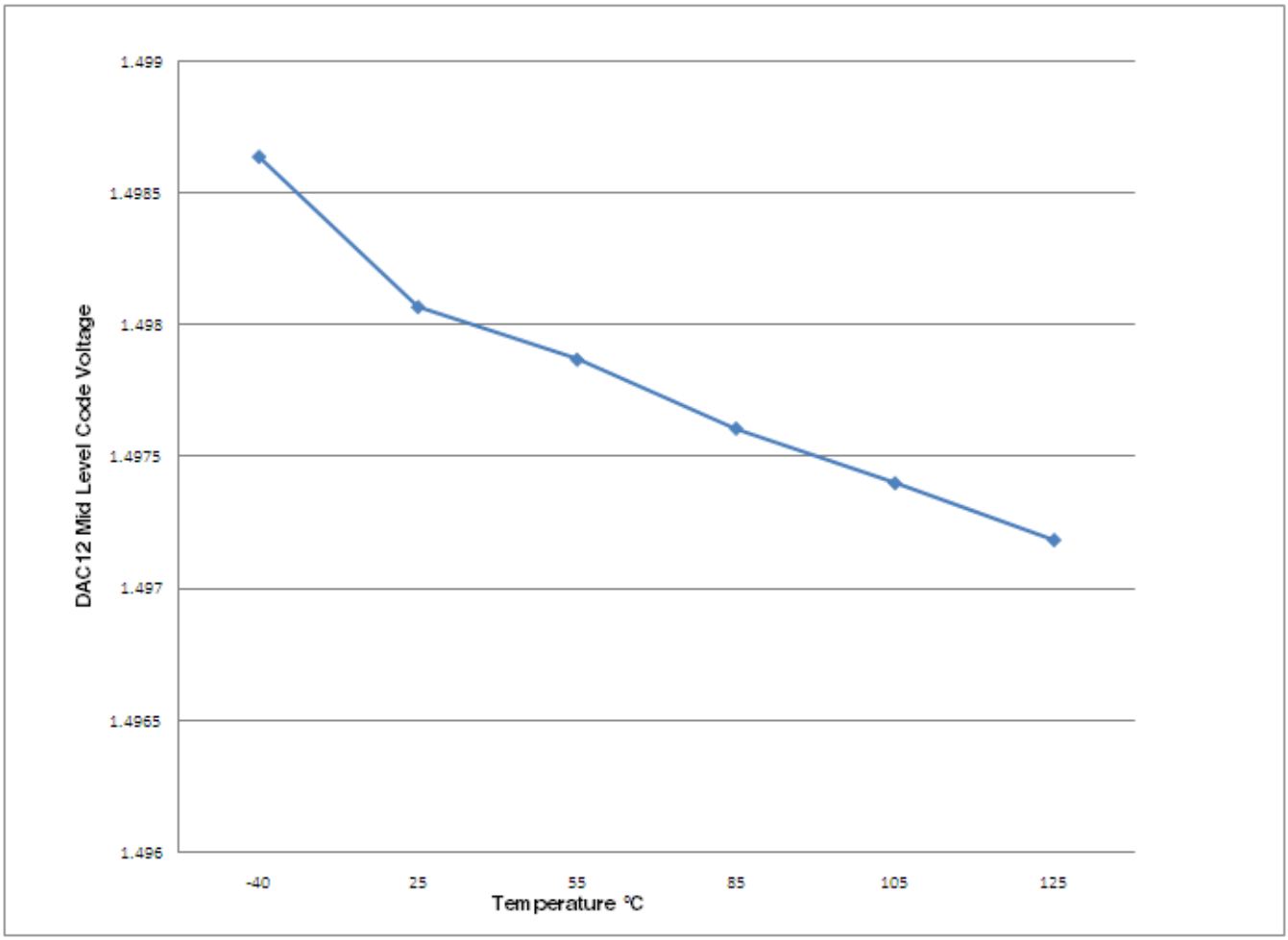



**Figure 19. Offset at half scale vs. temperature**

## 6.6.4 Voltage reference electrical specifications

**Table 34. VREF full-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | 100 | | nF | 1, 2 |

1. $C_L$ must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified $C_L$ value over the operating temperature range of the device.

**Table 43. Slave mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | | 12.5 | MHz |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven | — | 14 | ns |
| DS16 | $\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven | — | 14 | ns |

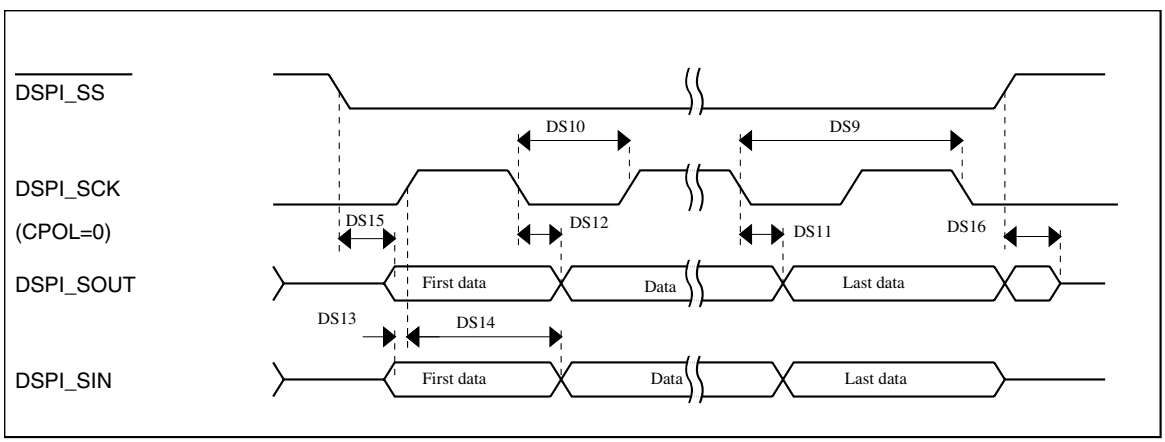



**Figure 23. DSPI classic SPI timing — slave mode**

## 6.8.7 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 44. Master mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 12.5 | MHz | |
| DS1 | DSPI_SCK output cycle time | 4 x $t_{BUS}$ | — | ns | |

*Table continues on the next page...*

6. $C_b$ = total capacitance of the one bus line in pF.

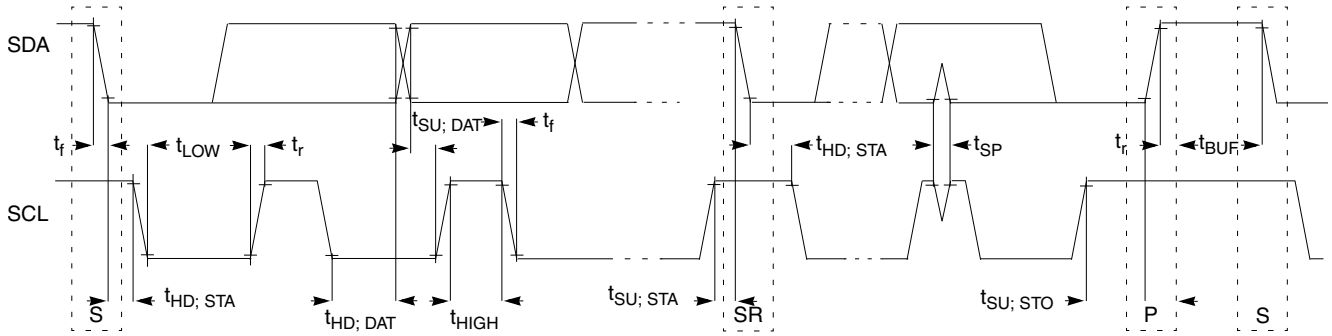



**Figure 26. Timing definition for fast and standard mode devices on the I²C bus**

## 6.8.9 UART switching specifications

See General switching specifications.

## 6.8.10 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

**Table 47. SDHC switching specifications**

| Num | Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|---|
| | **Card input clock** | | | | |
| SD1 | fpp | Clock frequency (low speed) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed\high speed) | 0 | 25\50 | MHz |
| | fpp | Clock frequency (MMC full speed\high speed) | 0 | 20\50 | MHz |
| | $f_{OD}$ | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | $t_{WL}$ | Clock low time | 7 | — | ns |
| SD3 | $t_{WH}$ | Clock high time | 7 | — | ns |
| SD4 | $t_{TLH}$ | Clock rise time | — | 3 | ns |
| SD5 | $t_{THL}$ | Clock fall time | — | 3 | ns |
| | **SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | | |
| SD6 | $t_{OD}$ | SDHC output delay (output valid) | -5 | 8.3 | ns |
| | **SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | | |
| SD7 | $t_{ISU}$ | SDHC input setup time | 5 | — | ns |
| SD8 | $t_{IH}$ | SDHC input hold time | 0 | — | ns |

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 121-pin MAPBGA | 98ASA00344D |

# 8 Pinout

## 8.1 K60 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 121 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|
| E4 | PTE0 | ADC1_SE4a | ADC1_SE4a | PTE0 | SPI1_PCS1 | UART1_TX | SDHC0_D1 | | I2C1_SDA | | |
| E3 | PTE1/ LLWU_P0 | ADC1_SE5a | ADC1_SE5a | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | SDHC0_D0 | | I2C1_SCL | | |
| E2 | PTE2/ LLWU_P1 | ADC1_SE6a | ADC1_SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_CTS_b | SDHC0_DCLK | | | | |
| F4 | PTE3 | ADC1_SE7a | ADC1_SE7a | PTE3 | SPI1_SIN | UART1_RTS_b | SDHC0_CMD | | | | |
| E7 | VDD | VDD | VDD | | | | | | | | |
| F7 | VSS | VSS | VSS | | | | | | | | |
| H7 | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | UART3_TX | SDHC0_D3 | | | | |
| G4 | PTE5 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | SDHC0_D2 | | | | |
| F3 | PTE6 | DISABLED | | PTE6 | SPI1_PCS3 | UART3_CTS_b | I2S0_MCLK | | I2S0_CLKIN | | |
| E6 | VDD | VDD | VDD | | | | | | | | |
| G7 | VSS | VSS | VSS | | | | | | | | |
| L6 | VSS | VSS | VSS | | | | | | | | |
| F1 | USB0_DP | USB0_DP | USB0_DP | | | | | | | | |