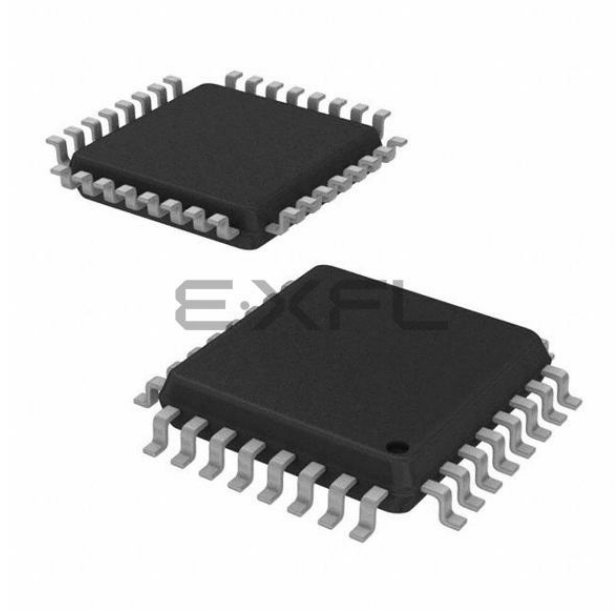

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Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa32vlc

Chapter 14
Real-time counter (RTC)

Chapter 1
Device Overview

1.1 Introduction

These devices are members of the low-cost, high-performance HCS08 family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 central processor unit and are available with a variety of modules, memory sizes and types, and package types. The following table summarizes the peripheral availability per package type for the devices available.

Table 1-1. Memory and package availability

Feature	MC9S08PA60	MC9S08PA32
Flash size (bytes)	60,864	32,768
EEPROM size (bytes)	256	256
RAM size (bytes)	4,096	4,096
LQFP-64	Yes	Yes
QFP-64	Yes	Yes
LQFP-48	Yes	Yes
LQFP-44	Yes	Yes
LQFP-32	Yes	Yes

Table 1-2. Feature availability

Pin number	64-pin	48-pin	44-pin	32-pin
Bus frequency (MHz)	20	20	20	20
IRQ	Yes			
WDOG	Yes			
DBG	Yes			
IPC	Yes			
CRC	Yes			
ICS	Yes			

Table continues on the next page...

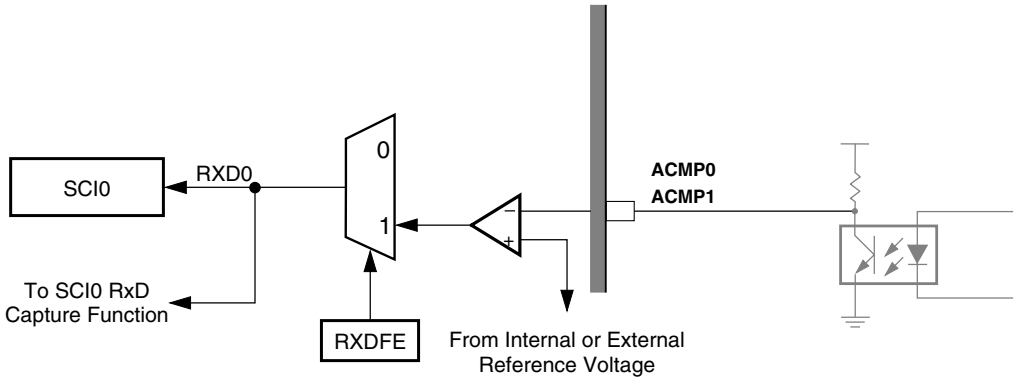

Figure 6-4. IR demodulation diagram

6.5.5 RTC capture

RTC overflow may be captured by FTM1 channel 1 by setting SYS_SOPT2[RTCC] bit. When this bit is set, the RTC overflow is connected to FTM1 channel 1 for capture, the FTM1CH1 pin is released to other shared functions.

6.5.6 FTM2 software synchronization

FTM2 contains three synchronization input trigger, one of which is a software trigger by writing 1 to the SYS_SOPT2[FTMSYNC] bit. Writing 0 to this bit takes no effect. This bit is always read 0.

6.5.7 ADC hardware trigger

ADC module may initiate a conversion via a hardware trigger. MTIM0 overflow, RTC, FTM2 match trigger with 8-bit programmable delay, and FTM2 init trigger with 8-bit programmable delay can be enabled as the hardware trigger for the ADC module by setting the SYS_SOPT2[ADHWT] bits. The following table shows the ADC hardware trigger setting.

Table 6-1. ADC hardware trigger setting

ADHWT	ADC hardware trigger
0:0	RTC overflow
0:1	MTIM0 overflow
1:0	FTM2 init trigger with 8-bit programmable delay
1:1	FTM2 match trigger with 8-bit programmable delay

PORT_PTED field descriptions (continued)

Field	Description
	Reset forces PTED to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.6 Port F Data Register (PORT_PTFD)

Address: 0h base + 5h offset = 5h

Bit	7	6	5	4	3	2	1	0
Read Write	PTFD							
Reset	0	0	0	0	0	0	0	0

PORT_PTFD field descriptions

Field	Description
PTFD	Port F Data Register Bits For port F pins that are configured as inputs, a read returns the logic level on the pin. For port F pins that are configured as outputs, a read returns the last value that was written to this register. For port F pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port F pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTFD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.7 Port G Data Register (PORT_PTGD)

Address: 0h base + 6h offset = 6h

Bit	7	6	5	4	3	2	1	0
Read	0				PTGD			
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTGD field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PTGD	Port G Data Register Bits For port G pins that are configured as inputs, a read returns the logic level on the pin. For port G pins that are configured as outputs, a read returns the last value that was written to this register.

Table continues on the next page...

PORT_IOFLT0 field descriptions (continued)

Field	Description
3–2 FLTB	Filter selection for input from PTB 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
FLTA	Filter selection for input from PTA 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3

7.7.27 Port Filter Register 1 (PORT_IOFLT1)

This register sets the filters for input from PTE to PTH.

Address: 0h base + 30EDh offset = 30EDh

Bit	7	6	5	4	3	2	1	0
Read Write	FLTH		FLTG		FLTF		FLTE	
Reset	0	0	0	0	0	0	0	0

PORT_IOFLT1 field descriptions

Field	Description
7–6 FLTH	Filter selection for input from PTH 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
5–4 FLTG	Filter selection for input from PTG 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
3–2 FLTF	Filter selection for input from PTF 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3

Table continues on the next page...

PORT_PTCPE field descriptions (continued)

Field	Description
	This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 7. 1 Pullup enabled for port C bit 7.
6 PTCPE6	Pull Enable for Port C Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 6. 1 Pullup enabled for port C bit 6.
5 PTCPE5	Pull Enable for Port C Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 5. 1 Pullup enabled for port C bit 5.
4 PTCPE4	Pull Enable for Port C Bit 4 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 4. 1 Pullup enabled for port C bit 4.
3 PTCPE3	Pull Enable for Port C Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 3. 1 Pullup enabled for port C bit 3.
2 PTCPE2	Pull Enable for Port C Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 2. 1 Pullup enabled for port C bit 2.
1 PTCPE1	Pull Enable for Port C Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 1. 1 Pullup enabled for port C bit 1.
0 PTCPE0	Pull Enable for Port C Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect.

Table continues on the next page...

- ICS_C1[IREFS] bit is written to 0
- BDM mode is not active and ICS_C2[LP] bit is written to 1

In FLL bypassed external low power mode, the ICSOUT clock is derived from the external reference clock source and the FLL is disabled. The ICSLCLK will be not available for BDC communications. The external reference clock source is enabled.

8.2.2.7 Stop (STOP)

In stop mode, the FLL is disabled and the internal clock source can be enabled or disabled. The BDC clock is not available and the ICS does not provide MCU clock source.

Stop mode is entered whenever the MCU enters a stop state. In this mode, all ICS clock signals are static except in the following cases:

- ICSIRCLK will be active in stop mode when all of the following conditions occur:
  - ICS_C1[IRCLKEN] bit is written to 1
  - ICS_C1[IREFSTEN] bit is written to 1
- OSCOUT will be active in stop mode when all of the following conditions occur:
  - ICS_OSCSC[OSCEN] bit is written to 1
  - ICS_OSCSC[OSCSTEN] bit is written to 1

NOTE

The DCO frequency changes from the pre-stop value to its reset value and the FLL need to re-acquire the lock before the frequency is stable. Timing sensitive operations must wait for the FLL acquisition time, t_{Aquire}, before executing.

9.9.4 Inter-Integrated Circuit (I2C)

This device contains an inter-integrated circuit (I2C) module for communication with other integrated circuits.

The following figure shows the device block diagram highlighting I2C module and pins.

10.3.7.3 Indexed to Direct, Post Increment

Used only by the MOV instruction, this addressing mode accesses a source operand addressed by the H:X register, and a destination location within the direct page addressed by the byte following the opcode. H:X is incremented after the source operand is accessed.

10.3.7.4 Direct to Indexed, Post-Increment

Used only with the MOV instruction, this addressing mode accesses a source operand addressed by the byte following the opcode, and a destination location addressed by the H:X register. H:X is incremented after the destination operand is written.

10.4 Operation modes

The CPU can be placed into the following operation modes: stop, wait, background and security.

10.4.1 Stop mode

Usually, all system clocks, including the crystal oscillator (when used), are halted during stop mode to minimize power consumption. In such systems, external circuitry is needed to control the time spent in stop mode and to issue a signal to wake up the target MCU when it is time to resume processing. Unlike the earlier M68HC05 and M68HC08 MCUs, the HCS08 V6 can be configured to keep a minimum set of clocks running in stop mode. This optionally allows an internal periodic signal to wake the target MCU from stop mode.

When a host debug system is connected to the background debug pin (BKGD) and the ENBDM control bit has been set by a serial command through the background interface (or because the MCU was reset into active background mode), the oscillator is forced to remain active when the MCU enters stop mode. In this case, if a serial BACKGROUND command is issued to the MCU through the background debug interface while the CPU is in stop mode, CPU clocks will resume and the CPU will enter active background mode where other serial background commands can be processed. This ensures that a host development system can still gain access to a target MCU even if it is in stop mode.

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
BCLR n,opr8a	Clear Bit n in Memory	Mn ← 0	–	–	–	–	–	–	DIR (b1)	13	dd	5
			–	–	–	–	–	–	DIR (b2)	15	dd	5
			–	–	–	–	–	–	DIR (b3)	17	dd	5
			–	–	–	–	–	–	DIR (b4)	19	dd	
			–	–	–	–	–	–	DIR (b5)	1B	dd	5
			–	–	–	–	–	–	DIR (b6)	1D	dd	5
			–	–	–	–	–	–	DIR (b7)	1F	dd	5
BCS rel	Branch if Carry Bit Set (same as BLO)	Branch if (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ rel	Branch if Equal	Branch if (Z) = 1	–	–	–	–	–	–	REL	27	rr	3
BGE rel	Branch if Greater Than or Equal To (Signed Operands)	Branch if (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGND	Enter Active Background if ENBDM = 1	Waits For and Processes BDM Commands Until GO, TRACE1, or TAGGO	–	–	–	–	–	–	INH	82		5+
BGT rel	Branch if Greater Than (Signed Operands)	Branch if (Z) ǀ (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC rel	Branch if Half Carry Bit Clear	Branch if (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS rel	Branch if Half Carry Bit Set	Branch if (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI rel	Branch if Higher	Branch if (C) ǀ (Z) = 0	–	–	–	–	–	–	REL	22	rr	3
BHS rel	Branch if Higher or Same (same as BCC)	Branch if (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH rel	Branch if IRQ Pin High	Branch if IRQ pin = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL rel	Branch if IRQ Pin Low	Branch if IRQ pin = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #opr8i	Bit Test	(A) & (M), (CCR Updated but Operands Not Changed)	0	–	–	↕	↕	–	IMM	A5	ii	2
BIT opr8a			0	–	–	↕	↕	–	DIR	B5	dd	3
BIT opr16a			0	–	–	↕	↕	–	EXT	C5	hh ll	4
BIT oprx16,X			0	–	–	↕	↕	–	IX2	D5	ee ff	4
BIT oprx8,X			0	–	–	↕	↕	–	IX1	E5	ff	3
BIT ,X			0	–	–	↕	↕	–	IX	F5		3
BIT oprx16,SP			0	–	–	↕	↕	–	SP2	9ED5	ee ff	5
BIT oprx8,SP			0	–	–	↕	↕	–	SP1	9EE5	ff	4

Table continues on the next page...

In output compare mode, the FTM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter matches the value in the CnVH:CnVL registers of an output compare channel, the channel (n) output can be set, cleared, or toggled.

When a channel is initially configured to toggle mode, the previous value of the channel output is held until the first output compare event occurs.

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnVH:CnVL).

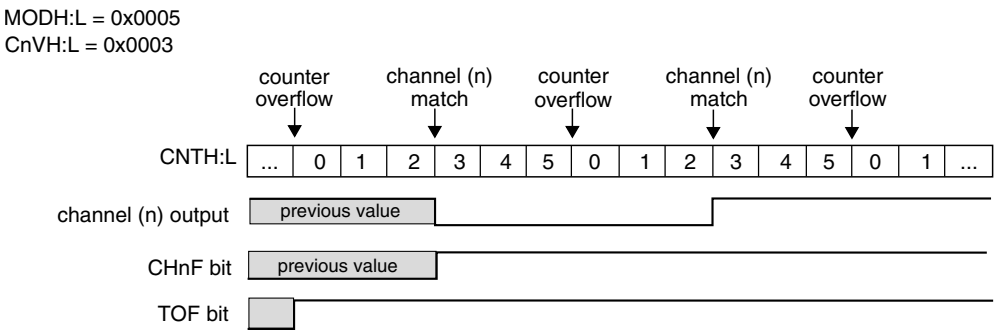

Figure 12-196. Example of the output compare mode when the match toggles the channel output

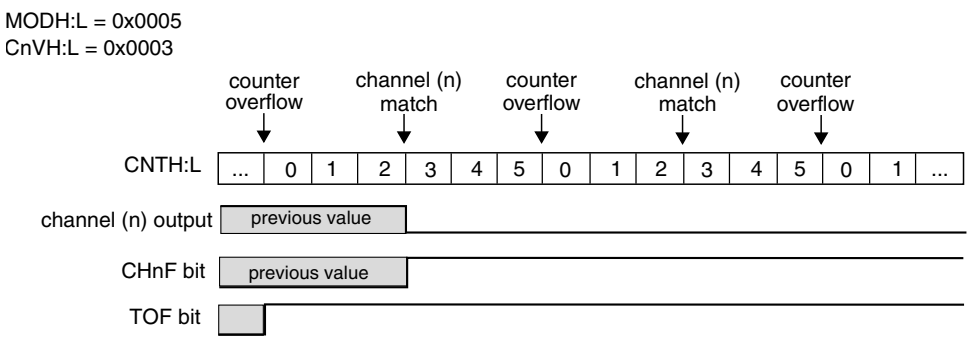

Figure 12-197. Example of the output compare mode when the match clears the channel output

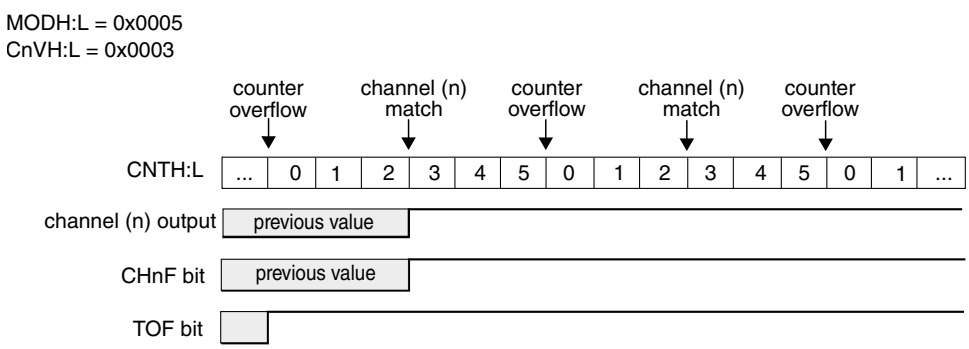

Figure 12-198. Example of the output compare mode when the match sets the channel output

12.4.8 Combine mode

The combine mode is selected when all of the following apply:

- (FTMEN = 1)
- (DECAPEN = 0)
- (COMBINE = 1)
- (CPWMS = 0)

In combine mode, the even channel (n) and adjacent odd channel (n+1) are combined to generate a PWM signal in the channel (n) output.

In the combine mode, the PWM period is determined by (MODH:L – CNTINH:L + 0x0001) and the PWM pulse width (duty cycle) is determined by (|C(n+1)VH:L – C(n)VH:L|).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = C(n)VH:L). The CH(n+1)F bit is set and the channel (n+1) interrupt is generated (if CH(n+1)IE = 1) at the channel (n+1) match (FTM counter = C(n+1)VH:C(n+1)VL).

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced low at the beginning of the period (FTM counter = CNTINH:L) and at the channel (n+1) match (FTM counter = C(n+1)VH:L). It is forced high at the channel (n) match (FTM counter = C(n)VH:L). See the following figure.

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced high at the beginning of the period (FTM counter = CNTINH:L) and at the channel (n+1) match (FTM counter = C(n+1)VH:L). It is forced low at the channel (n) match (FTM counter = C(n)VH:L). See the following figure.

In combine mode, the ELS(n+1)B and ELS(n+1)A bits are not used in the generation of the channels (n) and (n+1) output.

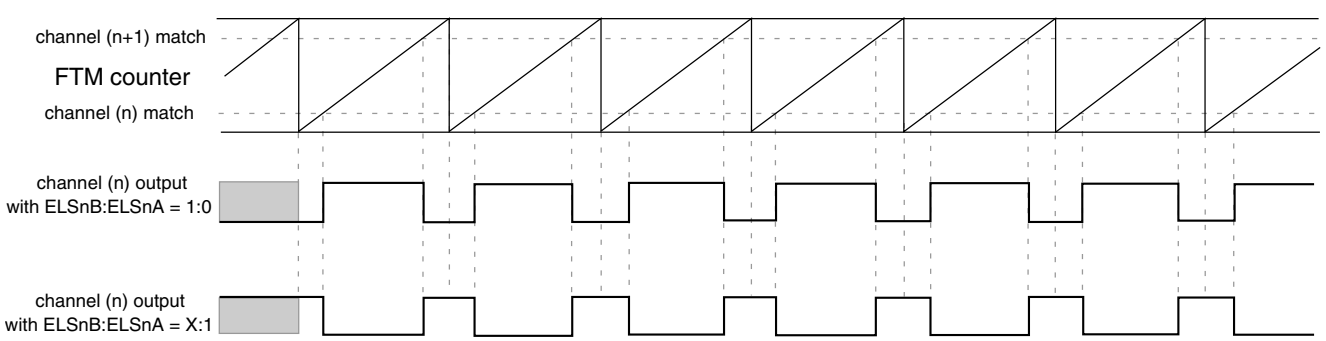

Figure 12-205. Combine mode

The following figures illustrate the generation of PWM signals using combine mode.

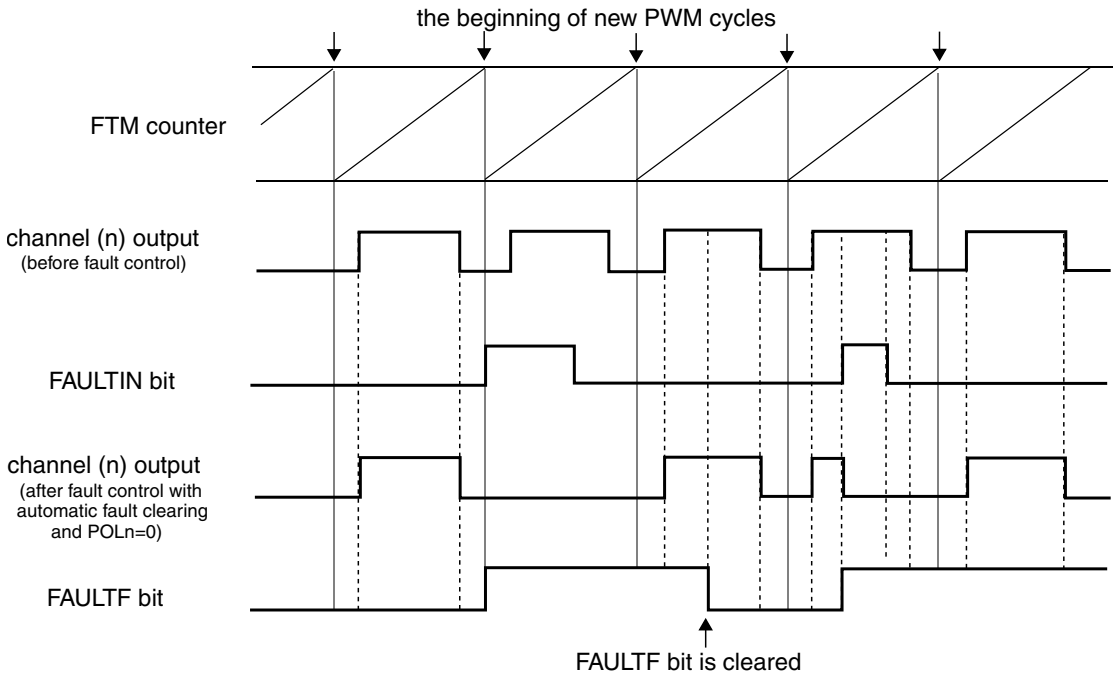

Figure 12-244. Fault control with automatic fault clearing

12.4.14.2 Manual fault clearing

If the manual fault clearing is selected (FAULTM[1:0] = 0:1 or 1:0), then disabled channel outputs are enabled when the FAULTF bit is cleared and a new PWM cycle begins. See the following figure.

It is possible to manually clear a fault by clearing the FAULTF bit, and enable disabled channels regardless of the fault input signal (FAULTIN) (the filter output if the filter is enabled or the synchronizer output if the filter is disabled). However, it is recommended to verify the value of the fault input signal (value of the FAULTIN bit) before clearing the FAULTF bit to avoid unpredictable results.

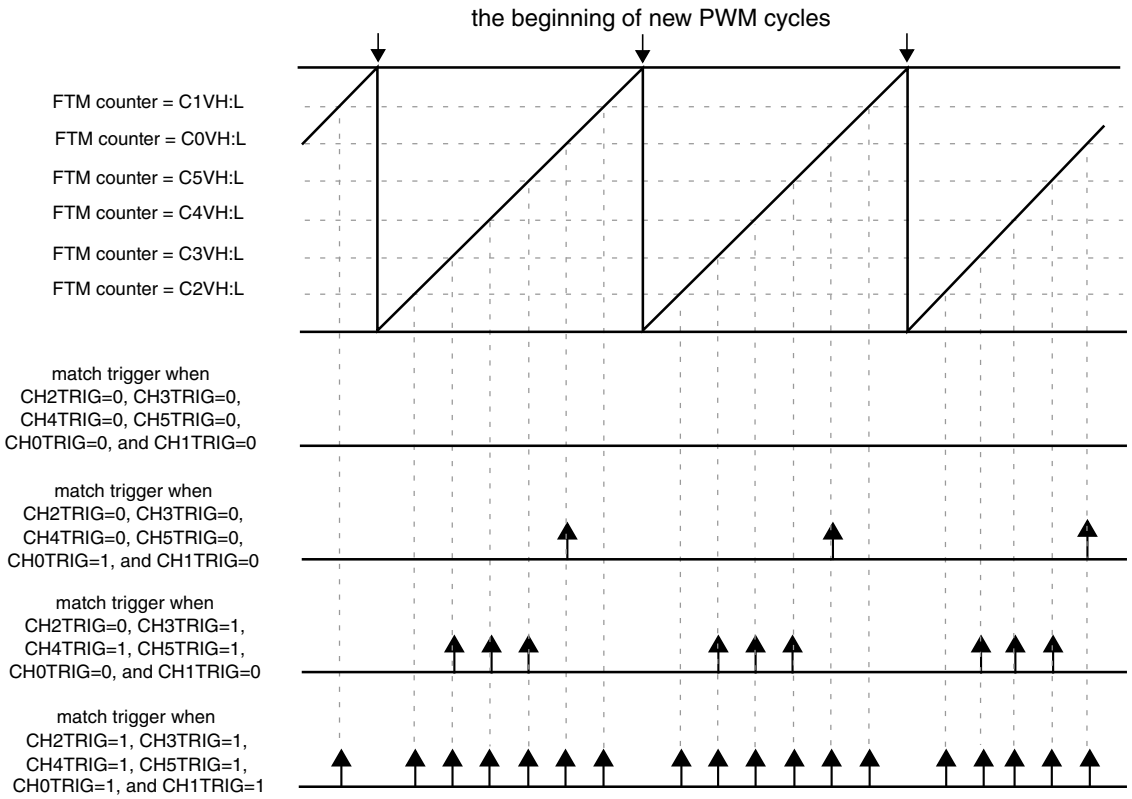

Figure 12-247. Match triggers

Note

Match trigger is available only in combine mode.

12.4.19 Initialization trigger

If INITTRIGEN = 1, the FTM generates a trigger when the FTM counter is updated with the CNTINH:L registers value in the following cases:

- The FTM counter is automatically updated with the CNTINH:L registers value by selected counting mode.

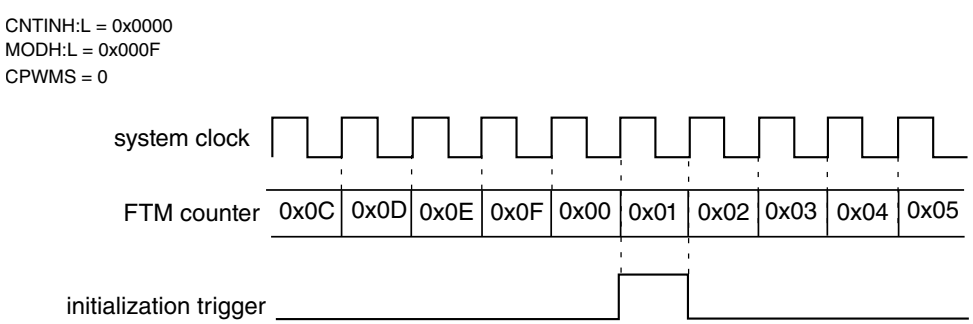

Figure 12-248. Initialization trigger is generated when the FTM counter achieves the value of CNTINH:L

12.4.23 BDM mode

When BDM mode is active, the FlexTimer counter and the channels output are frozen.

However, the value of FlexTimer counter or the channels output are modified in BDM mode when:

- A write of any value to the CNTH or CNTL registers (Counter reset) resets the FTM counter to the value of CNTINH:L and the channels output to their initial value, except for channels in output compare mode.
- The PWM synchronization with REINIT = 1 (see FTM counter synchronization) resets the FTM counter to the value of CNTINH:L registers and the channels output to their initial value, except for channels in output compare mode.
- The initialization (Initialization) forces the value of the CHnOI bit to the channel (n) output.

Note

Do not use the above cases together with fault control (Fault control). If fault control is enabled and the fault condition is at the enabled fault input, these cases reset the FTM counter to the CNTINH:L value and the channels output to their initial value.

12.5 Reset overview

The FTM is reset whenever any chip reset occurs.

When the FTM exits from reset:

- The FTM counter and the prescaler counter are zero and are stopped (CLKS[1:0] = 0b00)
- The timer overflow interrupt is zero (Timer overflow interrupt)
- The channels interrupts are zero (Channel (n) interrupt)
- The fault interrupt is zero (Fault interrupt)
- The channels are in input capture mode (Input capture mode)
- The channels outputs are zero
- The channels pins are not controlled by FTM (ELS(n)B:ELS(n)A = 0b00). See table "Mode, Edge, and Level Selection"

The receive input active edge detect circuit remains active in Stop3 mode. An active edge on the receive input brings the CPU out of Stop3 mode if the interrupt is not masked (SCI_BDH[RXEDGIE] = 1).

Because the clocks are halted, the SCI module resumes operation upon exit from stop, only in Stop3 mode. Software must ensure stop mode is not entered while there is a character (including preamble, break and normal data) being transmitted out of or received into the SCI module, that means SCI_S1[TC] =1, SCI_S1[TDRE] = 1, and SCI_S2[RAF] = 0 must all meet before entering stop mode.

15.4.6.3 Loop mode

When SCI_C1[LOOPS] is set, the SCI_C1[RSRC] bit in the same register chooses between loop mode (SCI_C1[RSRC] = 0) or single-wire mode (SCI_C1[RSRC] = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

15.4.6.4 Single-wire operation

When SCI_C1[LOOPS] is set, SCI_C1[RSRC] chooses between loop mode (SCI_C1[RSRC] = 0) or single-wire mode (SCI_C1[RSRC] = 1). Single-wire mode implements a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general-purpose port I/O pin.

In single-wire mode, the SCI_C3[TXDIR] bit controls the direction of serial data on the TxD pin. When SCI_C3[TXDIR] is cleared, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When SCI_C3[TXDIR] is set, the TxD pin is an output driven by the transmitter. In single-wire mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general-purpose port I/O pin.

17.4.1 General

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI Control Register 1. While C1[SPE] is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select (SS)
- Serial clock (SPSCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

An SPI transfer is initiated in the master SPI device by reading the SPI status register (SPIx_S) when S[SPTEF] = 1 and then writing data to the transmit data buffer (write to SPIx_DH:SPIx_DL). When a transfer is complete, received data is moved into the receive data buffer. The SPIx_DH:SPIx_DL registers act as the SPI receive data buffer for reads and as the SPI transmit data buffer for writes.

The Clock Phase Control (CPHA) and Clock Polarity Control (CPOL) bits in the SPI Control Register 1 (SPIx_C1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. C1[CPHA] is used to accommodate two fundamentally different protocols by sampling data on odd numbered SPSCK edges or on even numbered SPSCK edges.

The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI Control Register 1 is set, master mode is selected; when C1[MSTR] is clear, slave mode is selected.

17.4.2 Master mode

The SPI operates in master mode when C1[MSTR] is set. Only a master SPI module can initiate transmissions. A transmission begins by reading the SPIx_S register while S[SPTEF] = 1 and writing to the master SPI data registers. If the shift register is empty, the byte immediately transfers to the shift register. The data begins shifting out on the MOSI pin under the control of the serial clock.

- SPSCK
  - The SPR3, SPR2, SPR1, and SPR0 baud rate selection bits in conjunction with the SPPR2, SPPR1, and SPPR0 baud rate preselection bits in the SPI Baud Rate register control the baud rate generator and determine the speed of the

Note

Care must be taken when expecting data from a master while the slave is in a Wait mode or a Stop mode where the peripheral bus clock is stopped but internal logic states are retained. Even though the shift register continues to operate, the rest of the SPI is shut down (that is, an SPRF interrupt is not generated until an exit from Stop or Wait mode). Also, the data from the shift register is not copied into the SPIx_DH:SPIx_DL registers until after the slave SPI has exited Wait or Stop mode. An SPRF flag and SPIx_DH:SPIx_DL copy is only generated if Wait mode is entered or exited during a transmission. If the slave enters Wait mode in idle mode and exits Wait mode in idle mode, neither an SPRF nor a SPIx_DH:SPIx_DL copy occurs.

17.4.10.3 SPI in Stop mode

Operation in a Stop mode where the peripheral bus clock is stopped but internal logic states are retained depends on the SPI system. The Stop mode does not depend on C2[SPISWAI]. Upon entry to this type of stop mode, the SPI module clock is disabled (held high or low).

- If the SPI is in master mode and exchanging data when the CPU enters the Stop mode, the transmission is frozen until the CPU exits stop mode. After the exit from stop mode, data to and from the external SPI is exchanged correctly.
- In slave mode, the SPI remains synchronized with the master.

The SPI is completely disabled in a stop mode where the peripheral bus clock is stopped and internal logic states are not retained. After an exit from this type of stop mode, all registers are reset to their default values, and the SPI module must be reinitialized.

17.4.11 Reset

The reset values of registers and signals are described in the Memory Map and Register Descriptions content, which details the registers and their bitfields.

- If a data transmission occurs in slave mode after a reset without a write to SPIx_DH:SPIx_DL, the transmission consists of "garbage" or the data last received from the master before the reset.
- Reading from SPIx_DH:SPIx_DL after reset always returns zeros.

the end of the pipe, the CPU executes a BGND instruction to go to active background mode rather than executing the tagged opcode. A force-type breakpoint causes the CPU to finish the current instruction and then go to active background mode.

If the background mode has not been enabled (ENBDM = 1) by a serial WRITE_CONTROL command through the BKGD pin, the CPU will execute an SWI instruction instead of going to active background mode.

23.4 Memory map and register description

This section contains the descriptions of the BDCand DBG registers and control bits. Refer to the high-page register summary in the device overview chapter of this data sheet for the absolute address assignments for all DBG registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

BDC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	BDC Status and Control Register (BDC_SCR)	8	R/W	00h	23.4.1/613
1	BDC Breakpoint Match Register: High (BDC_BKPTH)	8	R/W	00h	23.4.2/615
2	BDC Breakpoint Register: Low (BDC_BKPTL)	8	R/W	00h	23.4.3/616
3	System Background Debug Force Reset Register (BDC_SBDFR)	8	W (always reads 0)	00h	23.4.4/616

23.4.1 BDC Status and Control Register (BDC_SCR)

This register can be read or written by serial BDC commands (READ_STATUS and WRITE_CONTROL) but is not accessible to user programs because it is not located in the normal memory map of the MCU.

NOTE

The reset values shown in the register figure are those in the normal reset conditions. If the MCU is reset in BDM, ENBDM, BDMACT, CLKSW will be reset to 1 and others all be to 0.

24.4.4.3.6 A and B (full mode)

In the A and B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and B trigger mode, if the match condition for A and B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only B happens, no flags are set.

For breakpoint tagging operation with an end-trigger type trace, only matches from comparator A will be used to determine if the Breakpoint conditions are met and comparator B matches will be ignored.

24.4.4.3.7 A and not B (full mode)

In the A and not B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and not B trigger mode, if the match condition for A and not B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only not B occur no flags are set.

For breakpoint tagging operation with an end-trigger type trace, only matches from comparator A will be used to determine if the breakpoint conditions are met and comparator B matches will be ignored.

24.4.4.3.8 Inside range, A ≤ address ≤ B

In the inside range trigger mode, if the match condition for A and B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only B occur no flags are set.

24.4.4.3.9 Outside range, address < A or address > B

In the outside range trigger mode, if the match condition for A or B is met, the corresponding flag in the DBGS register is set.