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What is "Embedded - Microcontrollers"?

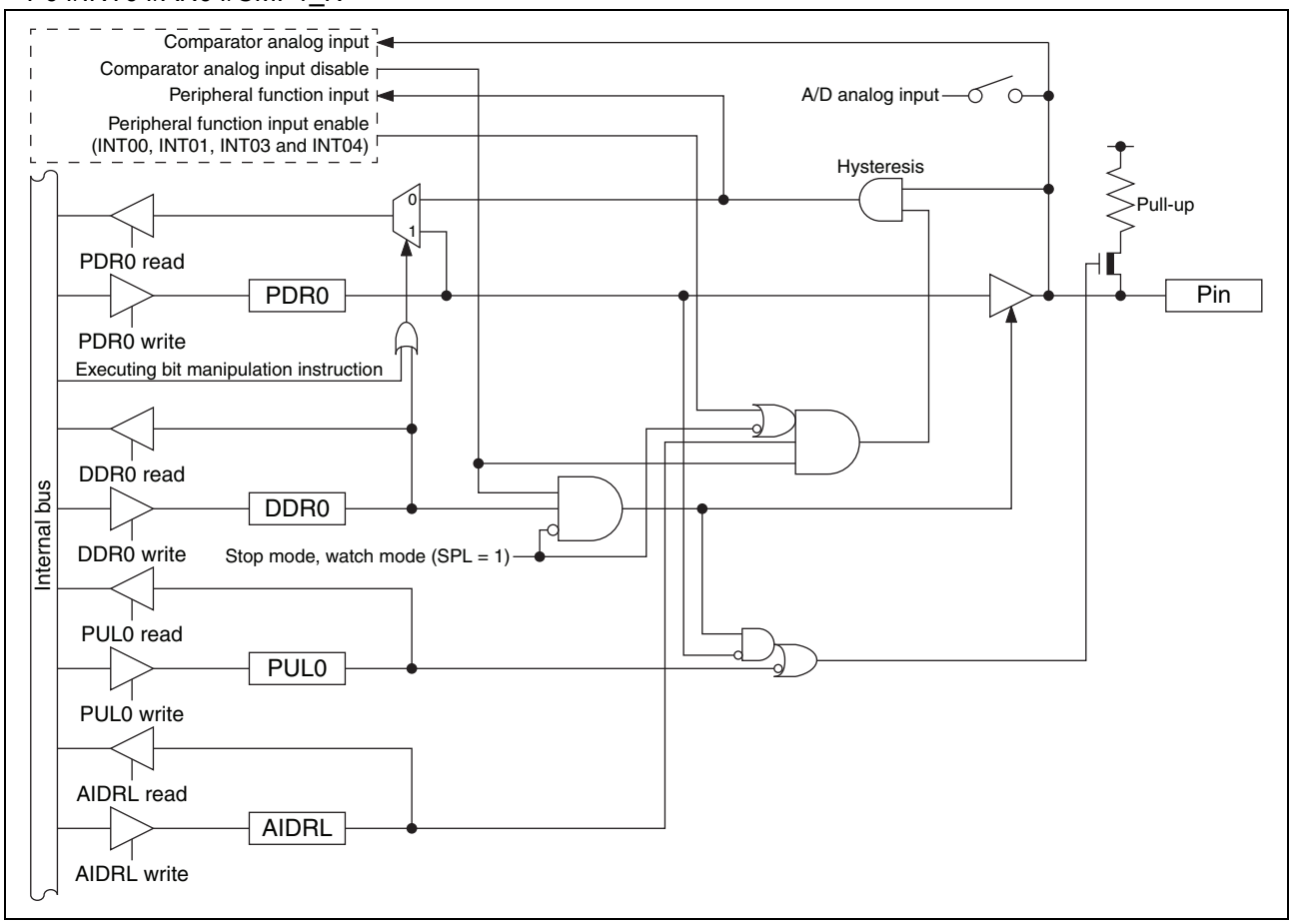
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f696kpmc-g-sne2

Address	Register abbreviation	Register name	R/W	Initial value
0x0055	ECCR	LIN-UART extended communication control register	R/W	0b000000XX
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I²C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I²C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I²C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I²C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I²C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I²C clock control register ch. 0	R/W	0b00000000
0x0066	OPCUR	16-bit MPG output control register (upper)	R/W	0b00000000
0x0067	OPCLR	16-bit MPG output control register (lower)	R/W	0b00000000
0x0068	IPCUR	16-bit MPG input control register (upper)	R/W	0b00000000
0x0069	IPCLR	16-bit MPG input control register (lower)	R/W	0b00000000
0x006A	NCCR	16-bit MPG noise cancellation control register	R/W	0b00000000
0x006B	TCSR	16-bit MPG timer control status register	R/W	0b00000000
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	—	(Disabled)	—	—
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111

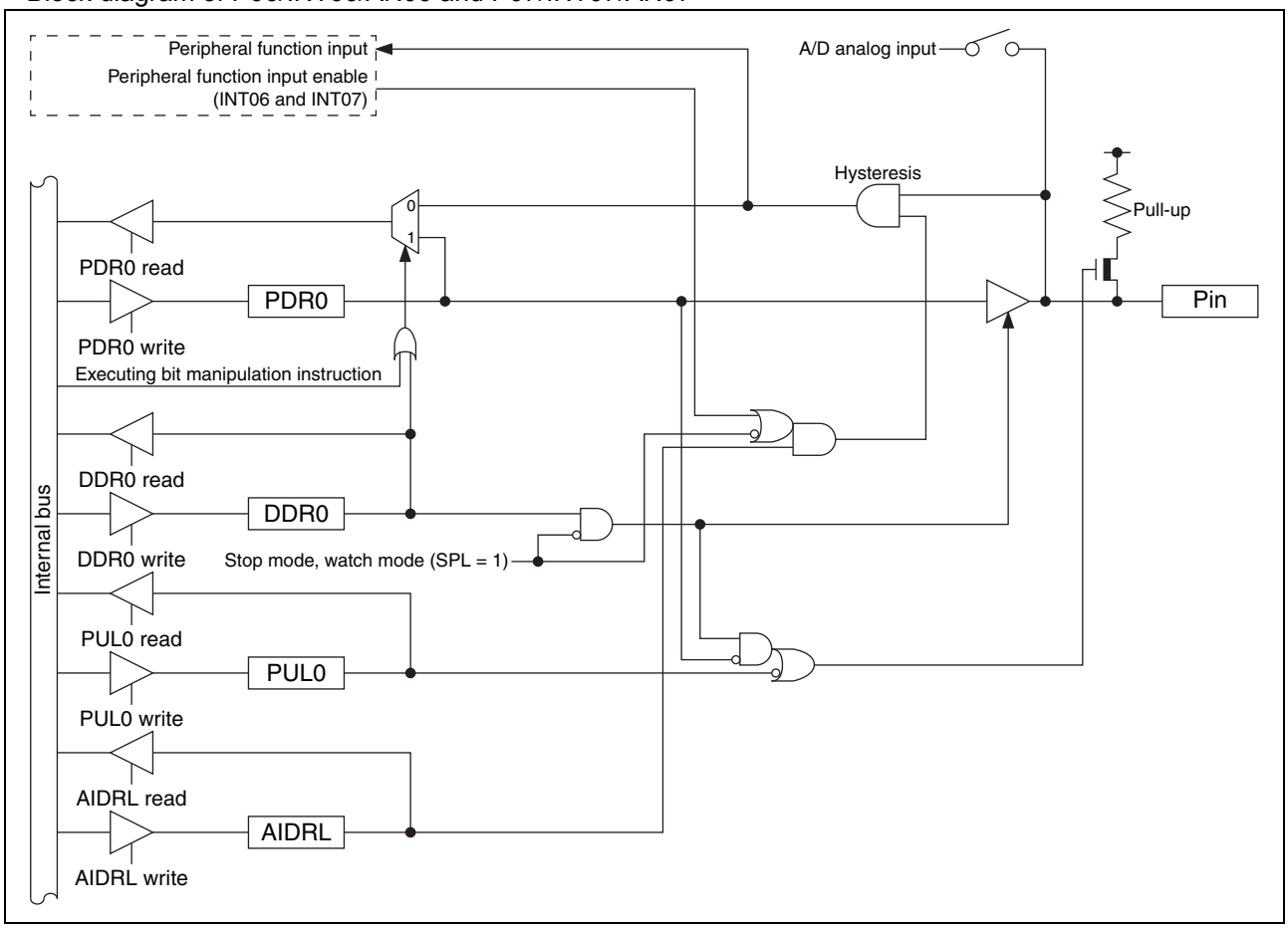
- Block diagram of P00/INT00/AN00/CMP0_P, P01/INT01/AN01/CMP0_N, P03/INT03/AN03/CMP1_P and P04/INT04/AN04/CMP1_N



- P06/INT06/AN06 pin
  This pin has the following peripheral functions:
  - External interrupt input pin (INT06)
  - 8/10-bit A/D converter analog input pin (AN06)

- P07/INT07/AN07 pin
  This pin has the following peripheral functions:
  - External interrupt input pin (INT07)
  - 8/10-bit A/D converter analog input pin (AN07)

- Block diagram of P06/INT06/AN06 and P07/INT07/AN07



17.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95690K Series Hardware Manual”.

17.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

17.2.2 Block diagrams of port 1

- P10/PPG10* pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG10)

- P11/PPG11* pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG11)

- P13/PPG00* pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG00)

- P14/PPG01* pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG01)

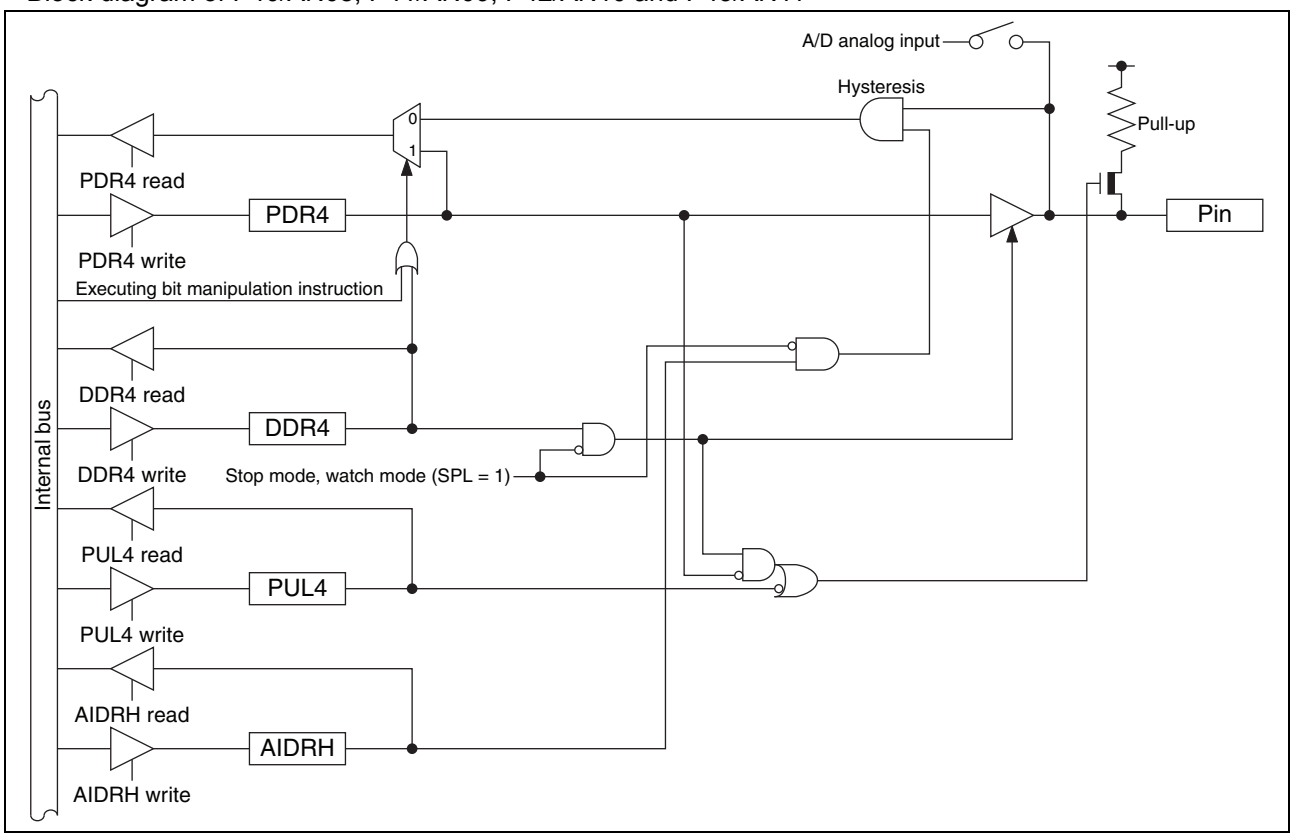
- P15/PPG20* pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 2 output pin (PPG20)

- P16/PPG21* pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 2 output pin (PPG21)

*: The 8/16-bit PPG output pins are mapped to pins according to the setting of the PPGSEL bit in the SYSC register. See the table below for details.

8/16-bit PPG output pin	SYSC:PPGSEL = 0	SYSC:PPGSEL = 1
	Pin	
PPG00	P13	P62
PPG01	P14	P63
PPG10	P10	P64
PPG11	P11	P65
PPG20	P15	P66
PPG21	P16	P67

- Block diagram of P40/AN08, P41/AN09, P42/AN10 and P43/AN11



17.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95690K Series Hardware Manual”.

17.5.1 Port 7 configuration

Port 7 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 7 data register (PDR7)
- Port 7 direction register (DDR7)
- Port 7 pull-up register (PUL7)

17.5.2 Block diagrams of port 7

- P70/TO00 pin

  This pin has the following peripheral function:
  - 8/16-bit composite time ch. 0 output pin (TO00)

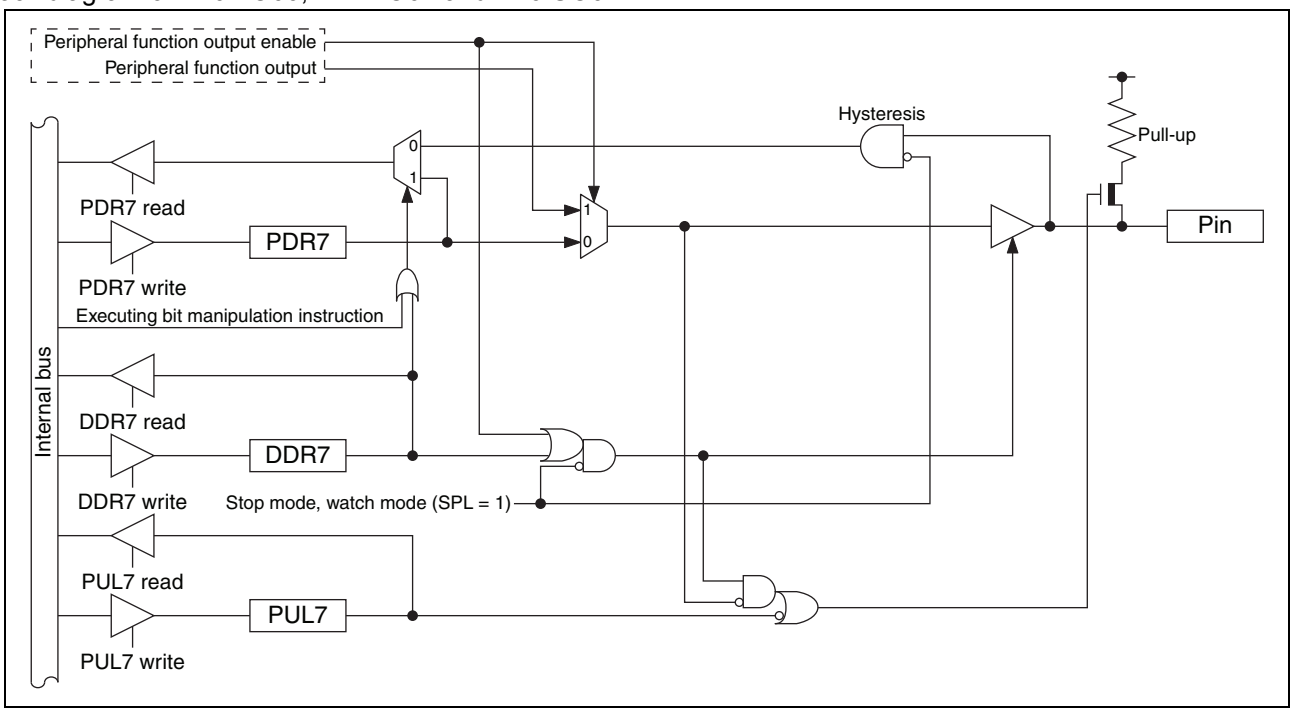
- P71/TO01 pin

  This pin has the following peripheral function:
  - 8/16-bit composite timer ch. 0 output pin (TO01)

- P76/UO0 pin

  This pin has the following peripheral function:
  - UART/SIO ch. 0 data output pin (UO0)

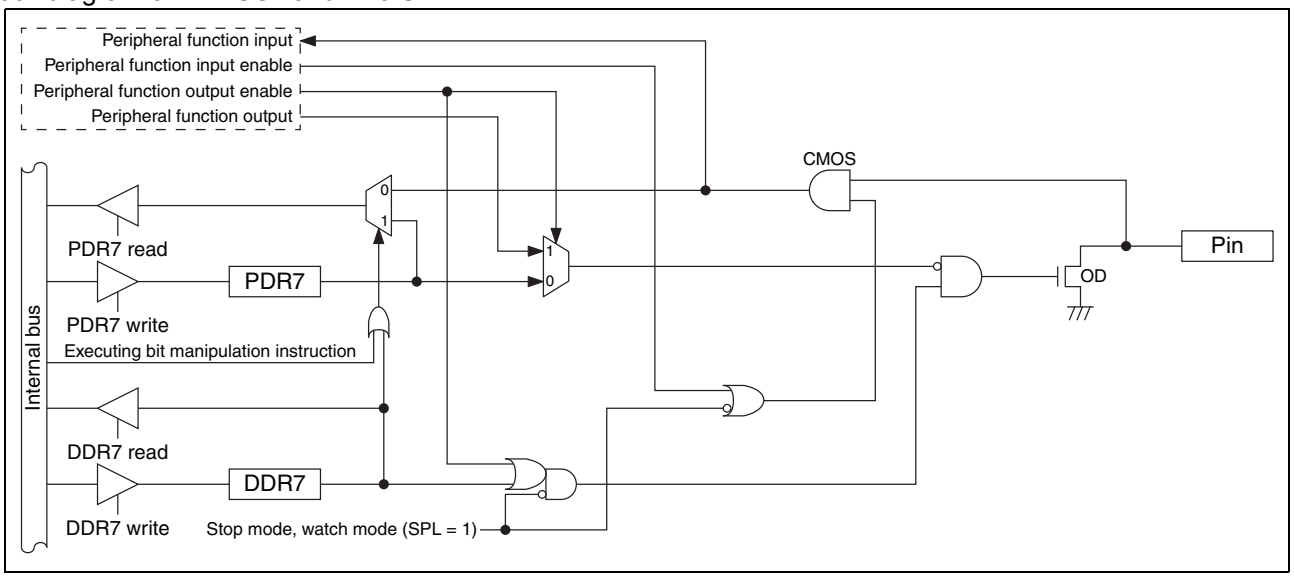
- Block diagram of P70/TO00, P71/TO01 and P76/UO0



- P72/SCL pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 clock I/O pin (SCL)

- P73/SDA pin
  This pin has the following peripheral function:
  - I²C bus interface ch. 0 data I/O pin (SDA)

- Block diagram of P72/SCL and P73/SDA



- P74/EC0 pin
  This pin has the following peripheral functions:
  - 8/16-bit composite timer ch. 0 clock input pin (EC0)

(Continued)

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P72/SCL P73/SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2, *9	- Hi-Z - Input blocked*2, *9	- Previous state kept - Input blocked*2, *9	- Hi-Z - Input blocked*2, *9	- Hi-Z - Input enabled*3 (However, it does not function.)
P70/TO00 P71/TO01 P76/UO0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z*5 - Input blocked*2	- Hi-Z - Input enabled*3 (However, it does not function.)
P74/EC0 P75/UCK0 P77/UI0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2, *7	- Hi-Z*5 - Input blocked*2, *7	- Previous state kept - Input blocked*2, *7	- Hi-Z*5 - Input blocked*2, *7	- Hi-Z - Input enabled*3 (However, it does not function.)

SPL: Pin state setting bit in the standby control register (STBC:SPL)
Hi-Z: High impedance
*1: The pin stays at the state shown when configured as a general-purpose I/O port.
*2: “Input blocked” means direct input gate operation from the pin is disabled.
*3: “Input enabled” means that the input function is enabled. While the input function is enabled, execute a pull-up or pull-down operation in order to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.
*4: The PF2/$\overline{\text{RST}}$ pin stays at the state shown when configured as a reset pin.
*5: The pull-up control setting is still effective.
*6: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled, and an analog signal can also be input to generate a comparator interrupt when the comparator interrupt is enabled.
*7: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.
*8: The output function of the comparator is still in operation in stop mode and watch mode.
*9: The I^2C bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wakeup function is enabled. For details of the MCU standby mode wakeup function, refer to “New 8FX MB95690K Series Hardware Manual”.

20. Electrical Characteristics

20.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average current	I_{OLAV1}	—	4	mA	Other than P60 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P60 to P67 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	37	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average current	I_{OHAV1}	—	–4	mA	Other than P60 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		–8		P60 to P67 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–47	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

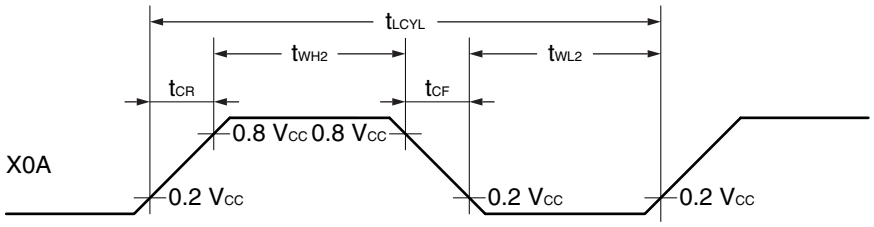
*3: Specific pins: P00 to P07, P10, P11, P13 to P17, P40 to P47, P60 to P67, P70, P71, P74 to P77, PF0, PF1, PG1, PG2

20.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

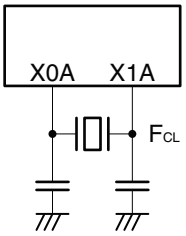
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P47, P72, P73, P77	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHS}	Other than P47, P72, P73, P77, PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P47, P72, P73, P77	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	Other than P47, P72, P73, P77, PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P72, P73, PF2	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P60 to P67, PF2	I_{OH} = –4 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P60 to P67	I_{OH} = –8 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P60 to P67	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P60 to P67	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	Other than P12, P72, P73, PF0, PF1, PF2	V_I = 0 V	25	50	100	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

- Input waveform generated when an external clock (subclock) is used

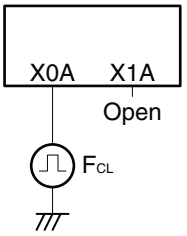


- Figure of subclock input port external connection

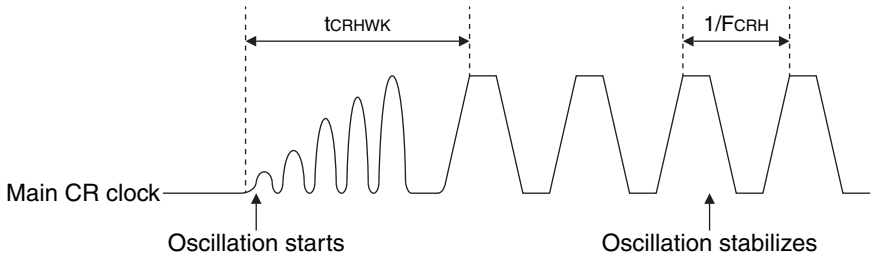
When a crystal oscillator or a ceramic oscillator is used



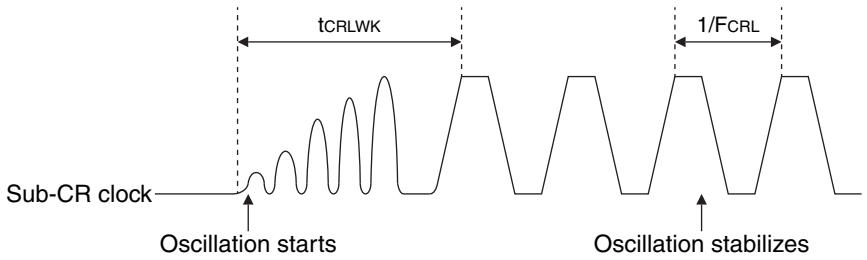
When an external clock is used



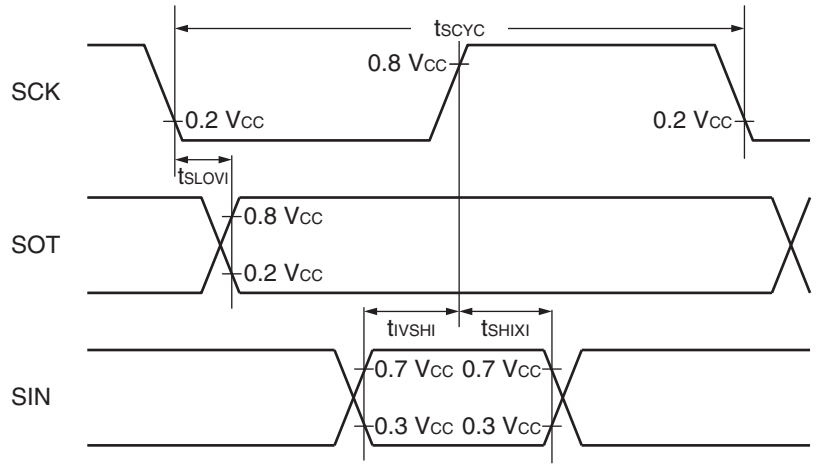
- Input waveform generated when an internal clock (main CR clock) is used



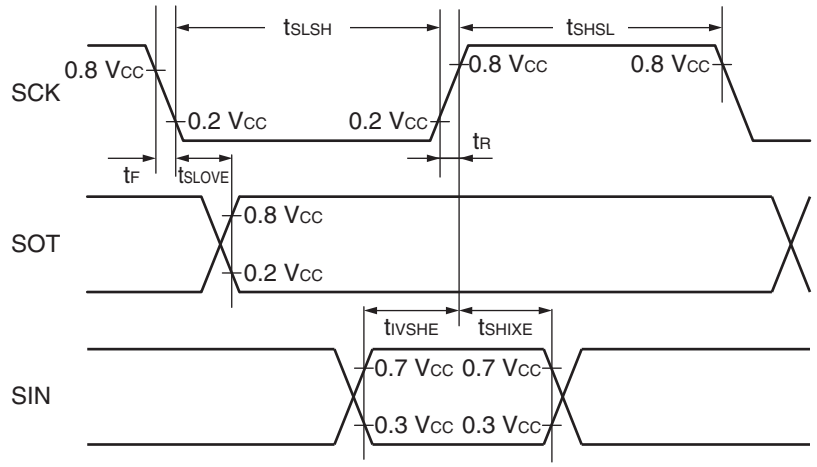
- Input waveform generated when an internal clock (sub-CR clock) is used

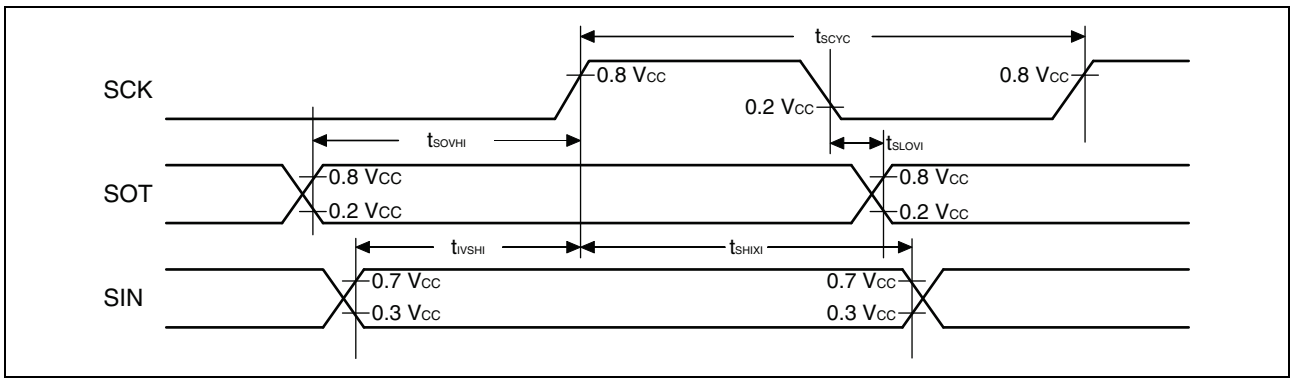


- Internal shift clock mode



- External shift clock mode





20.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage*	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
		2.61	2.8	2.99		
		2.89	3.1	3.31		
		3.08	3.3	3.52		
Detection voltage*	V_{DL-}	2.43	2.6	2.77	V	At power supply fall
		2.52	2.7	2.88		
		2.80	3	3.20		
		2.99	3.2	3.41		
Hysteresis width	V_{HYS}	—	—	100	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	650	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	650	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	30	µs	
Reset detection delay time	t_{d2}	—	—	30	µs	
LVD reset threshold voltage transition stabilization time	t_{stb}	10	—	—	µs	

*: After the LVD reset is enabled by the LVD reset circuit control register (LVDCC), the release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDCC register and the LVDR register, refer to “CHAPTER 16 LOW-VOLTAGE DETECTION RESET CIRCUIT” in “New 8FX MB95690K Series Hardware Manual”.

20.4.8 I²C Bus Interface Timing

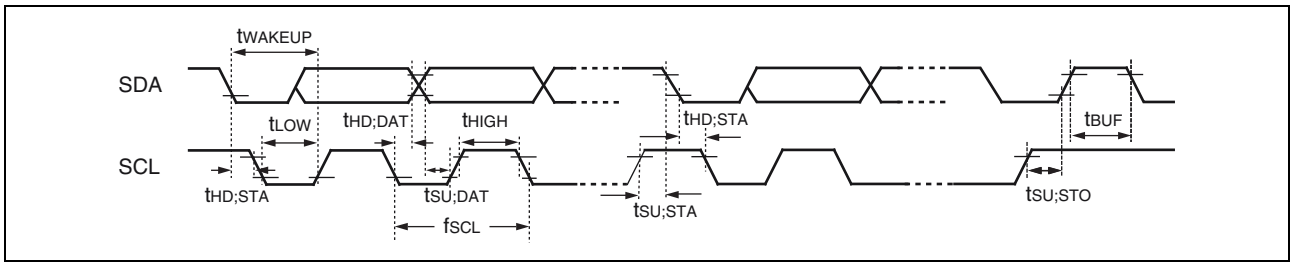
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT}$ ≥ 250 ns is fulfilled.



20.5 A/D Converter

20.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

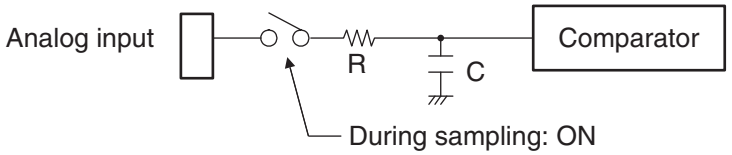
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		–3	—	+3	LSB	
Linearity error		–2.5	—	+2.5	LSB	
Differential linearity error		–1.9	—	+1.9	LSB	
Zero transition voltage	V_{0T}	V_{SS} – 7.2 LSB	V_{SS} + 0.5 LSB	V_{SS} + 8.2 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} – 6.2 LSB	V_{CC} – 1.5 LSB	V_{CC} + 9.2 LSB	V	
Compare time	—	3	—	10	µs	2.7 V ≤ V_{CC} ≤ 5.5 V
Sampling time	—	0.941	—	∞	µs	2.7 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 3.3 kΩ and external capacitance = 10 pF
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

20.5.2 Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter of the MB95690K Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

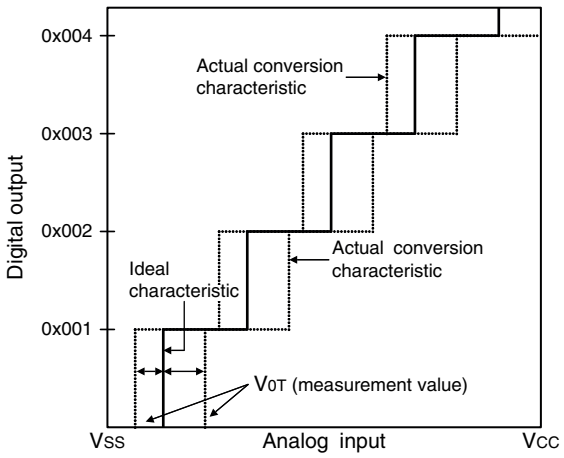
- Analog input equivalent circuit



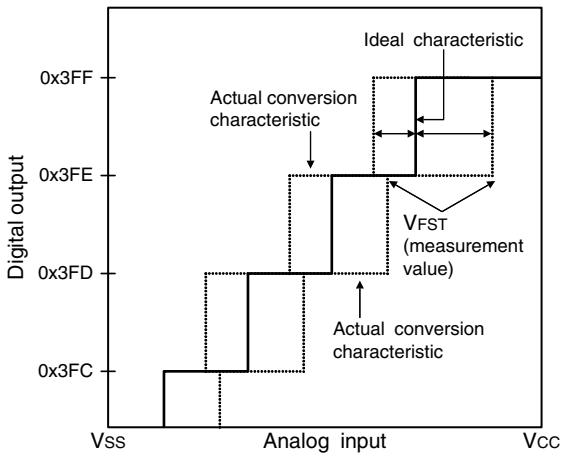
V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.45 kΩ (Max)	14.89 pF (Max)
2.7 V ≤ V_{CC} < 4.5 V	2.7 kΩ (Max)	14.89 pF (Max)

Note: The values are reference values.

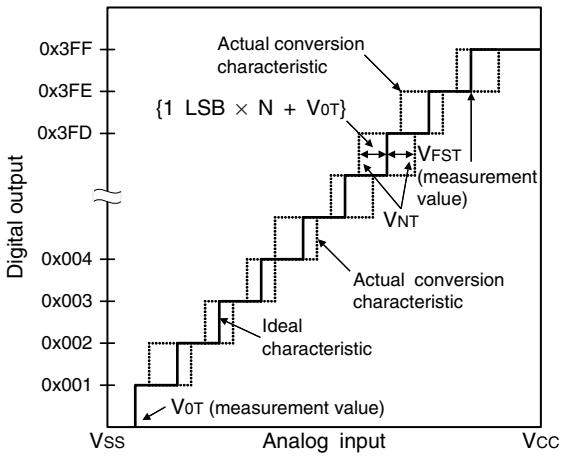
Zero transition error



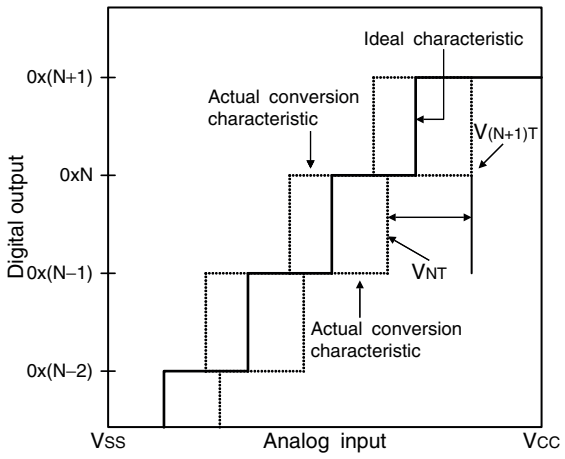
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

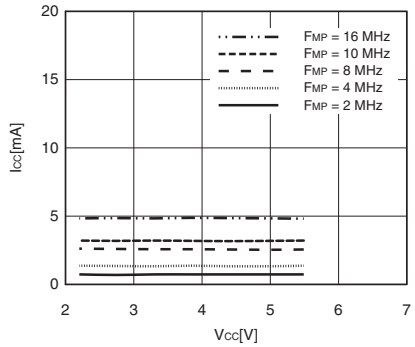
V_{FST} (ideal value) = V_{CC} – 2 LSB [V]

21. Sample Characteristics

- Power supply current temperature characteristics

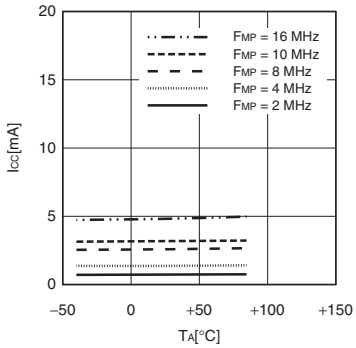
I_{CC} – V_{CC}

T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



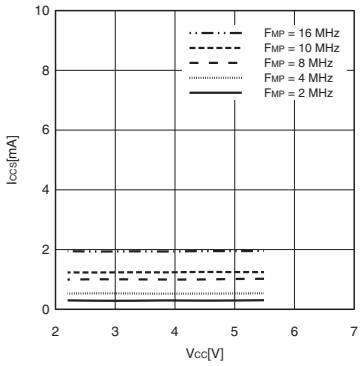
I_{CC} – T_A

V_{CC} = 5.5 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



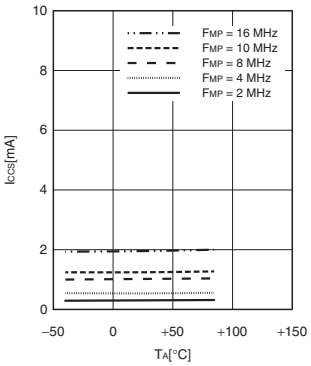
I_{CCS} – V_{CC}

T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



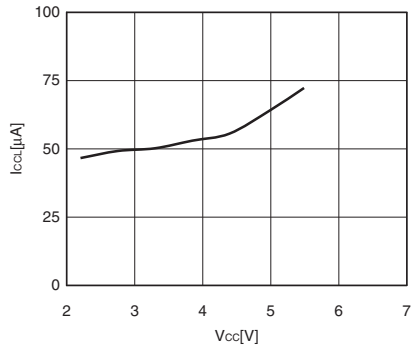
I_{CCS} – T_A

V_{CC} = 5.5 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



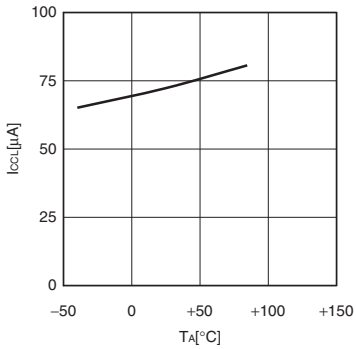
I_{CCL} – V_{CC}

T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating

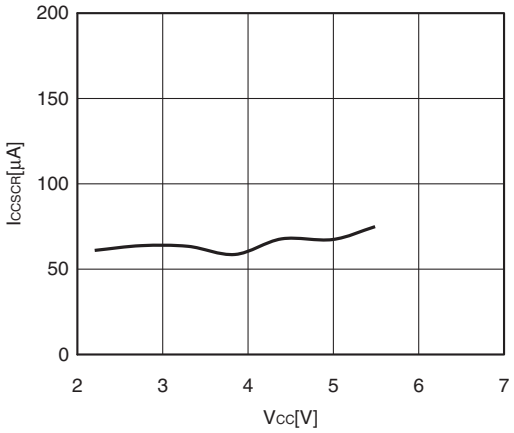


I_{CCL} – T_A

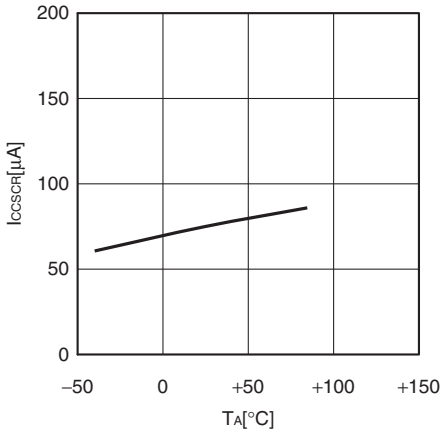
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCSCR} – V_{CC}
T_A = +25 °C, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode

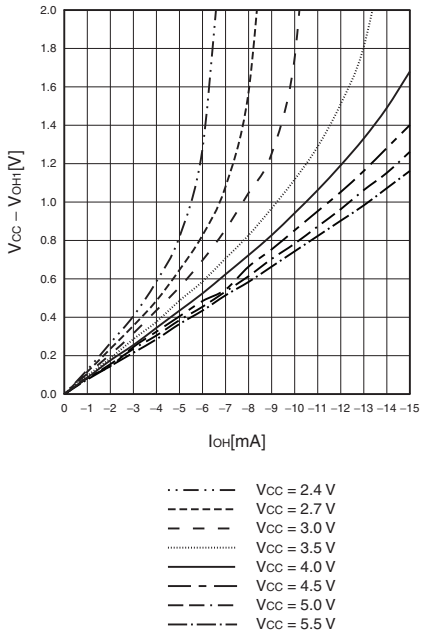


I_{CCSCR} – T_A
V_{CC} = 5.5 V, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode

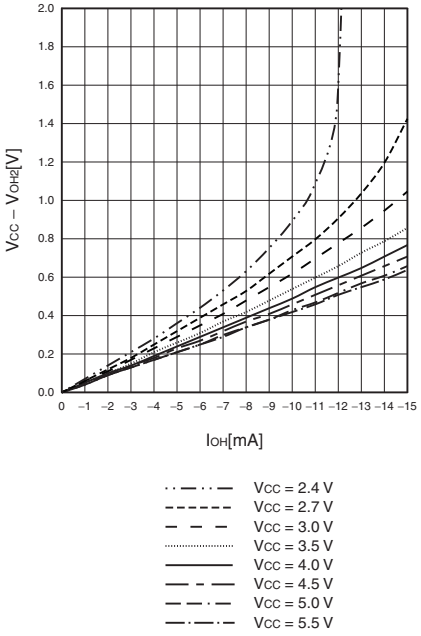


- Output voltage characteristics

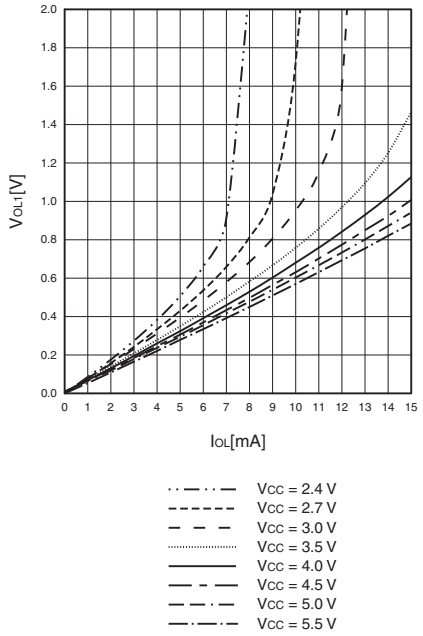
$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



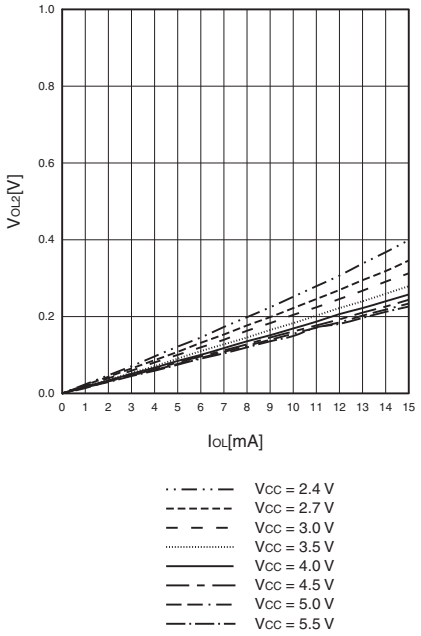
$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



$V_{OL1} - I_{OL}$
$T_A = +25\ °C$



$V_{OL2} - I_{OL}$
$T_A = +25\ °C$



24. Major Changes In This Edition

Spansion Publication Number: DS702-00014-2v0-E

Page	Section	Details
2	■ FEATURES	Added information on FPT-44P-M25.
4	■ PRODUCT LINE-UP	Added information on FPT-44P-M25 to the parameters “General-purpose I/O” and “8/10-bit A/D converter”.
5		Added information on FPT-44P-M25 to the parameter “External interrupt”.
6		Added FPT-44P-M25 to the parameter “Package”.
7	■ PACKAGES AND CORRESPONDING PRODUCTS	Added information on FPT-44P-M25.
9	■ PIN ASSIGNMENT	Added the pin assignment diagram of FPT-44P-M25.
13 to 16	■ PIN FUNCTIONS (FPT-44P-M25)	New section
17	■ PIN FUNCTIONS (FPT-48P-M49, FPT-52P-M02, LCC-48P-M11)	Renamed the section “■ PIN FUNCTIONS” to “■ PIN FUNCTIONS (FPT-48P-M49, FPT-52P-M02, LCC-48P-M11).
29	■ PIN CONNECTION • DBG pin	Revised details of “• DBG pin”.
	• $\overline{\text{RST}}$ pin	Revised details of “• $\overline{\text{RST}}$ pin”.
30	• C pin	Corrected the following statement. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
31	■ BLOCK DIAGRAM (FPT-44P-M25)	New section
32	■ BLOCK DIAGRAM (FPT-48P-M49, FPT-52P-M02, LCC-48P-M11)	Renamed the section “■ BLOCK DIAGRAM” to “■ BLOCK DIAGRAM (FPT-48P-M49, FPT-52P-M02, LCC-48P-M11).
75	■ I/O PORTS 6. Port F (4) Port F operations • Operation as an input port	Added the following statement. For a pin shared with other peripheral functions, disable the output of such peripheral functions.
78	7. Port G (4) Port G operations • Operation as an input port	Added the following statement. For a pin shared with other peripheral functions, disable the output of such peripheral functions.