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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f698kpmc-g-sne2

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
31	P64	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
	OPT2		MPG waveform sequencer output pin				
	PPG10		8/16-bit PPG ch. 1 output pin				
	EC1		8/16-bit composite timer ch. 1 clock input pin				
32	P65	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
	OPT3		MPG waveform sequencer output pin				
	PPG11		8/16-bit PPG ch. 1 output pin				
33	P66	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
	OPT4		MPG waveform sequencer output pin				
	PPG20		8/16-bit PPG ch. 2 output pin				
	PPG1		16-bit PPG timer ch. 1 output pin				
34	P67	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
	OPT5		MPG waveform sequencer output pin				
	PPG21		8/16-bit PPG ch. 2 output pin				
	TRG1		16-bit PPG timer ch. 1 trigger input pin				
35	P00	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	INT00		External interrupt input pin				
	AN00		8/10-bit A/D converter analog input pin				
	CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				
36	P01	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	INT01		External interrupt input pin				
	AN01		8/10-bit A/D converter analog input pin				
	CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				
37	P02	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	INT02		External interrupt input pin				
	AN02		8/10-bit A/D converter analog input pin				
	CMP0_O		Comparator ch. 0 digital output pin				
38	P03	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	INT03		External interrupt input pin				
	AN03		8/10-bit A/D converter analog input pin				
	CMP1_P		Comparator ch. 1 non-inverting analog input (positive input) pin				

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

  Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

10. Pin Connection

- Treatment of unused pins
  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

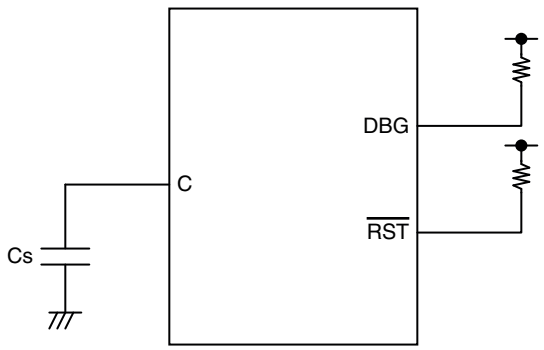
- Power supply pins
  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin
  Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.
  After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.
  The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

- $\overline{RST}$ pin
  Connect the $\overline{RST}$ pin to an external pull-up resistor of 2 kΩ or above.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{RST}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.
  The PF2/$\overline{RST}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{RST}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

- C pin
  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/$\overline{RST}$/C pins connection diagram



Address	Register abbreviation	Register name	R/W	Initial value
0x0055	ECCR	LIN-UART extended communication control register	R/W	0b000000XX
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I²C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I²C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I²C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I²C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I²C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I²C clock control register ch. 0	R/W	0b00000000
0x0066	OPCUR	16-bit MPG output control register (upper)	R/W	0b00000000
0x0067	OPCLR	16-bit MPG output control register (lower)	R/W	0b00000000
0x0068	IPCUR	16-bit MPG input control register (upper)	R/W	0b00000000
0x0069	IPCLR	16-bit MPG input control register (lower)	R/W	0b00000000
0x006A	NCCR	16-bit MPG noise cancellation control register	R/W	0b00000000
0x006B	TCSR	16-bit MPG timer control status register	R/W	0b00000000
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	—	(Disabled)	—	—
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111

Address	Register abbreviation	Register name	R/W	Initial value
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0FA6	PPS21	8/16-bit PPG21 cycle setting buffer register	R/W	0b11111111
0x0FA7	PPS20	8/16-bit PPG20 cycle setting buffer register	R/W	0b11111111
0x0FA8	TMRH1	16-bit reload timer timer register (upper) ch. 1	R/W	0b00000000
	TMRLRH1	16-bit reload timer reload register (upper) ch. 1		
0x0FA9	TMRL1	16-bit reload timer timer register (lower) ch. 1	R/W	0b00000000
	TMRLRL1	16-bit reload timer reload register (lower) ch. 1		
0x0FAA	PDS21	8/16-bit PPG21 duty setting buffer register	R/W	0b11111111
0x0FAB	PDS20	8/16-bit PPG20 duty setting buffer register	R/W	0b11111111
0x0FAC to 0x0FAF	—	(Disabled)	—	—
0x0FB0	PDCRH1	16-bit PPG downcounter register (upper) ch. 1	R	0b00000000
0x0FB1	PDCRL1	16-bit PPG downcounter register (lower) ch. 1	R	0b00000000
0x0FB2	PCSRH1	16-bit PPG cycle setting buffer register (upper) ch. 1	R/W	0b11111111
0x0FB3	PCSRL1	16-bit PPG cycle setting buffer register (lower) ch. 1	R/W	0b11111111
0x0FB4	PDUTH1	16-bit PPG duty setting buffer register (upper) ch. 1	R/W	0b11111111
0x0FB5	PDUTL1	16-bit PPG duty setting buffer register (lower) ch. 1	R/W	0b11111111
0x0FB6 to 0x0FBB	—	(Disabled)	—	—
0x0FBC	BGR1	LIN-UART baud rate generator register 1	R/W	0b00000000
0x0FBD	BGR0	LIN-UART baud rate generator register 0	R/W	0b00000000
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FC0, 0x0FC1	—	(Disabled)	—	—
0x0FC2	AIDRH	A/D input disable register (upper)	R/W	0b00000000
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4	OPDBRH0	16-bit MPG output data buffer register (upper) ch. 0	R/W	0b00000000
0x0FC5	OPDBRL0	16-bit MPG output data buffer register (lower) ch. 0	R/W	0b00000000
0x0FC6	OPDBRH1	16-bit MPG output data buffer register (upper) ch. 1	R/W	0b00000000
0x0FC7	OPDBRL1	16-bit MPG output data buffer register (lower) ch. 1	R/W	0b00000000
0x0FC8	OPDBRH2	16-bit MPG output data buffer register (upper) ch. 2	R/W	0b00000000
0x0FC9	OPDBRL2	16-bit MPG output data buffer register (lower) ch. 2	R/W	0b00000000
0x0FCA	OPDBRH3	16-bit MPG output data buffer register (upper) ch. 3	R/W	0b00000000
0x0FCB	OPDBRL3	16-bit MPG output data buffer register (lower) ch. 3	R/W	0b00000000
0x0FCC	OPDBRH4	16-bit MPG output data buffer register (upper) ch. 4	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0FCD	OPDBRL4	16-bit MPG output data buffer register (lower) ch. 4	R/W	0b00000000
0x0FCE	OPDBRH5	16-bit MPG output data buffer register (upper) ch. 5	R/W	0b00000000
0x0FCF	OPDBRL5	16-bit MPG output data buffer register (lower) ch. 5	R/W	0b00000000
0x0FD0	OPDBRH6	16-bit MPG output data buffer register (upper) ch. 6	R/W	0b00000000
0x0FD1	OPDBRL6	16-bit MPG output data buffer register (lower) ch. 6	R/W	0b00000000
0x0FD2	OPDBRH7	16-bit MPG output data buffer register (upper) ch. 7	R/W	0b00000000
0x0FD3	OPDBRL7	16-bit MPG output data buffer register (lower) ch. 7	R/W	0b00000000
0x0FD4	OPDBRH8	16-bit MPG output data buffer register (upper) ch. 8	R/W	0b00000000
0x0FD5	OPDBRL8	16-bit MPG output data buffer register (lower) ch. 8	R/W	0b00000000
0x0FD6	OPDBRH9	16-bit MPG output data buffer register (upper) ch. 9	R/W	0b00000000
0x0FD7	OPDBRL9	16-bit MPG output data buffer register (lower) ch. 9	R/W	0b00000000
0x0FD8	OPDBRHA	16-bit MPG output data buffer register (upper) ch. A	R/W	0b00000000
0x0FD9	OPDBRLA	16-bit MPG output data buffer register (lower) ch. A	R/W	0b00000000
0x0FDA	OPDBRHB	16-bit MPG output data buffer register (upper) ch. B	R/W	0b00000000
0x0FDB	OPDBRLB	16-bit MPG output data buffer register (lower) ch. B	R/W	0b00000000
0x0FDC	OPDUR	16-bit MPG output data register (upper)	R	0b0000XXXX
0x0FDD	OPDLR	16-bit MPG output data register (lower)	R	0bXXXXXXXX
0x0FDE	CPCUR	16-bit MPG compare clear register (upper)	R/W	0bXXXXXXXX
0x0FDF	CPCLR	16-bit MPG compare clear register (lower)	R/W	0bXXXXXXXX
0x0FE0	LVDPW	LVD reset circuit password register	R/W	0b00000000
0x0FE1	—	(Disabled)	—	—
0x0FE2	TMBUR	16-bit MPG timer buffer register (upper)	R	0bXXXXXXXX
0x0FE3	TMBLR	16-bit MPG timer buffer register (lower)	R	0bXXXXXXXX
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000

17. I/O Ports

- List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 4 data register	PDR4	R, RM/W	0b00000000
Port 4 direction register	DDR4	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 7 data register	PDR7	R, RM/W	0b00000000
Port 7 direction register	DDR7	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 0 pull-up register	PUL0	R/W	0b00000000
Port 1 pull-up register	PUL1	R/W	0b00000000
Port 4 pull-up register	PUL4	R/W	0b00000000
Port 6 pull-up register	PUL6	R/W	0b00000000
Port 7 pull-up register	PUL7	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (upper)	AIDRH	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

corresponding bit in the PUL0 register to “0”.

- Operation as an external interrupt input pin
  - Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

- Operation of the pull-up register
  Setting the bit in the PUL0 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL0 register.

- Operation as a comparator input pin (only for P00 and P03)
  - Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
  - Regardless of the value of the PDR0 register and that of the DDR0 register, if the comparator analog input enable bit in the comparator control register ch. 0/ch. 1 (CMR0/CMR1:VCID) is set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit to “1”.
  - For details of the comparator, refer to “CHAPTER 28 COMPARATOR” in “New 8FX MB95690K Series Hardware Manual”.

- Operation as a comparator input pin (only for P01 and P04)
  - Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
  - Regardless of the value of the PDR0 register and that of the DDR0 register, if the comparator analog input enable bit (VCID) and the negative analog input voltage source select bit (BGRS) in the comparator control register ch. 0/ch. 1 (CMR0/CMR1) are both set to “0”, the comparator input function is enabled.
  - To disable the comparator input function, set the VCID bit or the BGRS bit to “1”.
  - For details of the comparator, refer to “CHAPTER 28 COMPARATOR” in “New 8FX MB95690K Series Hardware Manual”.

17.2.4 Port 1 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
  - If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR1 register returns the PDR1 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

17.3 Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95690K Series Hardware Manual”.

17.3.1 Port 4 configuration

Port 4 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 4 data register (PDR4)
- Port 4 direction register (DDR4)
- Port 4 pull-up register (PUL4)
- A/D input disable register (upper) (AIDRH)

17.3.2 Block diagrams of port 4

- P40/AN08 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN08)

- P41/AN09 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN09)

- P42/AN10 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN10)

- P43/AN11 pin

  This pin has the following peripheral function:
  - 8/10-bit A/D converter analog input pin (AN11)

17.3.3 Port 4 registers

- Port 4 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR4	0	Pin state is “L” level.	PDR4 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR4 value is “1”.	As output port, outputs “H” level.
DDR4	0	Port input enabled		
	1	Port output enabled		
PUL4	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRH	0	Analog input enabled		
	1	Port input enabled		

- Correspondence between registers and pins for port 4

	Correspondence between related register bits and pins							
Pin name	**P47**	**P46**	**P45**	**P44**	**P43**	**P42**	**P41**	**P40**
PDR4	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR4								
PUL4								
AIDRH	-	-	-	-				

17.3.4 Port 4 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
  - If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR4 register returns the PDR4 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When using a pin shared with the analog input function as an input port, set the corresponding bit in the A/D input disable register (upper) (AIDRH) to “1”
  - If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR4 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR4 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

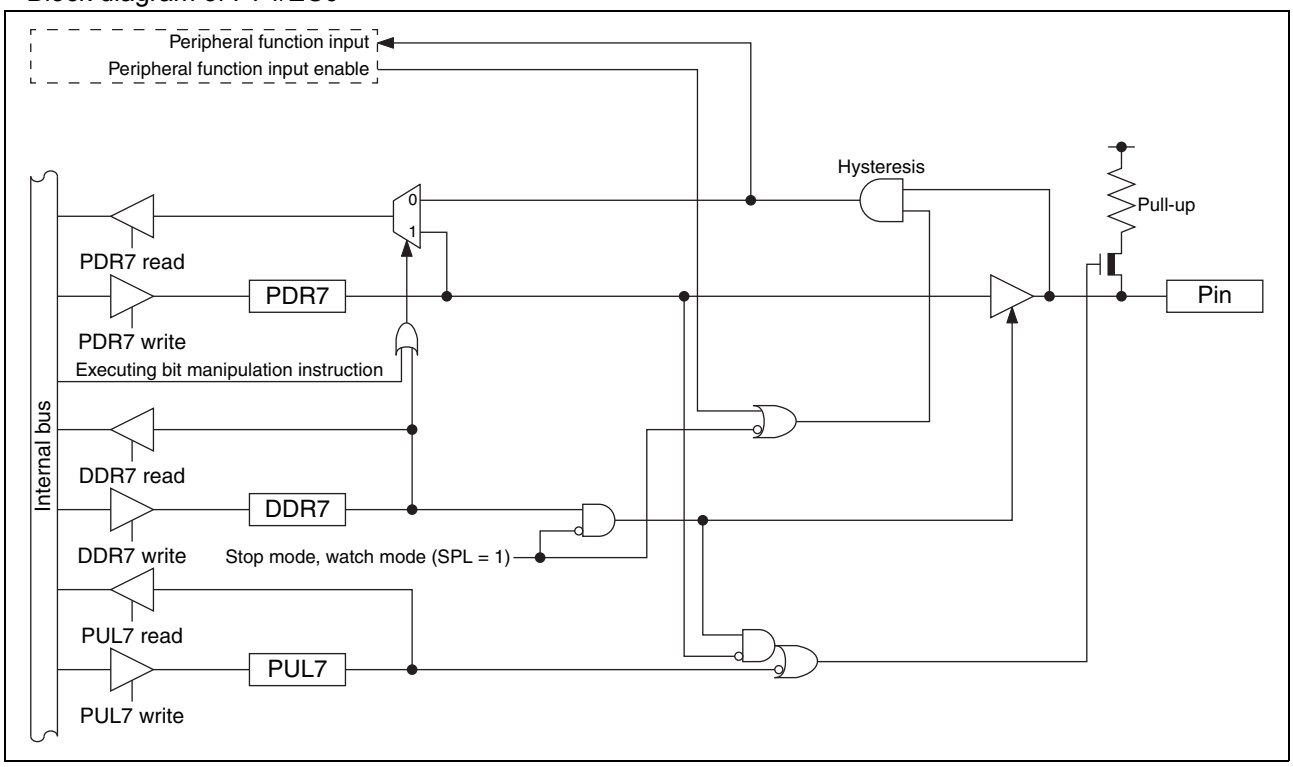
- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR4 register corresponding to the input pin of a peripheral function to “0”.
  - When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRH register corresponding to that pin to “1”.
  - Reading the PDR4 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRH register is initialized to “0”.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P45/SCK and P47/SIN is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation as an analog input pin
  - Set the bit in the DDR4 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRH register to “0”.

- Block diagram of P74/EC0



17.5.4 Port 7 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR7 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR7 register to external pins.
  - If data is written to the PDR7 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR7 register returns the PDR7 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR7 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR7 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR7 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR7 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR7 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR7 register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDR7 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P74/EC0, P75/UCK0 and P77/UI0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

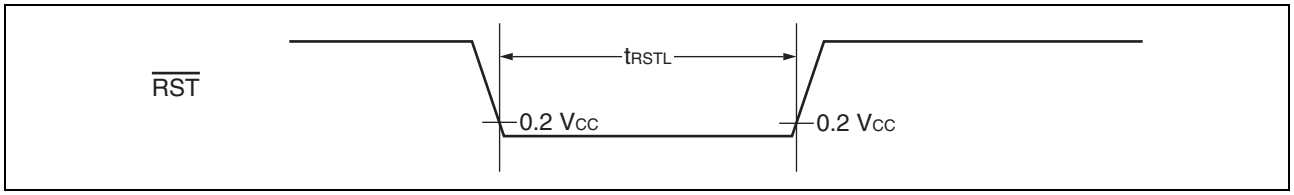
- Operation of the pull-up register
  Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

20.4.3 External Reset

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

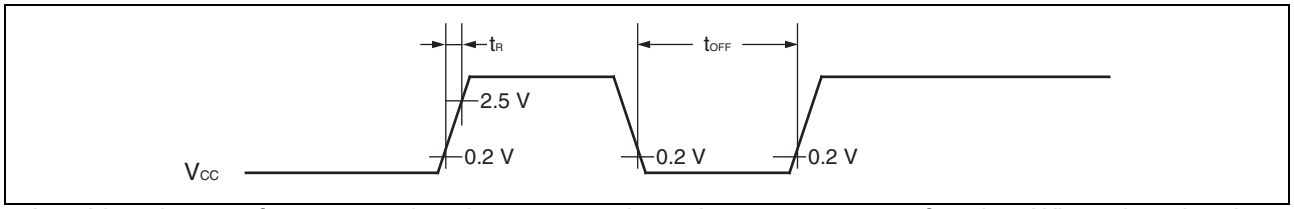
*: See "Source Clock/Machine Clock" for t_{MCLK}.



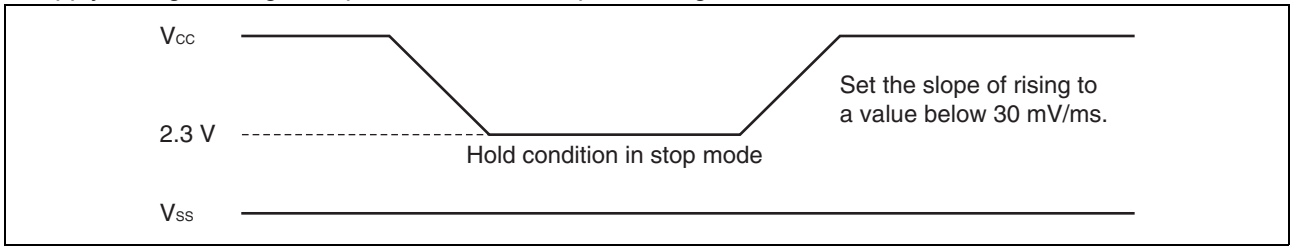
20.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

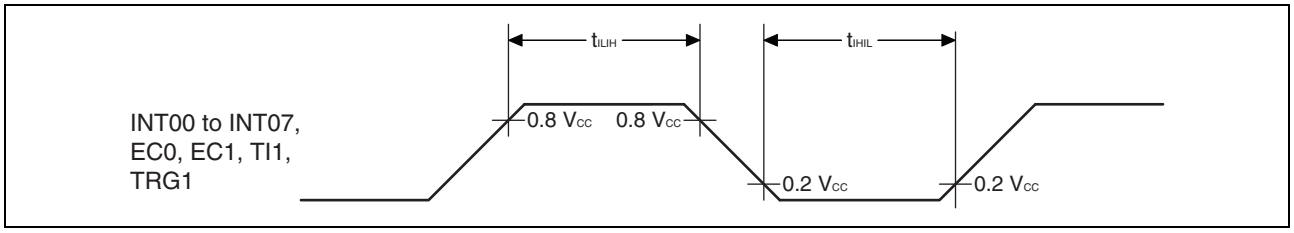


20.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, TI1, TRG1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



20.4.6 LIN-UART Timing

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		30	—	ns
SCK↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.
*3: See “Source Clock/Machine Clock” for t_{MCLK}.

Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

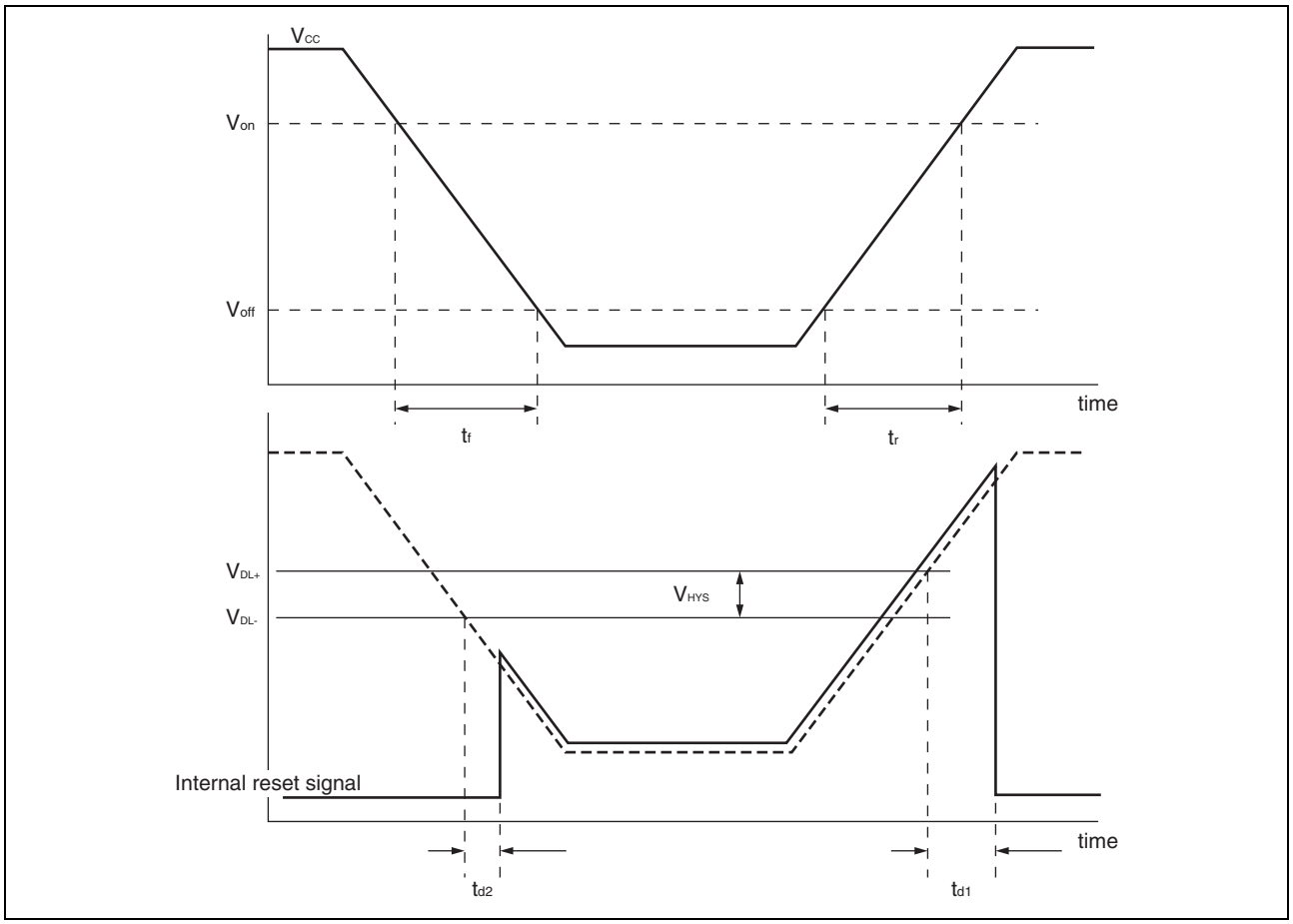
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK, SIN		30	—	ns
SCK↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.


V_{CC}
V_{on}
V_{off}
time
t_f
t_r
V_{DL+}
V_{DL-}
V_{HYS}
Internal reset signal
time
t_{d2}
t_{d1}

20.4.11 Comparator Timing

(V_{CC} = 2.88 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Voltage range	CMP0_P, CMP0_N, CMP1_P, CMP1_N	0	—	V_{CC} – 1.3	V	
Offset voltage	CMP0_P, CMP0_N, CMP1_P, CMP1_N	–15	—	+15	mV	
Delay time	CMP0_O, CMP1_O	—	650	1200	ns	Overdrive 5 mV
		—	140	420	ns	Overdrive 50 mV
Power down delay	CMP0_O, CMP1_O	—	—	1200	ns	Power down recovery PD: 1 → 0
Power up stabilization wait time	CMP0_O, CMP1_O	—	—	1200	ns	Output stabilization wait time at power up

20.4.12 BGR for Comparator

(V_{CC} = 2.88 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power up stabilization wait time	—	—	—	150	µs	Load: 10 pF
Output voltage	VBGR	1.1495	1.21	1.2705	V	