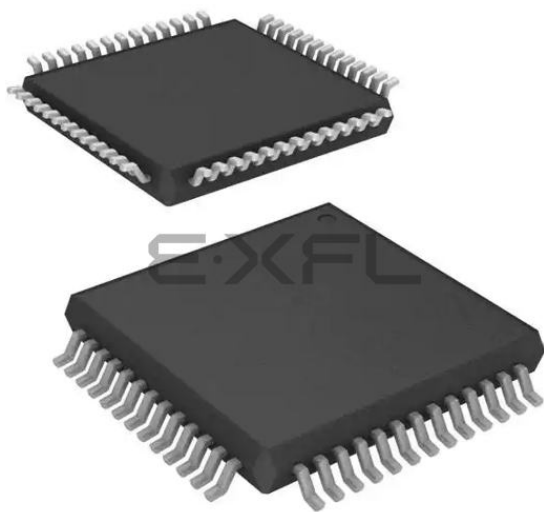




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f698kpmc1-g-sne2

New 8FX 8-bit Microcontrollers

The MB95690K Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral functions.

Features

■ F²MC-8FX CPU core

- Instruction set optimized for controllers
 - Multiplication and division instructions
 - 16-bit arithmetic operations
 - Bit test branch instructions
 - Bit manipulation instructions, etc.

■ Clock

- Selectable main clock source
 - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
 - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
 - Main CR clock (4 MHz $\pm$ 2%)
 - Main CR PLL clock
 - The main CR PLL clock frequency becomes 8 MHz $\pm$ 2% when the PLL multiplication rate is 2.
 - The main CR PLL clock frequency becomes 10 MHz $\pm$ 2% when the PLL multiplication rate is 2.5.
 - The main CR PLL clock frequency becomes 12 MHz $\pm$ 2% when the PLL multiplication rate is 3.
 - The main CR PLL clock frequency becomes 16 MHz $\pm$ 2% when the PLL multiplication rate is 4.
- Selectable subclock source
 - Suboscillation clock (32.768 kHz)
 - External clock (32.768 kHz)
 - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

■ Timer

- 8/16-bit composite timer $\times$ 2 channels
- 8/16-bit PPG $\times$ 3 channels
- 16-bit PPG timer $\times$ 1 channel (can work independently or together with the multi-pulse generator)
- 16-bit reload timer $\times$ 1 channel (can work independently or together with the multi-pulse generator)
- Time-base timer $\times$ 1 channel
- Watch prescaler $\times$ 1 channel

■ UART/SIO $\times$ 1 channel

- Full duplex double buffer
- Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer

■ I²C bus interface $\times$ 1 channel

- Built-in wake-up function

■ Multi-pulse generator (MPG) (for DC motor control) $\times$ 1 channel

- 16-bit reload timer $\times$ 1 channel
- 16-bit PPG timer $\times$ 1 channel

- Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)

■ LIN-UART

- Full duplex double buffer
- Capable of clock asynchronous serial data transfer and clock synchronous serial data transfer

■ External interrupt

- LQF044: 7 channels
- LQA048, LQC052, WNR048: 8 channels
- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

■ 8/10-bit A/D converter

- LQF044: 8 channels
- LQA048, LQC052, WNR048: 12 channels
- 8-bit or 10-bit resolution can be selected.

■ Low power consumption (standby) modes

- There are four standby modes as follows:
 - Stop mode
 - Sleep mode
 - Watch mode
 - Time-base timer mode
- In standby mode, two further options can be selected: normal standby mode and deep standby mode.

■ I/O port

- LQF044 (number of I/O ports: 41)
 - General-purpose I/O ports (CMOS I/O):37
 - General-purpose I/O ports (N-ch open drain):4
- LQA048, LQC052, WNR048 (number of I/O ports: 45)
 - General-purpose I/O ports (CMOS I/O):41
 - General-purpose I/O ports (N-ch open drain):4

■ On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

■ Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

■ Power-on reset

- A power-on reset is generated when the power is switched on.

■ Low-voltage detection (LVD) reset circuit

- The LVD function is enabled by default. For details, see "20.2 Recommended Operating Conditions" in "Electrical Characteristics".
- The LVD function can be controlled through software.

Contents

Features.....	1	15. Areas For Specific Applications	34
1. Product Line-up	4	16. I/O Map.....	35
2. Packages And Corresponding Products.....	6	17. I/O Ports.....	42
3. Differences Among Products And Notes On Product Selection	7	17.1 Port 0.....	43
4. Pin Assignment	8	17.2 Port 1.....	50
5. Pin Functions (LQF044)	12	17.3 Port 4.....	55
6. Pin Functions (LQA048, LQC052, WNR048)	16	17.4 Port 6.....	62
7. I/O Circuit Type	21	17.5 Port 7.....	67
8. Handling Precautions.....	23	17.6 Port F.....	74
8.1 Precautions for Product Design.....	23	17.7 Port G.....	77
8.2 Precautions for Package Mounting	24	18. Interrupt Source Table	80
8.3 Precautions for Use Environment.....	26	19. Pin States In Each Mode	81
9. Notes On Device Handling.....	26	20. Electrical Characteristics.....	84
10. Pin Connection	27	20.1 Absolute Maximum Ratings.....	84
11. Block Diagram (LQF044)	29	20.2 Recommended Operating Conditions	86
12. Block Diagram (LQA048, LQC052, WNR048)	30	20.3 DC Characteristics	87
13. CPU Core.....	31	20.4 AC Characteristics.....	90
14. Memory Space	32	20.5 A/D Converter.....	109
14.1 I/O area (addresses: 0x0000 to 0x007F).....	32	20.6 Flash Memory Program/Erase Characteristics	113
14.2 Extended I/O area		21. Sample Characteristics.....	114
(addresses: 0x0F80 to 0x0FFF).....	32	22. Ordering Information.....	121
14.3 Data area.....	32	23. Package Dimension.....	122
14.4 Program area	32	24. Major Changes In This Edition	126
14.5 Memory space map.....	33	Document History Page	127
		Sales, Solutions, and Legal Information	129

1. Product Line-up

Part number	MB95F694K	MB95F696K	MB95F698K
Parameter			
Type	Flash memory product		
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.		
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	512 bytes	1 Kbyte	2 Kbyte
Power-on reset	Yes		
Low-voltage detection reset	Controlled through software		
Reset input	Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz)		
General-purpose I/O	• LQF044 - I/O port : 41 - CMOS I/O : 37 - N-ch open drain : 4 • LQA048, LQC052, WNR048 - I/O port : 45 - CMOS I/O : 41 - N-ch open drain : 4		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)		
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the software watchdog timer.		
Wild register	It can be used to replace 3 bytes of data.		
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled. • The LIN function can be used as a LIN master or a LIN slave.		
8/10-bit A/D converter	• LQF044: 8 channels • LQA048, LQC052, WNR048: 12 channels 8-bit or 10-bit resolution can be selected.		

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
LQFP48*1, QFN48*2	LQFP52*3				Input	Output	OD*5	PU*6
41	44	P04	E	General-purpose I/O port	CMOS/ analog	CMOS	—	O
		INT04		External interrupt input pin				
		AN04		8/10-bit A/D converter analog input pin				
		CMP1_N		Comparator ch. 1 inverting analog input (negative input) pin				
42	45	P05	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT05		External interrupt input pin				
		AN05		8/10-bit A/D converter analog input pin				
		CMP1_O		Comparator ch. 1 digital output pin				
—	46	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
43	47	P06	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT06		External interrupt input pin				
		AN06		8/10-bit A/D converter analog input pin				
44	48	P07	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT07		External interrupt input pin				
		AN07		8/10-bit A/D converter analog input pin				
45	49	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
		RST		Reset pin				
46	50	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X0		Main clock input oscillation pin				
47	51	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X1		Main clock I/O oscillation pin				
48	52	Vss	—	Power supply pin (GND)	—	—	—	—

O: Available

*1: LQA048

*2: WNR048

*3: LQC052

*4: For the I/O circuit types, see "I/O Circuit Type".

*5: N-ch open drain

*6: Pull-up

- **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- **Lead-Free Packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

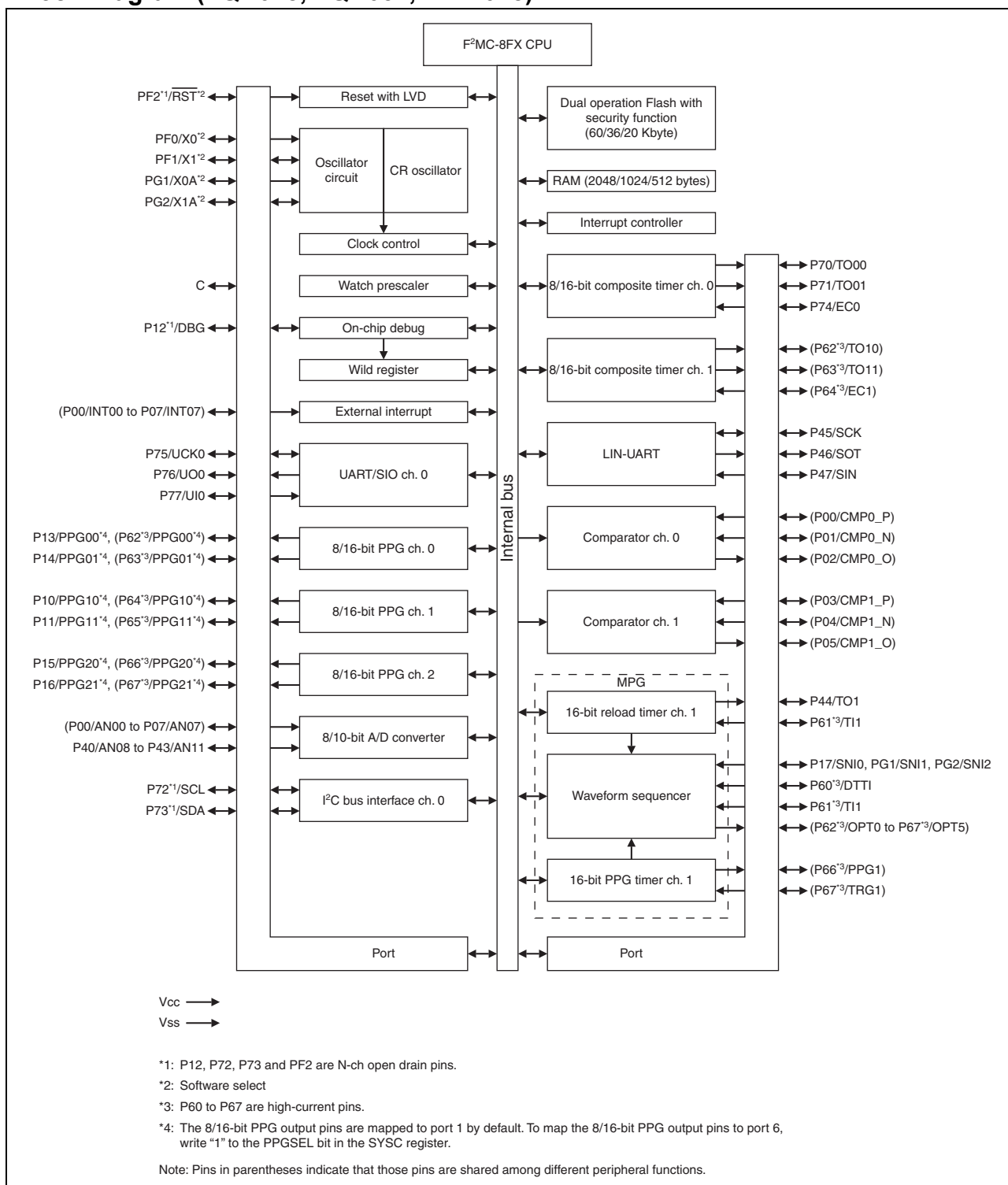
Condition: 125°C/24 h

- **Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

12. Block Diagram (LQA048, LQC052, WNR048)

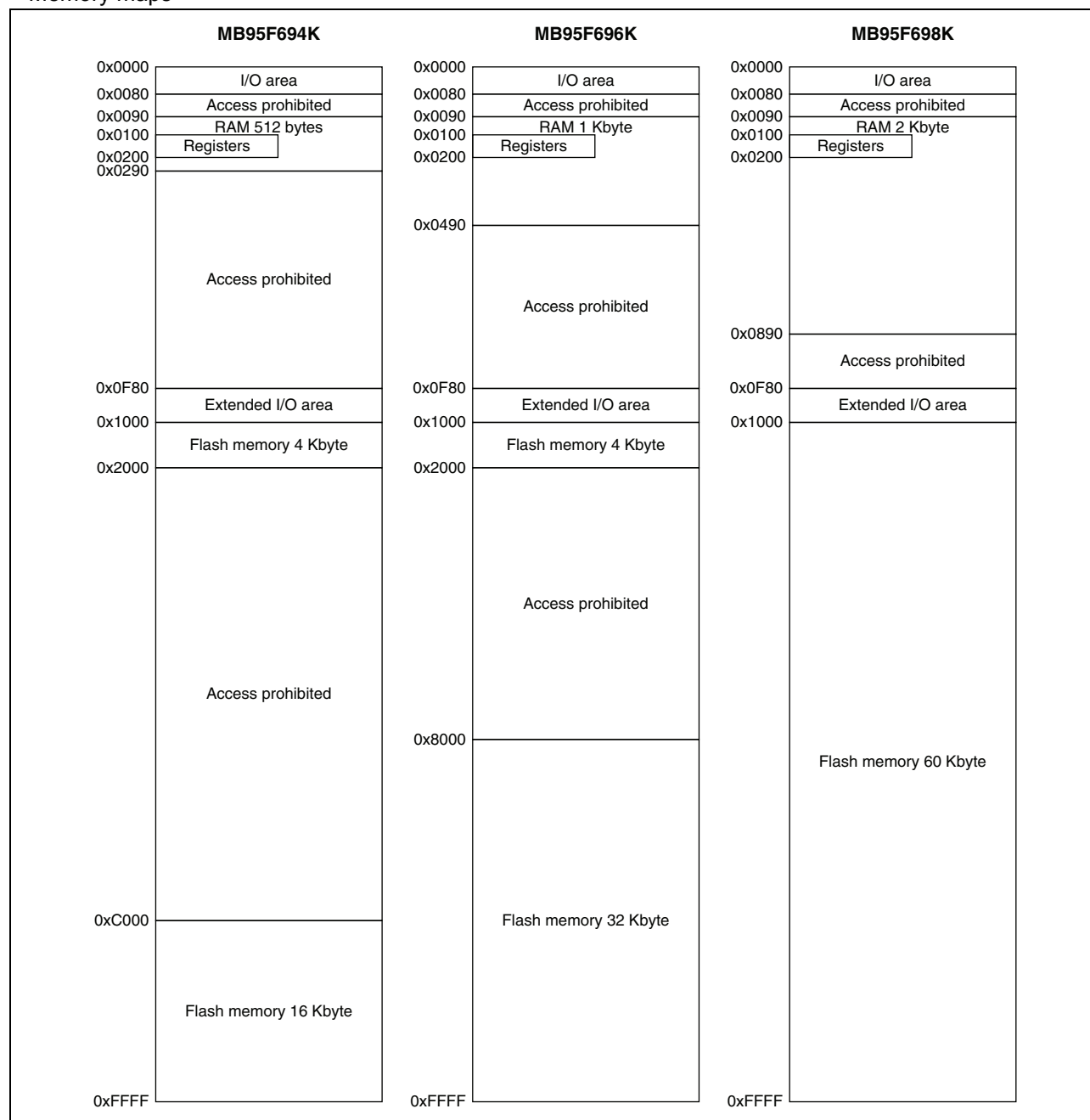


13. CPU Core

- Memory space

The memory space of the MB95690K Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95690K Series are shown below.

- Memory maps

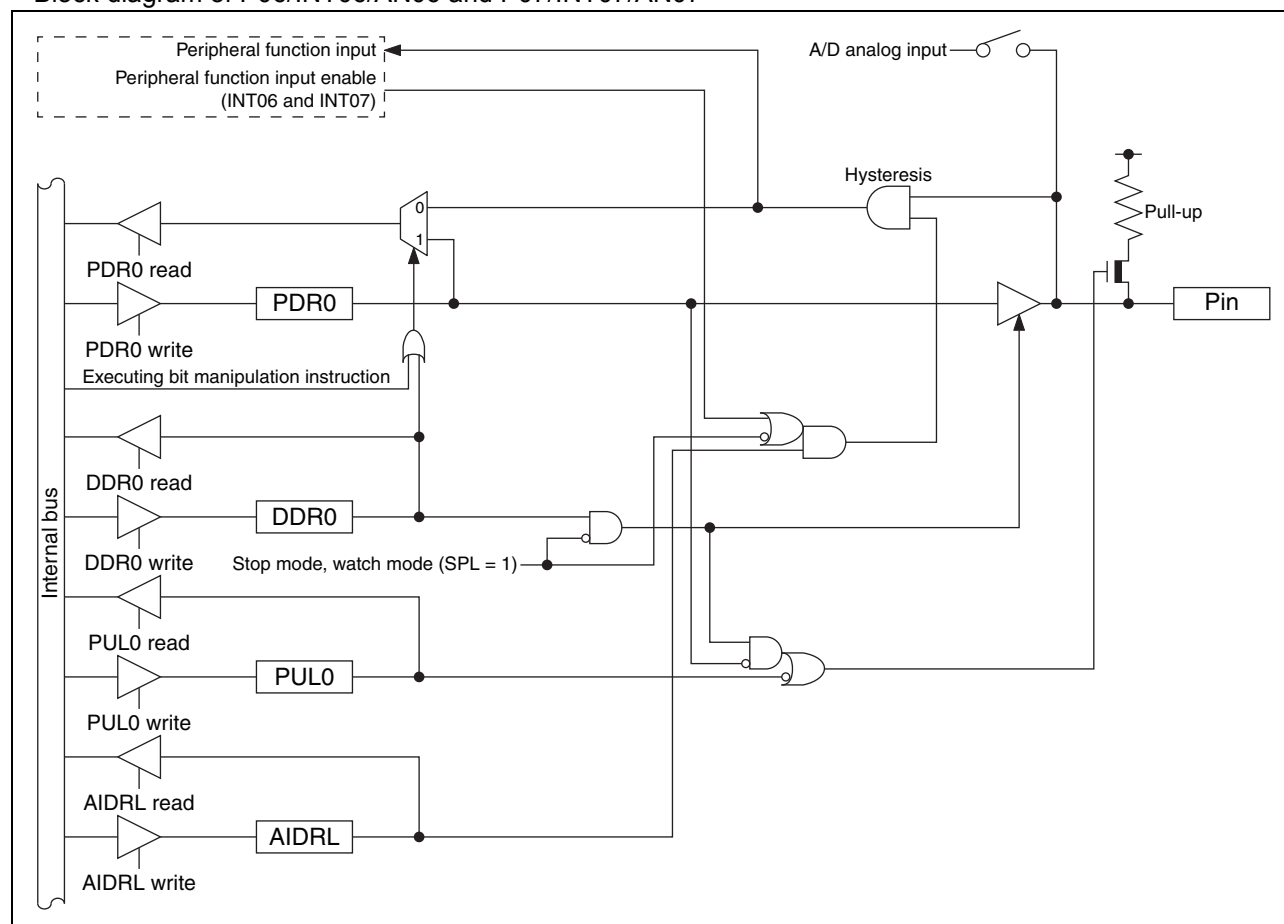


Address	Register abbreviation	Register name	R/W	Initial value
0x0030	PUL4	Port 4 pull-up register	R/W	0b00000000
0x0031	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0032	PUL7	Port 7 pull-up register	R/W	0b00000000
0x0033, 0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	PC21	8/16-bit PPG timer 21 control register	R/W	0b00000000
0x003F	PC20	8/16-bit PPG timer 20 control register	R/W	0b00000000
0x0040	TMCSRH1	16-bit reload timer control status register (upper) ch. 1	R/W	0b00000000
0x0041	TMCSRL1	16-bit reload timer control status register (lower) ch. 1	R/W	0b00000000
0x0042	CMR0	Comparator control register ch. 0	R/W	0b11000101
0x0043	CMR1	Comparator control register ch. 1	R/W	0b11000101
0x0044	PCNTH1	16-bit PPG status control register (upper)	R/W	0b00000000
0x0045	PCNTL1	16-bit PPG status control register (lower)	R/W	0b00000000
0x0046, 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	—	(Disabled)	—	—
0x004E	LVDR	LVD reset voltage selection ID register	R/W	0b00000000
0x004F	LVDCC	LVD reset circuit control register	R/W	0b00000001
0x0050	SCR	LIN-UART serial control register	R/W	0b00000000
0x0051	SMR	LIN-UART serial mode register	R/W	0b00000000
0x0052	SSR	LIN-UART serial status register	R/W	0b00001000
0x0053	RDR	LIN-UART receive data register	R/W	0b00000000
	TDR	LIN-UART transmit data register		
0x0054	ESCR	LIN-UART extended status control register	R/W	0b00000100

- P06/INT06/AN06 pin
 - This pin has the following peripheral functions:
 - External interrupt input pin (INT06)
 - 8/10-bit A/D converter analog input pin (AN06)

- P07/INT07/AN07 pin
 - This pin has the following peripheral functions:
 - External interrupt input pin (INT07)
 - 8/10-bit A/D converter analog input pin (AN07)

- Block diagram of P06/INT06/AN06 and P07/INT07/AN07



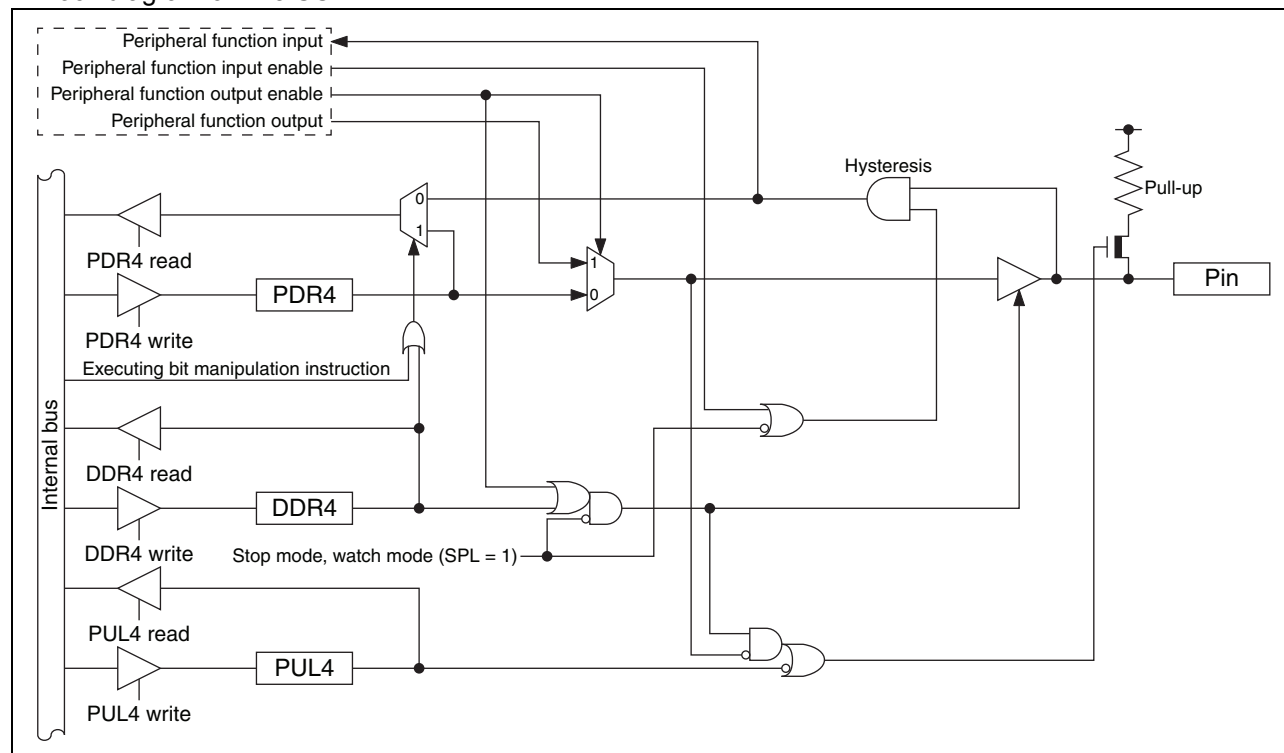
17.1.4 Port 0 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
 - If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR0 register returns the PDR0 register value.
- Operation as an input port
 - A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When using a pin shared with the analog input function as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to “1”.
 - If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
- Operation as a peripheral function output pin
 - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
 - The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
- Operation as a peripheral function input pin
 - To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
 - When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
 - Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.
- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT00 to INT07), the input is enabled and not blocked.
 - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation as an analog input pin
 - Set the bit in the DDR0 register bit corresponding to the analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the

- P45/SCK pin
This pin has the following peripheral functions:
 - LIN-UART clock I/O pin (SCK)

- Block diagram of P45/SCK



- P47/SIN pin
This pin has the following peripheral function:
 - LIN-UART data input pin (SIN)

- For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL4 register to “0”.
- Operation of the pull-up register
 Setting the bit in the PUL4 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL4 register.

17.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95690K Series Hardware Manual”.

17.4.1 Port 6 configuration

Port 6 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)
- Port 6 pull-up register (PUL6)

17.4.2 Block diagrams of port 6

- P60/DTTI pin

This pin has the following peripheral function:

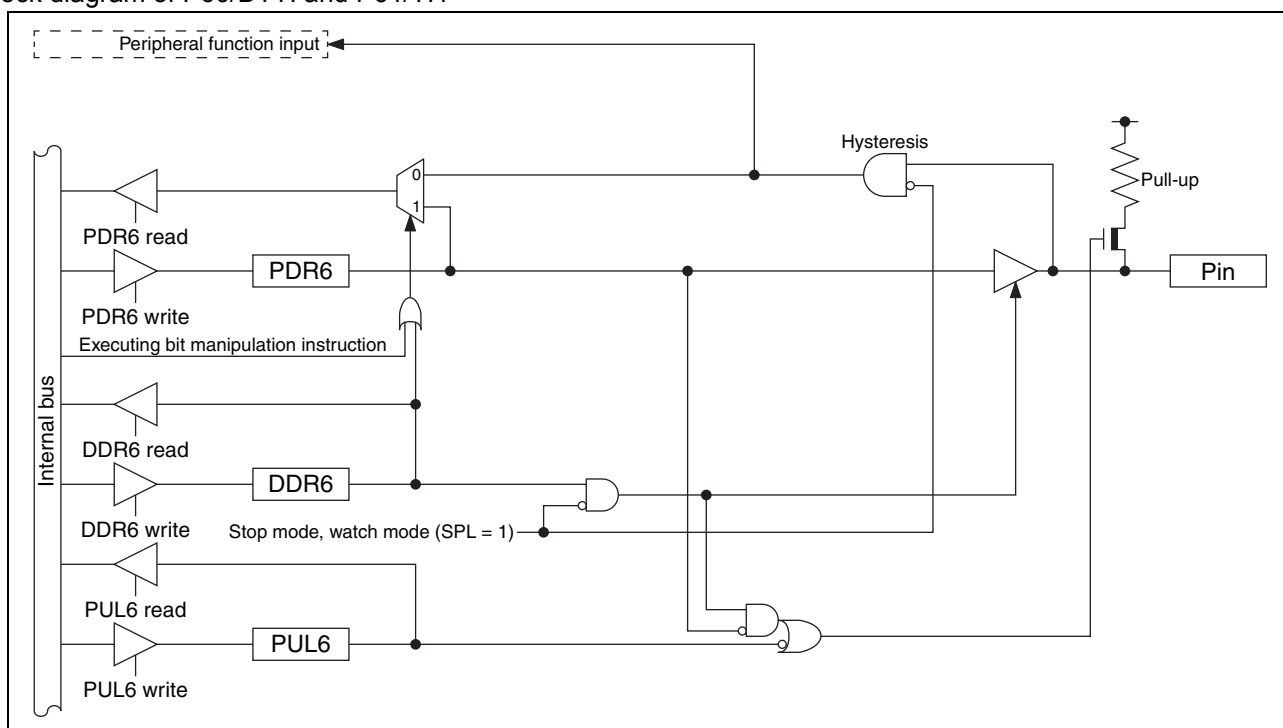
- MPG waveform sequencer input pin (DTTI)

- P61/TI1 pin

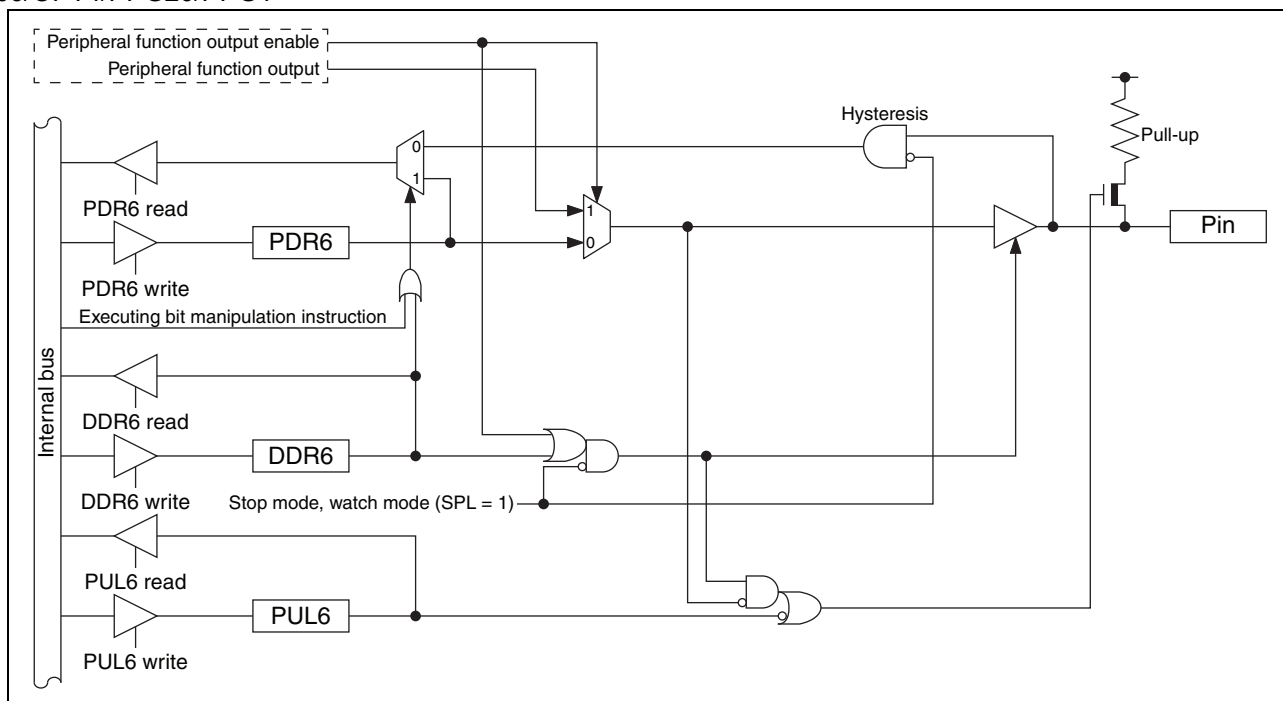
This pin has the following peripheral function:

- 16-bit reload timer ch. 1 input pin (TI1)

- Block diagram of P60/DTTI and P61/TI1



- P62/OPT0/PPG00/TO10 pin
This pin has the following peripheral functions:
 - MPG waveform sequencer output pin (OPT0)
 - 8/16-bit PPG ch. 0 output pin (PPG00)
 - 8/16-bit composite timer ch. 1 output pin (TO10)
- P63/OPT1/PPG01/TO11 pin
This pin has the following peripheral functions:
 - MPG waveform sequencer output pin (OPT1)
 - 8/16-bit PPG ch. 0 output pin (PPG01)
 - 8/16-bit composite timer ch. 1 output pin (TO11)
- P65/OPT3/PPG11 pin
This pin has the following peripheral functions:
 - MPG waveform sequencer output pin (OPT3)
 - 8/16-bit PPG ch. 1 output pin (PPG11)
- P66/OPT4/PPG20/PPG1 pin
This pin has the following peripheral functions:
 - MPG waveform sequencer output pin (OPT4)
 - 8/16-bit PPG ch. 2 output pin (PPG20)
 - 16-bit PPG timer ch. 1 output pin (PPG1)
- Block diagram of P62/OPT0/PPG00/TO10, P63/OPT1/PPG01/TO11, P65/OPT3/PPG11 and P66/OPT4/PPG20/PPG1



17.4.3 Port 6 registers

- Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is "L" level.	PDR6 value is "0".	As output port, outputs "L" level.
	1	Pin state is "H" level.	PDR6 value is "1".	As output port, outputs "H" level.
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		

- Correspondence between registers and pins for port 6

	Correspondence between related register bits and pins							
Pin name	P67	P66	P65	P64	P63	P62	P61	P60
PDR6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR6								
PUL6								

17.5.3 Port 7 registers

- Port 7 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR7	0	Pin state is "L" level.	PDR7 value is "0".	As output port, outputs "L" level.
	1	Pin state is "H" level.	PDR7 value is "1".	As output port, outputs "H" level.*
DDR7	0	Port input enabled		
	1	Port output enabled		
PUL7	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 7

	Correspondence between related register bits and pins							
Pin name	P77	P76	P75	P74	P73	P72	P71	P70
PDR7	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR7								
PUL7					-	-		

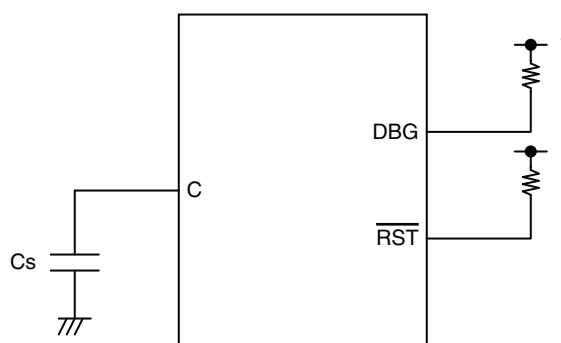
20.2 Recommended Operating Conditions

 (V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V _{CC}	2.88	5.5	V	
Decoupling capacitor	C _s	0.022	1	μF	*
Operating temperature	T _A	-40	+85	°C	Other than on-chip debug mode
		+5	+35		On-chip debug mode

- *: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_s. For the connection to a decoupling capacitor C_s, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_s and the distance between C_s and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG / $\overline{\text{RST}}$ / C pins connection diagram



- *: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at "L" level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

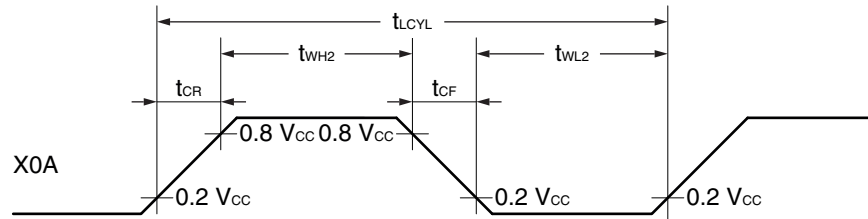
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

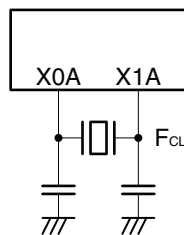
No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

- Input waveform generated when an external clock (subclock) is used

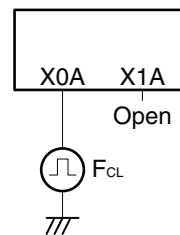


- Figure of subclock input port external connection

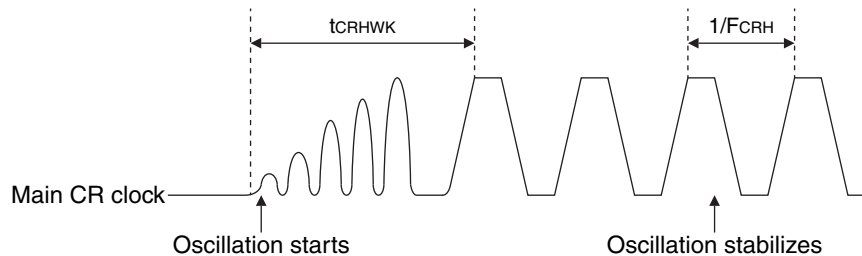
When a crystal oscillator or a ceramic oscillator is used



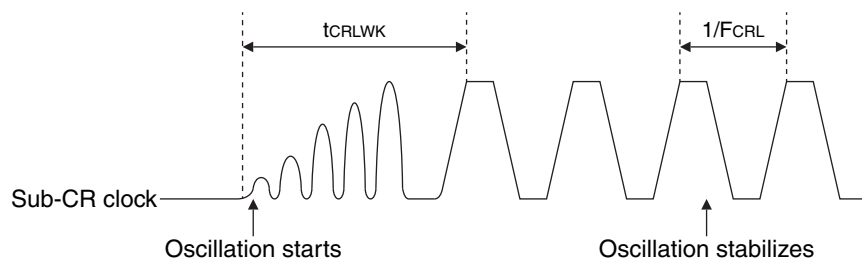
When an external clock is used



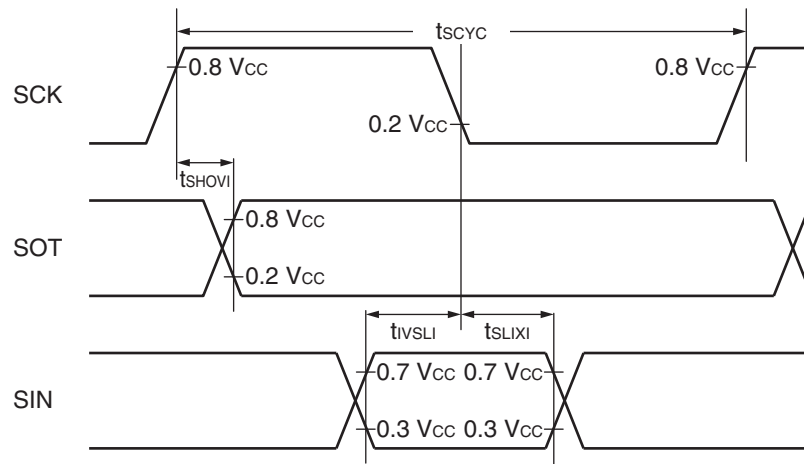
- Input waveform generated when an internal clock (main CR clock) is used



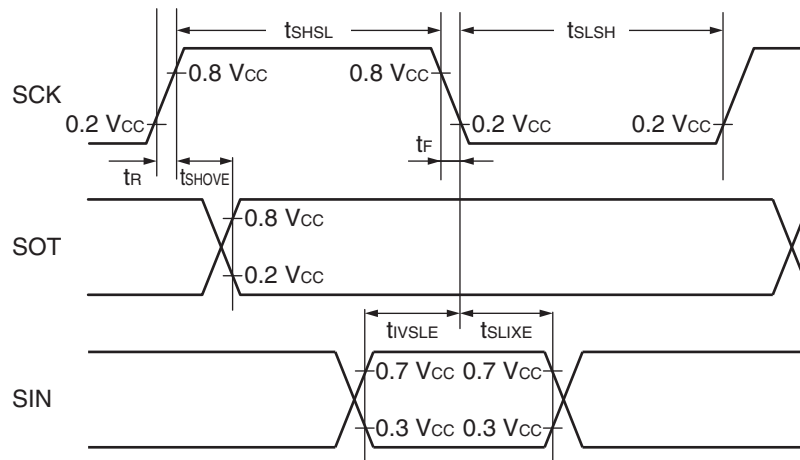
- Input waveform generated when an internal clock (sub-CR clock) is used

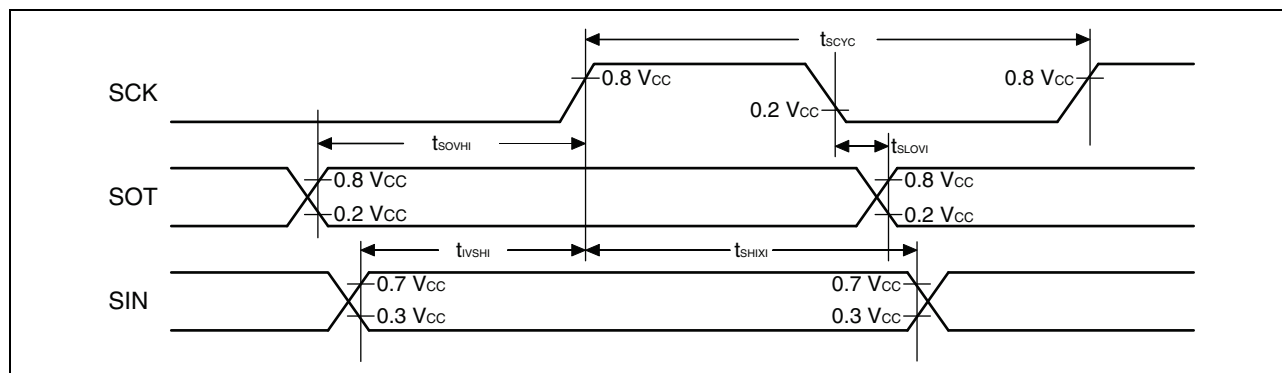


- Internal shift clock mode



- External shift clock mode





20.4.7 Low-voltage Detection

($V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage*	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
		2.61	2.8	2.99		
		2.89	3.1	3.31		
		3.08	3.3	3.52		
Detection voltage*	V_{DL-}	2.43	2.6	2.77	V	At power supply fall
		2.52	2.7	2.88		
		2.80	3	3.20		
		2.99	3.2	3.41		
Hysteresis width	V_{HYS}	—	—	100	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	650	—	—	μs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	650	—	—	μs	Slope of power supply that the reset release signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	30	μs	
Reset detection delay time	t_{d2}	—	—	30	μs	
LVD reset threshold voltage transition stabilization time	t_{stb}	10	—	—	μs	

*: After the LVD reset is enabled by the LVD reset circuit control register (LVDCC), the release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDCC register and the LVDR register, refer to "CHAPTER 16 LOW-VOLTAGE DETECTION RESET CIRCUIT" in "New 8FX MB95690K Series Hardware Manual".

• Input voltage characteristics

