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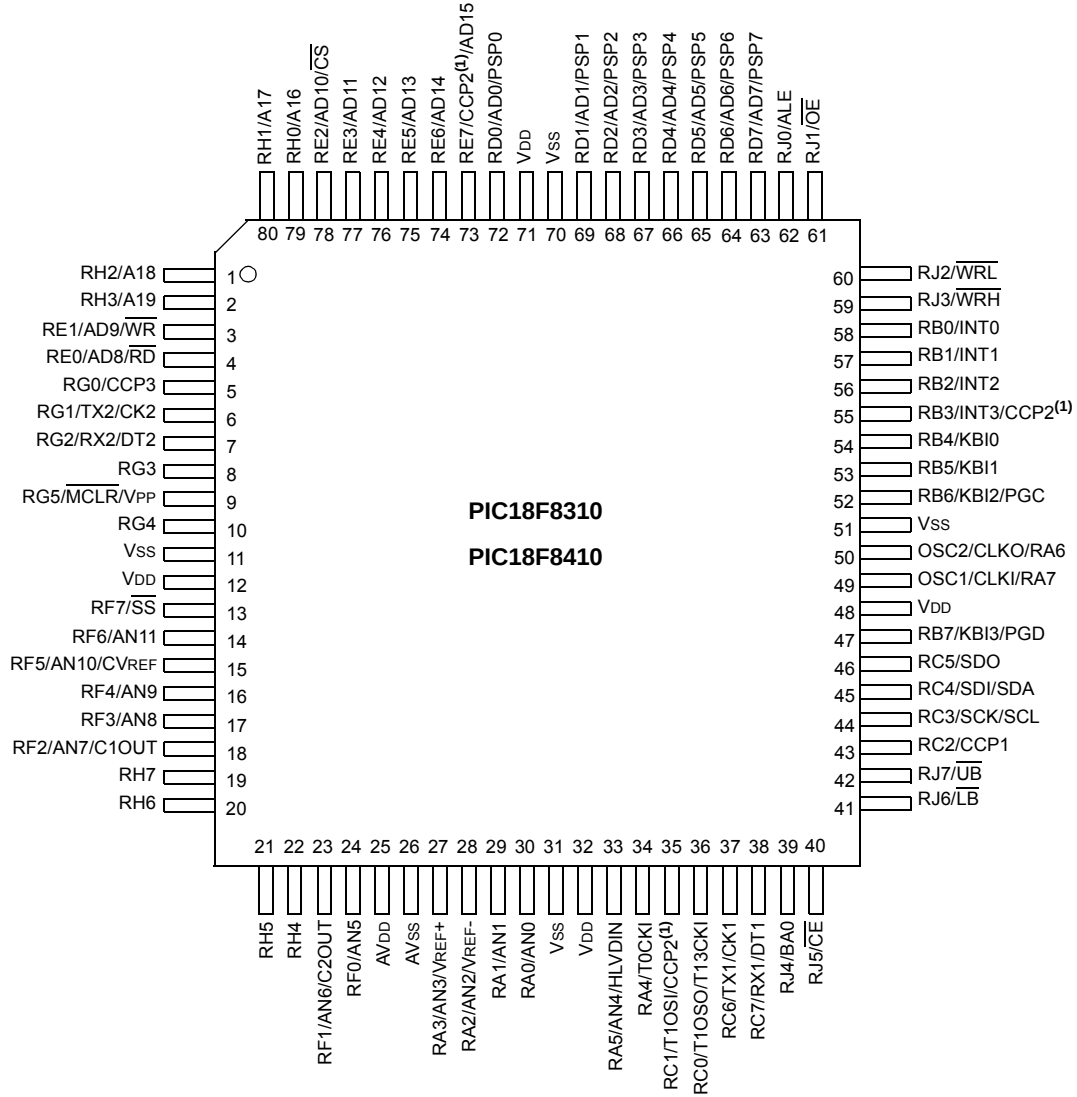
Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8310-e-pt

PIC18F6310/6410/8310/8410

Pin Diagrams (Continued)

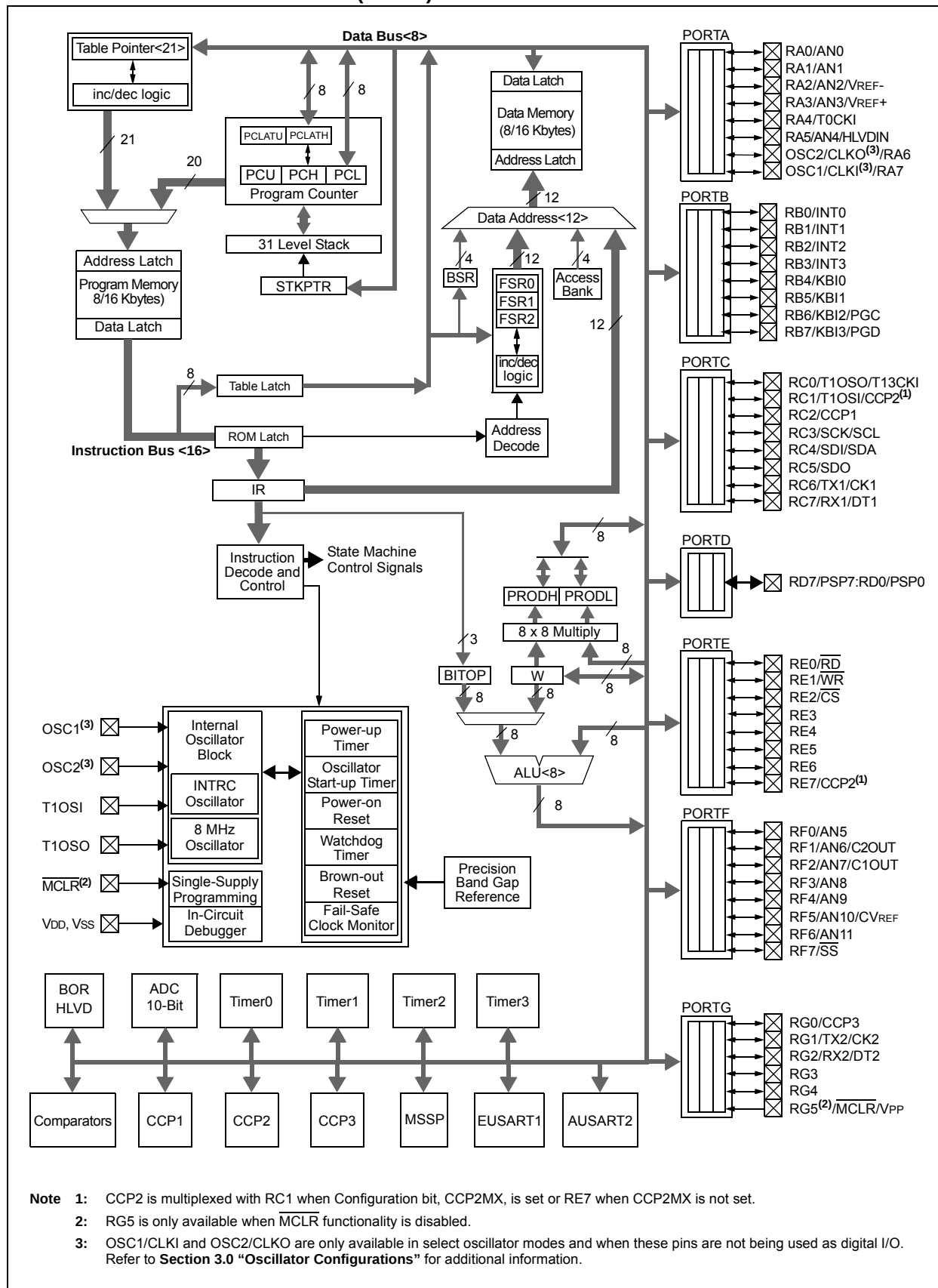
80-Pin TQFP



Note 1: RE7 is the alternate pin for CCP2 multiplexing.

PIC18F6310/6410/8310/8410

FIGURE 1-1: PIC18F6310/6410 (64-PIN) BLOCK DIAGRAM



PIC18F6310/6410/8310/8410

NOTES:

PIC18F6310/6410/8310/8410

TABLE 11-7: PORTD FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RD0/AD0/PSP0	RD0	0	O	DIG	LATD<0> data output.
		1	I	ST	PORTD<0> data input.
	AD0 ⁽²⁾	x	O	DIG	External memory interface, Address/Data Bit 0 output. ⁽¹⁾
		x	I	TTL	External memory interface, Data Bit 0 input. ⁽¹⁾
	PSP0	x	O	DIG	PSP read data output (LATD<0>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD1/AD1/PSP1	RD1	0	O	DIG	LATD<1> data output.
		1	I	ST	PORTD<1> data input.
	AD1 ⁽²⁾	x	O	DIG	External memory interface, Address/Data Bit 1 output. ⁽¹⁾
		x	I	TTL	External memory interface, Data Bit 1 input. ⁽¹⁾
	PSP1	x	O	DIG	PSP read data output (LATD<1>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD2/AD2/PSP2	RD2	0	O	DIG	LATD<2> data output.
		1	I	ST	PORTD<2> data input.
	AD2 ⁽²⁾	x	O	DIG	External memory interface, Address/Data Bit 2 output. ⁽¹⁾
		x	I	TTL	External memory interface, Data Bit 2 input. ⁽¹⁾
	PSP2	x	O	DIG	PSP read data output (LATD<2>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD3/AD3/PSP3	RD3	0	O	DIG	LATD<3> data output.
		1	I	ST	PORTD<3> data input.
	AD3 ⁽²⁾	x	O	DIG	External memory interface, Address/Data Bit 3 output. ⁽¹⁾
		x	I	TTL	External memory interface, Data Bit 3 input. ⁽¹⁾
	PSP3	x	O	DIG	PSP read data output (LATD<3>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD4/AD4/PSP4	RD4	0	O	DIG	LATD<4> data output.
		1	I	ST	PORTD<4> data input.
	AD4 ⁽²⁾	x	O	DIG	External memory interface, Address/Data Bit 4 output. ⁽¹⁾
		x	I	TTL	External memory interface, Data Bit 4 input. ⁽¹⁾
	PSP4	x	O	DIG	PSP read data output (LATD<4>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD5/AD5/PSP5	RD5	0	O	DIG	LATD<5> data output.
		1	I	ST	PORTD<5> data input.
	AD5 ⁽²⁾	x	O	DIG	External memory interface, Address/Data Bit 5 output. ⁽¹⁾
		x	I	TTL	External memory interface, Data Bit 5 input. ⁽¹⁾
	PSP5	x	O	DIG	PSP read data output (LATD<5>); takes priority over port data.
		x	I	TTL	PSP write data input.
RD6/AD6/PSP6	RD6	0	O	DIG	LATD<6> data output.
		1	I	ST	PORTD<6> data input.
	AD6 ⁽²⁾	x	O	DIG-3	External memory interface, Address/Data Bit 6 output. ⁽¹⁾
		x	I	TTL	External memory interface, Data Bit 6 input. ⁽¹⁾
	PSP6	x	O	DIG	PSP read data output (LATD<6>); takes priority over port data.
		x	I	TTL	PSP write data input.

Legend: O = Output, I = Input, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: External memory interface I/O takes priority over all other digital and PSP I/O.

2: Implemented on 80-pin devices only.

PIC18F6310/6410/8310/8410

FIGURE 11-4: PARALLEL SLAVE PORT READ WAVEFORMS

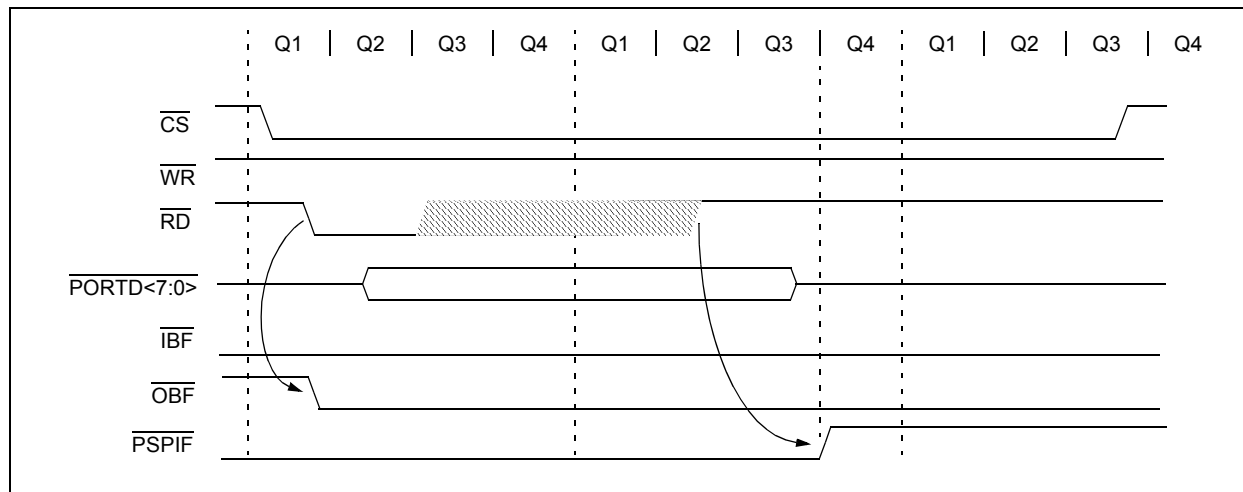


TABLE 11-19: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	66
LATD	LATD Output Latch Register								66
TRISD	PORTD Data Direction Register								66
PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	66
LATE	LATE Output Latch Register								66
TRISE	PORTE Data Direction Register								66
PSPCON	IBF	OBF	IBOV	PSPMODE	—	—	—	—	65
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	63
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	CCP1IF	TMR2IF	TMR1IF	65
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	CCP1IE	TMR2IE	TMR1IE	65
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	CCP1IP	TMR2IP	TMR1IP	65

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Parallel Slave Port.

14.0 TIMER2 MODULE

The Timer2 timer module incorporates the following features:

- 8-bit Timer and Period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software-programmable prescaler (1:1, 1:4 and 1:16)
- Software-programmable postscaler (1:1 through 1:16)
- Interrupt on TMR2-to-PR2 match
- Optional use as the shift clock for the MSSP module

The module is controlled through the T2CON register (Register 14-1), which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 14-1.

14.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock ($F_{osc}/4$). A 2-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divide-by-16 prescale options; these are selected by the prescaler control bits, T2CKPS<1:0> (T2CON<1:0>). The value of TMR2 is compared to that of the period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see **Section 14.2 “Timer2 Interrupt”**).

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset (Power-on Reset, $\overline{MCLR}$ Reset, Watchdog Timer Reset, or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 14-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	Unimplemented: Read as '0'
bit 6-3	T2OUTPS<3:0>: Timer2 Output Postscale Select bits 0000 = 1:1 Postscale 0001 = 1:2 Postscale • • • 1111 = 1:16 Postscale
bit 2	TMR2ON: Timer2 On bit 1 = Timer2 is on 0 = Timer2 is off
bit 1-0	T2CKPS<1:0>: Timer2 Clock Prescale Select bits 00 = Prescaler is 1 01 = Prescaler is 4 1x = Prescaler is 16

PIC18F6310/6410/8310/8410

16.0 CAPTURE/COMPARE/PWM (CCP) MODULES

PIC18F6310/6410/8310/8410 devices have three CCP (Capture/Compare/PWM) modules, labelled CCP1, CCP2 and CCP3. All modules implement standard Capture, Compare and Pulse-Width Modulation (PWM) modes.

Each CCP module contains a 16-bit register which can operate as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register. For the sake of clarity, all CCP module operation in the following sections is described with respect to CCP2, but are equally applicable to CCP1 and CCP3.

REGISTER 16-1: CCPxCON: CCP1/CCP2/CCP3 CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB<1:0>:** PWM Duty Cycle bit 1 and bit 0 for CCP Module x

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM Duty Cycle register. The eight Most Significant bits (DCx<9:2>) of the PWM Duty Cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>:** CCP Module x Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)

0001 = Reserved

0010 = Compare mode, toggle output on match (CCPxIF bit is set)

0011 = Reserved

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode: initialize CCPx pin low; on compare match, force CCPx pin high (CCPxIF bit is set)

1001 = Compare mode: initialize CCPx pin high; on compare match, force CCPx pin low (CCPxIF bit is set)

1010 = Compare mode: generate software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)

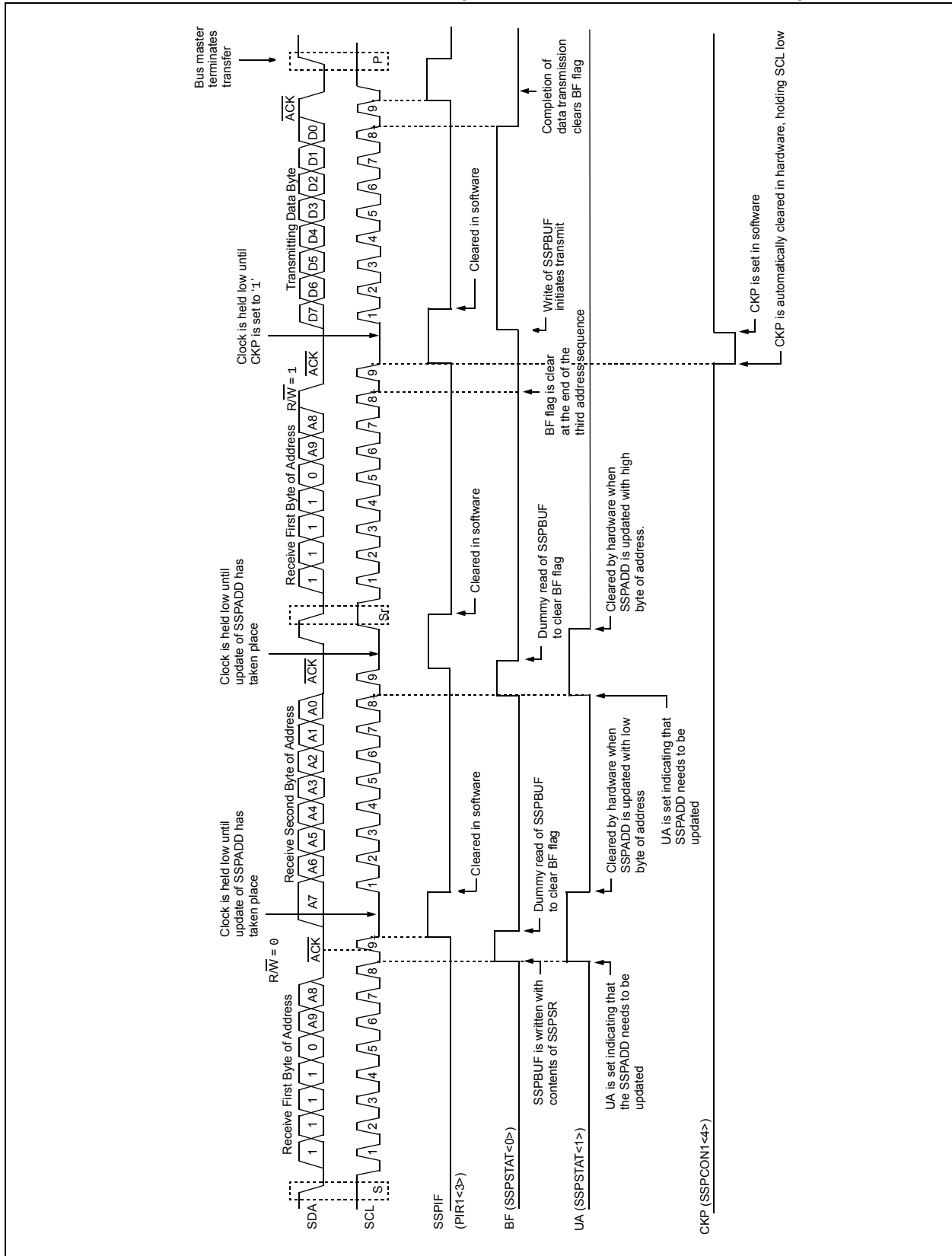
1011 = Compare mode: trigger special event, reset timer, start A/D conversion on CCPx match (CCPxIF bit is set)^(1,2)

11xx = PWM mode

Note 1: The Special Event Trigger on CCP1 will reset the timer but not start an A/D conversion on a CCP1 match.

2: For CCP3, the Special Event Trigger is not available. This mode functions the same as Compare Generate Interrupt mode (CCP3M<3:0> = 1010).

FIGURE 17-11: I²C™ SLAVE MODE TIMING (TRANSMISSION, 10-BIT ADDRESS)



PIC18F6310/6410/8310/8410

TABLE 18-3: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 1											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.00	8332	0.300	0.02	4165	0.300	0.02	2082	0.300	-0.04	1665
1.2	1.200	0.02	2082	1.200	-0.03	1041	1.200	-0.03	520	1.201	-0.16	415
2.4	2.402	0.06	1040	2.399	-0.03	520	2.404	0.16	259	2.403	-0.16	207
9.6	9.615	0.16	259	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 0, BRG16 = 1								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.04	832	0.300	-0.16	415	0.300	-0.16	207
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25
9.6	9.615	0.16	25	9.615	-0.16	12	—	—	—
19.2	19.231	0.16	12	—	—	—	—	—	—
57.6	62.500	8.51	3	—	—	—	—	—	—
115.2	125.000	8.51	1	—	—	—	—	—	—

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.00	33332	0.300	0.00	16665	0.300	0.00	8332	0.300	-0.01	6665
1.2	1.200	0.00	8332	1.200	0.02	4165	1.200	0.02	2082	1.200	-0.04	1665
2.4	2.400	0.02	4165	2.400	0.02	2082	2.402	0.06	1040	2.400	-0.04	832
9.6	9.606	0.06	1040	9.596	-0.03	520	9.615	0.16	259	9.615	-0.16	207
19.2	19.193	-0.03	520	19.231	0.16	259	19.231	0.16	129	19.230	-0.16	103
57.6	57.803	0.35	172	57.471	-0.22	86	58.140	0.94	42	57.142	0.79	34
115.2	114.943	-0.22	86	116.279	0.94	42	113.636	-1.36	21	117.647	-2.12	16

BAUD RATE (K)	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.01	3332	0.300	-0.04	1665	0.300	-0.04	832
1.2	1.200	0.04	832	1.201	-0.16	415	1.201	-0.16	207
2.4	2.404	0.16	415	2.403	-0.16	207	2.403	-0.16	103
9.6	9.615	0.16	103	9.615	-0.16	51	9.615	-0.16	25
19.2	19.231	0.16	51	19.230	-0.16	25	19.230	-0.16	12
57.6	58.824	2.12	16	55.555	3.55	8	—	—	—
115.2	111.111	-3.55	8	—	—	—	—	—	—

PIC18F6310/6410/8310/8410

TABLE 19-3: BAUD RATES FOR ASYNCHRONOUS MODES

BAUD RATE (K)	BRGH = 0											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	1.221	1.73	255	1.202	0.16	129	1.201	-0.16	103
2.4	2.441	1.73	255	2.404	0.16	129	2.404	0.16	64	2.403	-0.16	51
9.6	9.615	0.16	64	9.766	1.73	31	9.766	1.73	15	9.615	-0.16	12
19.2	19.531	1.73	31	19.531	1.73	15	19.531	1.73	7	—	—	—
57.6	56.818	-1.36	10	62.500	8.51	4	52.083	-9.58	2	—	—	—
115.2	125.000	8.51	4	104.167	-9.58	2	78.125	-32.18	1	—	—	—

BAUD RATE (K)	BRGH = 0								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	0.16	207	0.300	-0.16	103	0.300	-0.16	51
1.2	1.202	0.16	51	1.201	-0.16	25	1.201	-0.16	12
2.4	2.404	0.16	25	2.403	-0.16	12	—	—	—
9.6	8.929	-6.99	6	—	—	—	—	—	—
19.2	20.833	8.51	2	—	—	—	—	—	—
57.6	62.500	8.51	0	—	—	—	—	—	—
115.2	62.500	-45.75	0	—	—	—	—	—	—

BAUD RATE (K)	BRGH = 1											
	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 10.000 MHz			Fosc = 8.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	—	—	—
1.2	—	—	—	—	—	—	—	—	—	—	—	—
2.4	—	—	—	—	—	—	2.441	1.73	255	2.403	-0.16	207
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	—	—

BAUD RATE (K)	BRGH = 1								
	Fosc = 4.000 MHz			Fosc = 2.000 MHz			Fosc = 1.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	0.300	-0.16	207
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25
9.6	9.615	0.16	25	9.615	-0.16	12	—	—	—
19.2	19.231	0.16	12	—	—	—	—	—	—
57.6	62.500	8.51	3	—	—	—	—	—	—
115.2	125.000	8.51	1	—	—	—	—	—	—

PIC18F6310/6410/8310/8410

19.3.2 AUSART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either the Single Receive Enable bit, SREN (RCSTA2<5>), or the Continuous Receive Enable bit, CREN (RCSTA2<4>). Data is sampled on the RX2 pin on the falling edge of the clock.

If enable bit, SREN, is set, only a single word is received. If enable bit, CREN, is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.

To set up a Synchronous Master Reception:

1. Initialize the SPBRG2 register for the appropriate baud rate.
2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
3. Ensure bits, CREN and SREN, are clear.
4. If interrupts are desired, set enable bit, RC2IE.
5. If 9-bit reception is desired, set bit, RX9.
6. If a single reception is required, set bit, SREN. For continuous reception, set bit, CREN.
7. Interrupt flag bit, RC2IF, will be set when reception is complete and an interrupt will be generated if the enable bit, RC2IE, was set.
8. Read the RCSTA2 register to get the 9th bit (if enabled) and determine if any error occurred during reception.
9. Read the 8-bit received data by reading the RCREG2 register.
10. If any error occurred, clear the error by clearing bit, CREN.
11. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 19-8: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)

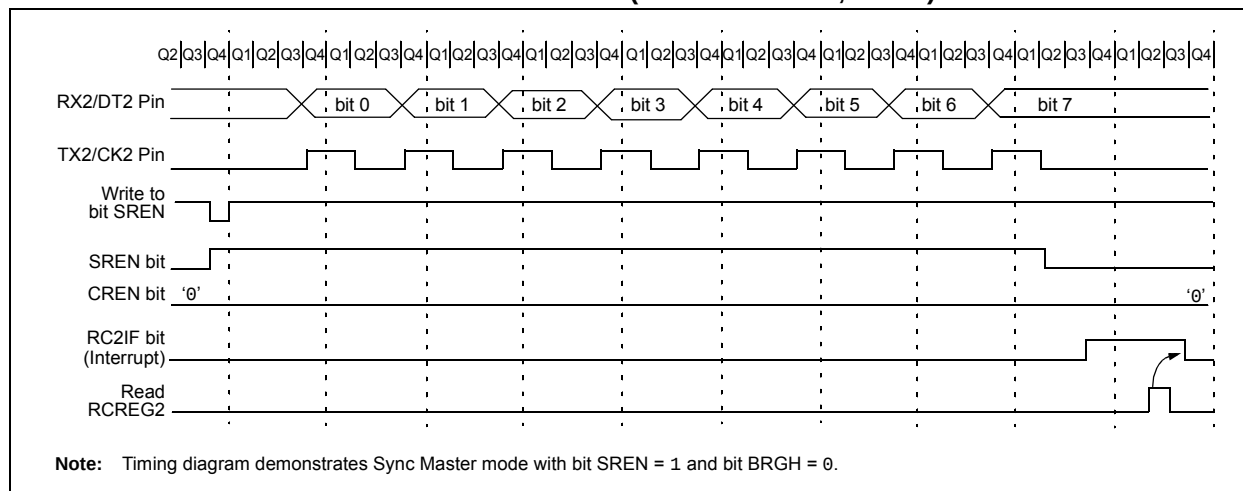


TABLE 19-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	63
PIR3	—	—	RC2IF	TX2IF	—	—	—	CCP3IF	65
PIE3	—	—	RC2IE	TX2IE	—	—	—	CCP3IE	65
IPR3	—	—	RC2IP	TX2IP	—	—	—	CCP3IP	65
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	66
RCREG2	AUSART2 Receive Register								66
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	66
SPBRG2	AUSART2 Baud Rate Generator Register Low Byte								66

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.

PIC18F6310/6410/8310/8410

19.4.2 AUSART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical except in the case of Sleep, or any Idle mode and bit, SREN, which is a “don’t care” in Slave mode.

If receive is enabled by setting the CREN bit prior to entering Sleep, or any Idle mode, then a word may be received while in this low-power mode. Once the word is received, the RSR register will transfer the data to the RCREG2 register; if the RC2IE enable bit is set, the interrupt generated will wake the chip from low-power mode. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Reception:

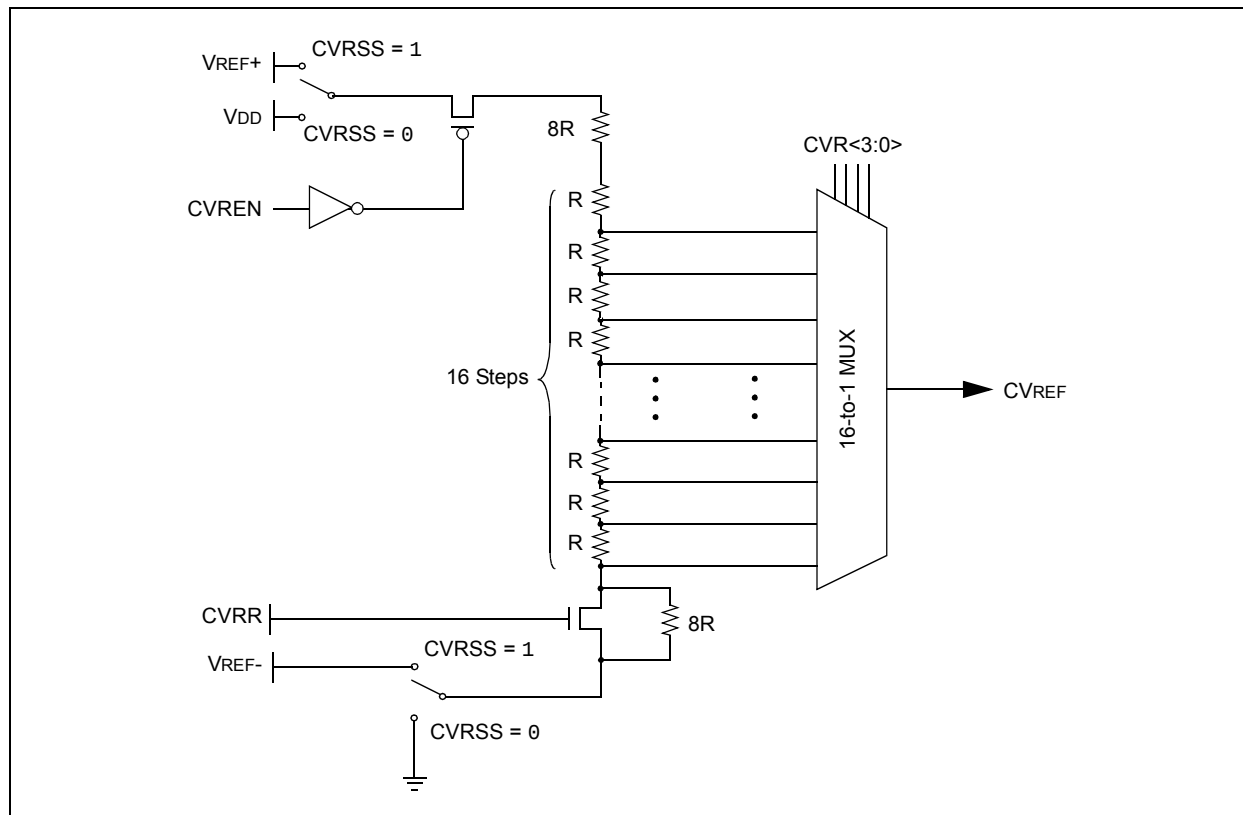
1. Enable the synchronous master serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
2. If interrupts are desired, set enable bit, RC2IE.
3. If 9-bit reception is desired, set bit, RX9.
4. To enable reception, set enable bit, CREN.
5. Flag bit, RC2IF, will be set when reception is complete. An interrupt will be generated if enable bit, RC2IE, was set.
6. Read the RCSTA2 register to get the 9th bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREG2 register.
8. If any error occurred, clear the error by clearing bit, CREN.
9. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 19-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	63
PIR3	—	—	RC2IF	TX2IF	—	—	—	CCP3IF	65
PIE3	—	—	RC2IE	TX2IE	—	—	—	CCP3IE	65
IPR3	—	—	RC2IP	TX2IP	—	—	—	CCP3IP	65
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	66
RCREG2	AUSART2 Receive Register								66
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	66
SPBRG2	AUSART2 Baud Rate Generator Register Low Byte								66

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used for synchronous slave reception.

FIGURE 22-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



22.2 Voltage Reference Accuracy/Error

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 22-1) keep CVREF from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the CVREF output changes with fluctuations in that source. The tested absolute accuracy of the voltage reference can be found in **Section 27.0 “Electrical Characteristics”**.

22.3 Operation During Sleep

When the device wakes up from Sleep, through an interrupt or a Watchdog Timer time-out, the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

22.4 Effects of a Reset

A device Reset disables the voltage reference by clearing bit, CVREN (CVRCON<7>). This Reset also disconnects the reference from the RA2 pin by clearing bit, CVROE (CVRCON<6>), and selects the high-voltage range by clearing bit, CVRR (CVRCON<5>). The CVR value select bits are also cleared.

22.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RF5 pin if the TRISF<5> bit and the CVROE bit are both set. Enabling the voltage reference output onto the RF5 pin, with an input signal present, will increase current consumption. Connecting RF5 as a digital output with CVRSS enabled will also increase current consumption.

The RF5 pin can be used as a simple D/A output with limited drive capability. Due to the limited current drive capability, a buffer must be used on the voltage reference output for external connections to VREF. Figure 22-2 shows an example buffering technique.

PIC18F6310/6410/8310/8410

COMF		Complement f						
Syntax:	COMF f {,d {,a}}							
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$							
Operation:	$(\overline{f}) \rightarrow \text{dest}$							
Status Affected:	N, Z							
Encoding:	<table border="1"><tr><td>0001</td><td>11da</td><td>ffff</td><td>ffff</td></tr></table>				0001	11da	ffff	ffff
0001	11da	ffff	ffff					
Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See Section 25.2.3 for details.							
Words:	1							
Cycles:	1							
Q Cycle Activity:								
	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process Data	Write to destination				

Example: COMF REG, 0, 0

Before Instruction
 REG = 13h
 After Instruction
 REG = 13h
 W = ECh

CPFSEQ		Compare f with W, skip if f = W						
Syntax:	CPFSEQ f {,a}							
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$							
Operation:	$(f) - (W)$, skip if $(f) = (W)$ (unsigned comparison)							
Status Affected:	None							
Encoding:	<table border="1"><tr><td>0110</td><td>001a</td><td>ffff</td><td>ffff</td></tr></table>				0110	001a	ffff	ffff
0110	001a	ffff	ffff					
Description:	Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If 'f' = W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See Section 25.2.3 for details.							
Words:	1							
Cycles:	1(2)							
	Note: 3 cycles if skip and followed by a 2-word instruction.							

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example: HERE CPFSEQ REG, 0
 NEQUAL :
 EQUAL :

Before Instruction
 PC Address = HERE
 W = ?
 REG = ?
 After Instruction
 If REG = W;
 PC = Address (EQUAL)
 If REG $\neq$ W;
 PC = Address (NEQUAL)

PIC18F6310/6410/8310/8410

SUBLW Subtract W from literal

Syntax: SUBLW k

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow W$

Status Affected: N, OV, C, DC, Z

Encoding:

0000	1000	kkkk	kkkk
------	------	------	------

Description: W is subtracted from the eight-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example 1: SUBLW 02h

Before Instruction

W = 01h
C = ?

After Instruction

W = 01h
C = 1 ; result is positive
Z = 0
N = 0

Example 2: SUBLW 02h

Before Instruction

W = 02h
C = ?

After Instruction

W = 00h
C = 1 ; result is zero
Z = 1
N = 0

Example 3: SUBLW 02h

Before Instruction

W = 03h
C = ?

After Instruction

W = FFh ; (2's complement)
C = 0 ; result is negative
Z = 0
N = 1

SUBWF Subtract W from f

Syntax: SUBWF f {,d {,a}}

Operands: $0 \leq f \leq 255$
 $d \in [0,1]$
 $a \in [0,1]$

Operation: $(f) - (W) \rightarrow \text{dest}$

Status Affected: N, OV, C, DC, Z

Encoding:

0101	11da	ffff	ffff
------	------	------	------

Description: Subtract W from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 25.2.3** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: SUBWF REG, 1, 0

Before Instruction

REG = 3
W = 2
C = ?

After Instruction

REG = 1
W = 2
C = 1 ; result is positive
Z = 0
N = 0

Example 2: SUBWF REG, 0, 0

Before Instruction

REG = 2
W = 2
C = ?

After Instruction

REG = 2
W = 0
C = 1 ; result is zero
Z = 1
N = 0

Example 3: SUBWF REG, 1, 0

Before Instruction

REG = 1
W = 2
C = ?

After Instruction

REG = FFh ; (2's complement)
W = 2
C = 0 ; result is negative
Z = 0
N = 1

PIC18F6310/6410/8310/8410

TBLRD		Table Read					
Syntax:	TBLRD (*; *+; *-, +*)						
Operands:	None						
Operation:	if TBLRD *, (Prog Mem (TBLPTR)) → TABLAT, TBLPTR – No Change; if TBLRD *+, (Prog Mem (TBLPTR)) → TABLAT, (TBLPTR) + 1 → TBLPTR; if TBLRD *-, (Prog Mem (TBLPTR)) → TABLAT, (TBLPTR) – 1 → TBLPTR; if TBLRD +*, (TBLPTR) + 1 → TBLPTR, (Prog Mem (TBLPTR)) → TABLAT						
Status Affected:	None						
Encoding:	<table><tr><td>0000</td><td>0000</td><td>0000</td><td>10nn nn=0 * =1 *+ =2 *- =3 +*</td></tr></table>			0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*
0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*				
Description:	This instruction is used to read the contents of Program Memory (P.M.). To address the program memory, a pointer called Table Pointer (TBLPTR) is used. The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-Mbyte address range. TBLPTR[0] = 0: Least Significant Byte of Program Memory Word TBLPTR[0] = 1: Most Significant Byte of Program Memory Word The TBLRD instruction can modify the value of TBLPTR as follows: • no change • post-increment • post-decrement • pre-increment						
Words:	1						
Cycles:	2						

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation
No operation	No operation (Read Program Memory)	No operation	No operation (Write TABLAT)

TBLRD	Table Read (Continued)
<u>Example 1:</u>	TBLRD *+ ;
Before Instruction	
TABLAT	= 55h
TBLPTR	= 00A356h
MEMORY(00A356h)	= 34h
After Instruction	
TABLAT	= 34h
TBLPTR	= 00A357h
<u>Example 2:</u>	TBLRD *- ;
Before Instruction	
TABLAT	= AAh
TBLPTR	= 01A357h
MEMORY(01A357h)	= 12h
MEMORY(01A358h)	= 34h
After Instruction	
TABLAT	= 34h
TBLPTR	= 01A358h

FIGURE 27-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

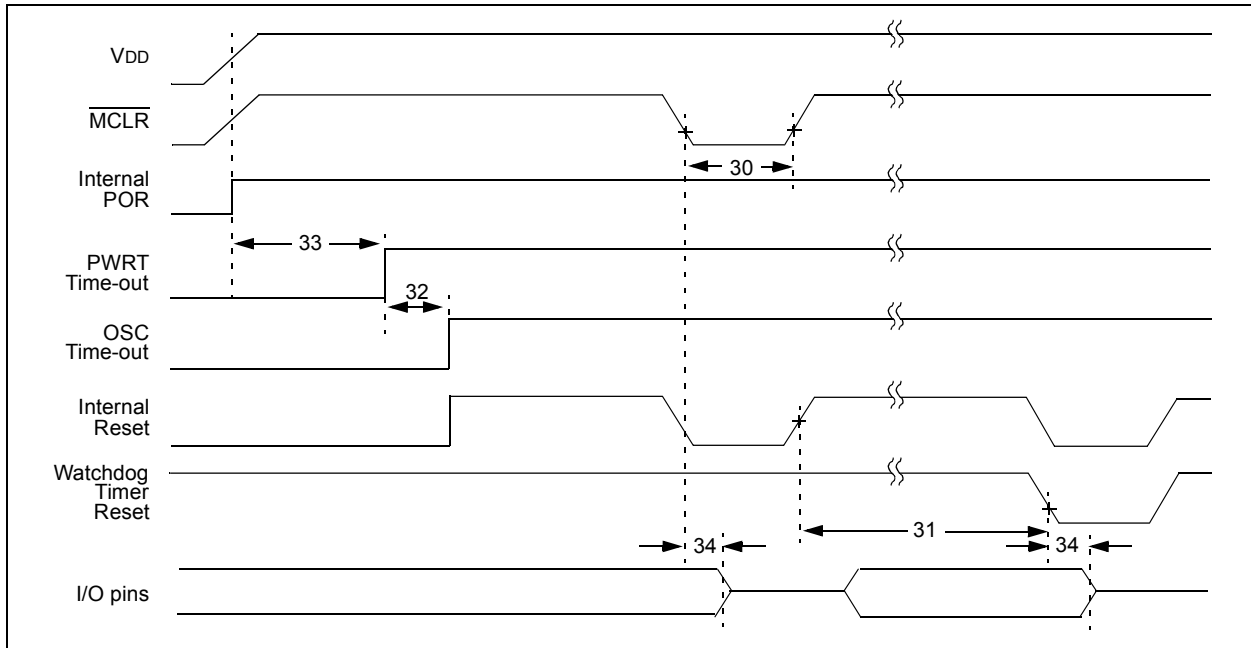


FIGURE 27-11: BROWN-OUT RESET TIMING

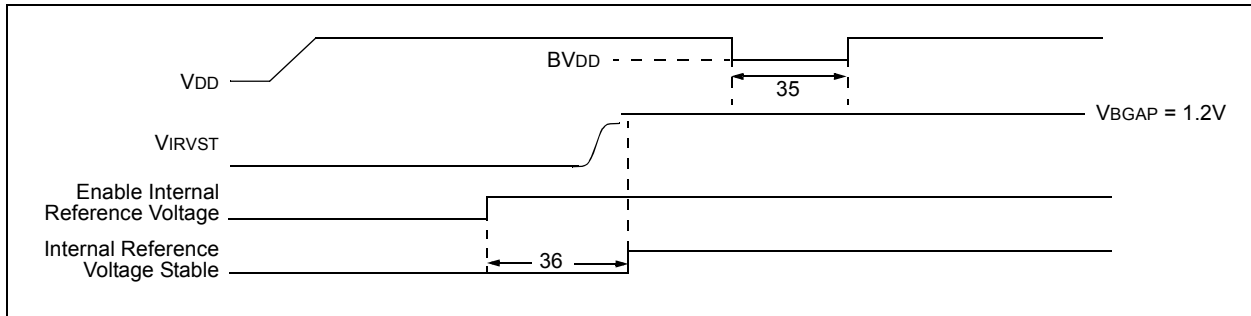


TABLE 27-12: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	—	—	μs	
31	TWDT	Watchdog Timer Time-out Period (no postscaler)	3.4	4.1	4.71	ms	
32	TOST	Oscillator Start-up Timer Period	1024 TOSC	—	1024 TOSC	—	TOSC = OSC1 period
33	TPWRT	Power-up Timer Period	55.5	65.5	75	ms	
34	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μs	
35	TBOR	Brown-out Reset Pulse Width	200	—	—	μs	VDD ≤ BVDD (see D005)
36	TIrVST	Time for Internal Reference Voltage to become stable	—	20	50	μs	
37	TLVD	Low-Voltage Detect Pulse Width	200	—	—	μs	VDD ≤ VLVD
38	TCSD	CPU Start-up Time	—	10	—	μs	
39	TI0BST	Time for INTRC Block to stabilize	—	1	—	ms	

PIC18F6310/6410/8310/8410

TBLRD	335
TBLWT	336
TSTFSZ	337
XORLW	337
XORWF	338
Summary Table	300
INTCON Register	
RBIF Bit	128
INTCON Registers	111
Inter-Integrated Circuit. <i>See</i> I ² C.	
Internal Oscillator Block	38
Adjustment	38
INTIO Modes	38
INTOSC Frequency Drift	38
INTOSC Output Frequency	38
OSCTUNE Register	38
Internal RC Oscillator	
Use with WDT	290
Internet Address	409
Interrupt Sources	281
A/D Conversion Complete	259
Context Saving During Interrupts	124
Interrupt-on-Change (RB7:RB4)	128
INTx Pin	124
PORTB, Interrupt-on-Change	124
TMR0	124
TMR0 Overflow	153
TMR1 Overflow	155
TMR2 to PR2 Match (PWM)	173
TMR3 Overflow	163, 165
Interrupts	109
Interrupts, Flag Bits	
Interrupt-on-Change (RB7:RB4) Flag (RBIF Bit)	128
INTOSC, INTRC. <i>See</i> Internal Oscillator Block.	
IORLW	320
IORWF	320
IPR Registers	120
L	
LFSR	321
M	
Master Clear ($\overline{\text{MCLR}}$)	57
Master Synchronous Serial Port (MSSP). <i>See</i> MSSP.	
Memory Organization	67
Data Memory	75
Program Memory	67
Memory Programming Requirements	365
Microchip Internet Web Site	409
Migration from Baseline to Enhanced Devices	396
Migration from High-End to Enhanced Devices	397
Migration from Mid-Range to Enhanced Devices	397
MOVF	321
MOVFF	322
MOVLB	322
MOVLW	323
MOVSS	342
MOVWF	323
MPLAB ASM30 Assembler, Linker, Librarian	348
MPLAB Integrated Development Environment	
Software	347
MPLAB PM3 Device Programmer	350
MPLAB REAL ICE In-Circuit Emulator System	349
MPLINK Object Linker/MPLIB Object Librarian	348

MSSP	
ACK Pulse	190, 191
Control Registers (general)	177
I ² C Mode. <i>See</i> I ² C Mode.	
Module Overview	177
SPI Master/Slave Connection	181
SPI Mode. <i>See</i> SPI Mode.	
SSPBUF	182
SSPSR	182
MULLW	324
MULWF	324
N	
NEGF	325
NOP	325
O	
Oscillator	
Clock Sources	40
Selecting the 31 kHz Source	41
Selection Using OSCCON Register	41
External Clock Input	36
RC	37
RCIO Mode	37
Switching	40
Transitions	41
Oscillator Configuration	35
EC	35
ECIO	35
HS	35
HSPLL	35
Internal Oscillator Block	38
INTIO1	35
INTIO2	35
LP	35
RC	35
RCIO	35
XT	35
Oscillator Selection	281
Oscillator Start-up Timer (OST)	43, 281
Oscillator, Timer1	155, 165
Oscillator, Timer3	163
P	
Packaging	389
Details	390
Marking	389
Parallel Slave Port (PSP)	148
Associated Registers	150
RE0/RD Pin	148
RE1/ $\overline{\text{WR}}$ Pin	148
RE2/ $\overline{\text{CS}}$ Pin	148
Select (PSPMODE Bit)	148
PIC18 Instruction Execution, Extended	88
PIE Registers	117
Pin Functions	
AVDD	30
AVDD	21
AVss	21
AVss	30
OSC1/CLKI/RA7	14, 22
OSC2/CLKO/RA6	14, 22
RA0/AN0	15, 23
RA1/AN1	15, 23
RA2/AN2/VREF-	15, 23
RA3/AN3/VREF+	15, 23

PIC18F6310/6410/8310/8410

RA4/T0CKI	15, 23	RH0/AD16	29
RA5/AN4/HLVDIN	15, 23	RH1/AD17	29
RB0/INT0	16, 24	RH2/AD18	29
RB1/INT1	16, 24	RH3/AD19	29
RB2/INT2	16, 24	RH4	29
RB3/INT3	16	RH5	29
RB3/INT3/CCP2	24	RH6	29
RB4/KBI0	16, 24	RH7	29
RB5/KBI1	16, 24	RJ0/ALE	30
RB6/KBI2/PGC	16, 24	RJ1/OE	30
RB7/KBI3/PGD	16, 24	RJ2/WRL	30
RC0/T1OSO/T13CKI	17, 25	RJ3/WRH	30
RC1/T1OSI/CCP2	17, 25	RJ4/BA0	30
RC2/CCP1	17, 25	RJ5/CE	30
RC3/SCK/SCL	17, 25	RJ6/LB	30
RC4/SDI/SDA	17, 25	RJ7/UB	30
RC5/SDO	17, 25	VDD	21
RC6/TX1/CK1	17, 25	VDD	30
RC7/RX1/DT1	17, 25	Vss	21
RD0/AD0/PSP0	26	Vss	30
RD0/PSP0	18	Pinout I/O Descriptions	
RD1/AD1/PSP1	26	PIC18F6310/6410	14
RD1/PSP1	18	PIC18F8310/8410	22
RD2/AD2/PSP2	26	PIR Registers	114
RD2/PSP2	18	PLL	37
RD3/AD3/PSP3	26	HSPLL Oscillator Mode	37
RD3/PSP3	18	Use with INTOSC	37, 38
RD4/AD4/PSP4	26	POP	326
RD4/PSP4	18	POR. See Power-on Reset.	
RD5/AD5/PSP5	26	PORTA	
RD5/PSP5	18	Associated Registers	127
RD6/AD6/PSP6	26	Functions	126
RD6/PSP6	18	LATA Register	125
RD7/AD7/PSP7	26	PORTA Register	125
RD7/PSP7	18	TRISA Register	125
RE0/AD8/RD	27	PORTB	
RE0/RD	19	Associated Registers	130
RE1/AD9/WR	27	Functions	129
RE1/WR	19	LATB Register	128
RE2/AD10/CS	27	PORTB Register	128
RE2/CS	19	RB7:RB4 Interrupt-on-Change Flag (RBIF Bit)	128
RE3	19	TRISB Register	128
RE3/AD11	27	PORTC	
RE4	19	Associated Registers	133
RE4/AD12	27	Functions	132
RE5	19	LATC Register	131
RE5/AD13	27	PORTC Register	131
RE6	19	RC3/SCK/SCL Pin	191
RE6/AD14	27	TRISC Register	131
RE7/CCP2	19	PORTD	148
RE7/CCP2/AD15	27	Associated Registers	136
RF0/AN5	20, 28	Functions	135
RF1/AN6/C2OUT	20, 28	LATD Register	134
RF2/AN7/C1OUT	20, 28	PORTD Register	134
RF3/AN8	20, 28	TRISD Register	134
RF4/AN9	20, 28	PORTE	
RF5/AN10/CVREF	20, 28	Analog Port Pins	148
RF6/AN11	20, 28	Associated Registers	139
RF7/SS	20, 28	Functions	138
RG0/CCP3	21, 29	LATE Register	137
RG1/TX2/CK2	21, 29	PORTE Register	137
RG2/RX2/DT2	21, 29	PSP Mode Select (PSPMODE Bit)	148
RG3	21, 29	RE0/RD Pin	148
RG4	21, 29	RE1/WR Pin	148
RG5	21, 29	RE2/CS Pin	148
RG5/MCLR/VPP	14, 22	TRISE Register	137

PIC18F6310/6410/8310/8410

PORTF				Instructions	74
Associated Registers	141			Two-Word Instructions	74
Functions	141			Interrupt Vector	67
LATF Register	140			Look-up Tables	72
PORTF Register	140			Map and Stack (diagram)	67
TRISF Register	140			Memory Access for PIC18F8310/8410 Modes	69
PORTG				Memory Maps for PIC18FX310/X410 Modes	69
Associated Registers	143			PIC18F8310/8410 Memory Modes	68
Functions	143			Reset Vector	67
LATG Register	142			Table Reads and Table Writes	89
PORTG Register	142			Writing and Erasing On-Chip Program	
TRISG Register	142			Memory (ICSP Mode)	92
PORTH				Writing To	
Associated Registers	145			Unexpected Termination	92
Functions	145			Write Verify	92
LATH Register	144			Writing to Memory Space (PIC18F8X10)	92
PORTH Register	144			Program Memory Modes	
TRISH Register	144			Extended Microcontroller	96
PORTJ				Microcontroller	96
Associated Registers	147			Microprocessor	96
Functions	147			Microprocessor with Boot Block	96
LATJ Register	146			Program Verification and Code Protection	295
PORTJ Register	146			Associated Registers	295
TRISJ Register	146			Programming, Device Instructions	297
Postscaler, WDT				PSP. See Parallel Slave Port.	
Assignment (PSA Bit)	153			Pulse-Width Modulation. See PWM (CCP Module).	
Rate Select (T0PS2:T0PS0 Bits)	153			PUSH	326
Switching Between Timer0 and WDT	153			PUSH and POP Instructions	71
Power-Managed Modes	45			PUSHL	342
and Multiple Sleep Commands	46			PWM (CCP Module)	
Clock Sources	45			Associated Registers	175
Clock Transitions, Status Indicators	46			Duty Cycle	174
Entering	45			Example Frequencies/Resolutions	174
Exiting Idle and Sleep Modes	53			Period	173
by Interrupt	53			Setup for PWM Operation	174
by Reset	53			TMR2 to PR2 Match	173
by WDT Time-out	53				
Without an Oscillator Start-up Delay	53				
Idle Modes	50				
Operation	105				
Run Modes	46				
Selecting	45				
Sleep Mode	50				
Summary (table)	45				
Power-on Reset (POR)	57, 281				
Oscillator Start-up Timer (OST)	59				
Power-up Timer (PWRT)	59				
Time-out Sequence	59				
Power-up Delays	43				
Power-up Timer (PWRT)	43, 281				
Prescaler, Capture	170				
Prescaler, Timer0	153				
Assignment (PSA Bit)	153				
Rate Select (T0PS2:T0PS0 Bits)	153				
Switching Between Timer0 and WDT	153				
Prescaler, TMR2	174				
Program Counter	70				
PCL, PCH and PCU Registers	70				
PCLATH and PCLATU Registers	70				
Program Memory	89				
Code Protection, from Table Reads	295				
Control Registers	90				
TABLAT (Table Latch) Register	90				
TBLPTR (Table Pointer) Register	90				
Erasing External Memory (PIC18F8X10)	92				