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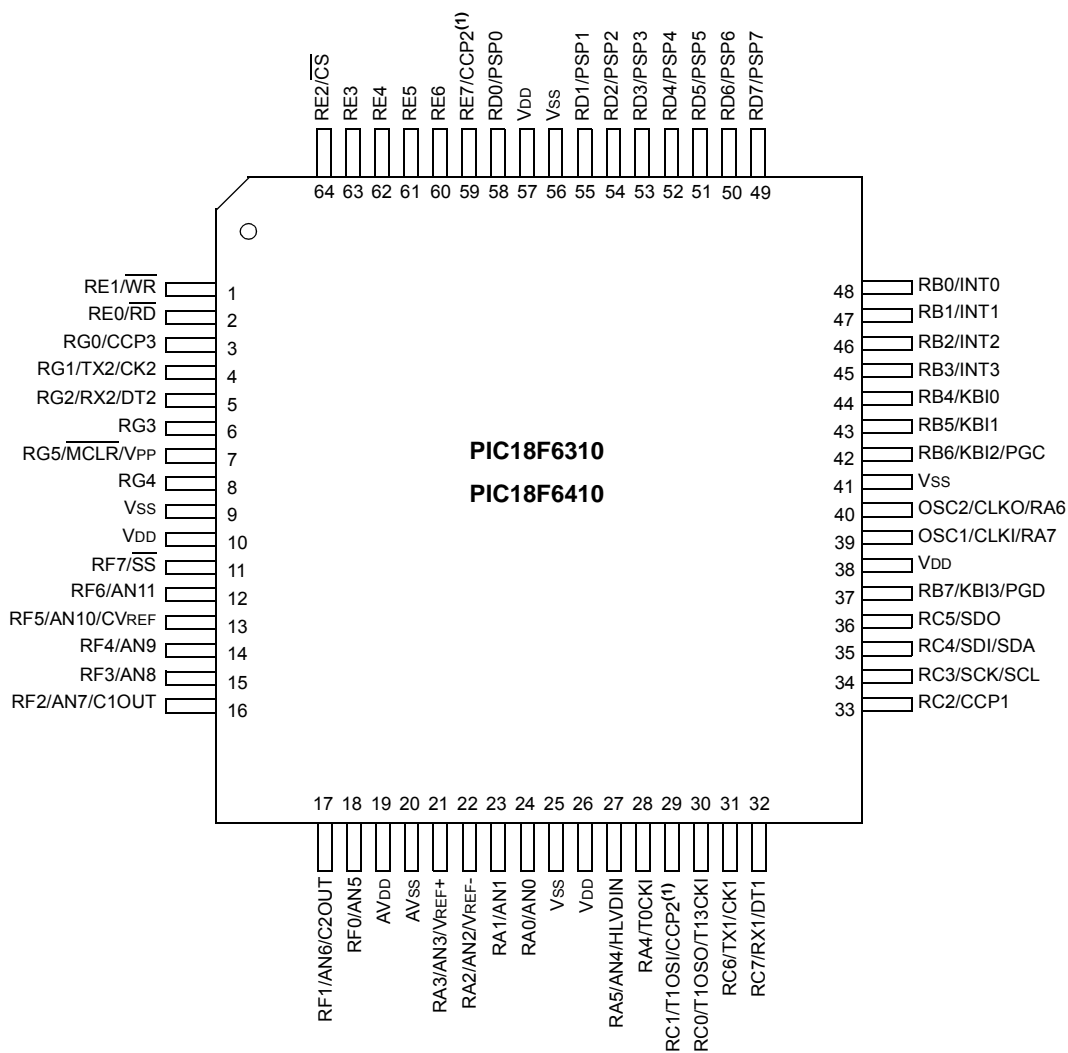
Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf6310t-i-pt

PIC18F6310/6410/8310/8410

Pin Diagrams

64-Pin TQFP



Note 1: RE7 is the alternate pin for CCP2 multiplexing.

PIC18F6310/6410/8310/8410

TABLE 1-2: PIC18F6310/6410 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG5/MCLR/VPP RG5 MCLR VPP	7	I I P	ST ST 	Master Clear (input) or programming voltage (input). Digital input. Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input.
OSC1/CLKI/RA7 OSC1 CLKI RA7	39	I I I/O	ST CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	40	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

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TABLE 1-2: PIC18F6310/6410 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/PSP0	58			PORTD is a bidirectional I/O port.
RD0		I/O	ST	Digital I/O.
PSP0		I/O	TTL	Parallel Slave Port data.
RD1/PSP1	55			
RD1		I/O	ST	Digital I/O.
PSP1		I/O	TTL	Parallel Slave Port data.
RD2/PSP2	54			
RD2		I/O	ST	Digital I/O.
PSP2		I/O	TTL	Parallel Slave Port data.
RD3/PSP3	53			
RD3		I/O	ST	Digital I/O.
PSP3		I/O	TTL	Parallel Slave Port data.
RD4/PSP4	52			
RD4		I/O	ST	Digital I/O.
PSP4		I/O	TTL	Parallel Slave Port data.
RD5/PSP5	51			
RD5		I/O	ST	Digital I/O.
PSP5		I/O	TTL	Parallel Slave Port data.
RD6/PSP6	50			
RD6		I/O	ST	Digital I/O.
PSP6		I/O	TTL	Parallel Slave Port data.
RD7/PSP7	49			
RD7		I/O	ST	Digital I/O.
PSP7		I/O	TTL	Parallel Slave Port data.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

8.4 Operation in Power-Managed Modes

In alternate, power-managed Run modes, the external bus continues to operate normally. If a clock source with a lower speed is selected, bus operations will run at that speed. In these cases, excessive access times for the external memory may result if wait states have been enabled and added to external memory operations.

If operations in a lower power Run mode are anticipated, users should provide in their applications for adjusting memory access times at the lower clock speeds.

In Sleep and Idle modes, the microcontroller core does not need to access data; bus operations are suspended. The state of the external bus is frozen with the address/data pins and most of the control pins holding at the same state they were in when the mode was invoked. The only potential changes are the CE, LB and UB pins which are held at logic high.

TABLE 8-2: REGISTERS ASSOCIATED WITH THE EXTERNAL MEMORY INTERFACE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
MEMCON	EBDIS	—	WAIT1	WAIT0	—	—	WM1	WM0	65
CONFIG3L	WAIT	BW	—	—	—	—	PM1	PM0	285
CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	—	CCP2MX	286

Legend: — = unimplemented, read as '0'. Shaded cells are not used for the external memory interface.

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REGISTER 10-6: PIR3: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 3

U-0	U-0	R-0	R-0	U-0	U-0	U-0	U-0
—	—	RC2IF	TX2IF	—	—	—	CCP3IF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **RC2IF:** AUSART Receive Interrupt Flag bit

1 = The AUSART receive buffer, RCREG2, is full (cleared when RCREG2 is read)

0 = The AUSART receive buffer is empty

bit 4 **TX2IF:** AUSART Transmit Interrupt Flag bit

1 = The AUSART transmit buffer, TXREG2, is empty (cleared when TXREG2 is written)

0 = The AUSART transmit buffer is full

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **CCP3IF:** CCP3 Interrupt Flag bit

Capture mode:

1 = A TMR1/TMR3 register capture occurred (must be cleared in software)

0 = No TMR1/TMR3 register capture occurred

Compare mode:

1 = A TMR1/TMR3 register compare match occurred (must be cleared in software)

0 = No TMR1/TMR3 register compare match occurred

PWM mode:

Unused in this mode.

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10.4 IPR Registers

The IPR registers contain the individual priority bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are three Peripheral Interrupt Priority registers (IPR1, IPR2, IPR3). Using the priority bits requires that the Interrupt Priority Enable (IPEN) bit be set.

REGISTER 10-10: IPR1: PERIPHERAL INTERRUPT PRIORITY REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PSPIP	ADIP	RC1IP	TX1IP	SSPIP	CCP1IP	TMR2IP	TMR1IP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **PSPIP**: Parallel Slave Port Read/Write Interrupt Priority bit

1 = High priority

0 = Low priority

bit 6 **ADIP**: A/D Converter Interrupt Priority bit

1 = High priority

0 = Low priority

bit 5 **RC1IP**: EUSART Receive Interrupt Priority bit

1 = High priority

0 = Low priority

bit 4 **TX1IP**: EUSART Transmit Interrupt Priority bit

1 = High priority

0 = Low priority

bit 3 **SSPIP**: Master Synchronous Serial Port Interrupt Priority bit

1 = High priority

0 = Low priority

bit 2 **CCP1IP**: CCP1 Interrupt Priority bit

1 = High priority

0 = Low priority

bit 1 **TMR2IP**: TMR2 to PR2 Match Interrupt Priority bit

1 = High priority

0 = Low priority

bit 0 **TMR1IP**: TMR1 Overflow Interrupt Priority bit

1 = High priority

0 = Low priority

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11.7 PORTG, TRISG and LATG Registers

PORTG is a 6-bit wide, bidirectional port. The corresponding Data Direction register is TRISG. Setting a TRISG bit (= 1) will make the corresponding PORTG pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISG bit (= 0) will make the corresponding PORTG pin an output (i.e., put the contents of the output latch on the selected pin).

The Output Latch register (LATG) is also memory mapped. Read-modify-write operations on the LATG register, read and write the latched output value for PORTG.

PORTG is multiplexed with USART functions (Table 11-13). PORTG pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTG pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings. The pin override value is not loaded into the TRIS register. This allows read-modify-write of the TRIS register without concern due to peripheral overrides.

The sixth pin of PORTG (RG5/ $\overline{\text{MCLR}}$ /VPP) is an input only pin. Its operation is controlled by the MCLRE Configuration bit. When selected as a port pin (MCLRE = 0), it functions as a digital input only pin; as such, it does not have TRIS or LAT bits associated with its operation. Otherwise, it functions as the device's Master Clear input. In either configuration, RG5 also functions as the programming voltage input during programming.

Note: On a Power-on Reset, RG5 is enabled as a digital input only if Master Clear functionality is disabled. All other 5 pins are configured as digital inputs.

EXAMPLE 11-7: INITIALIZING PORTG

```
CLRF    PORTG    ; Initialize PORTG by
                ; clearing output
                ; data latches
CLRF    LATG      ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0x04      ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISG     ; Set RG1:RG0 as outputs
                ; RG2 as input
                ; RG4:RG3 as inputs
```


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TABLE 11-17: PORTJ FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RJ0/ALE	RJ0	0	O	DIG	LATJ<0> data output.
		1	I	ST	PORTJ<0> data input.
	ALE	x	O	DIG	External memory interface address latch enable control output; takes priority over digital I/O.
RJ1/OE	RJ1	0	O	DIG	LATJ<1> data output.
		1	I	ST	PORTJ<1> data input.
	OE	x	O	DIG	External memory interface output enable control output; takes priority over digital I/O.
RJ2/WRL	RJ2	0	O	DIG	LATJ<2> data output.
		1	I	ST	PORTJ<2> data input.
	WRL	x	O	DIG	External memory bus write low byte control; takes priority over digital I/O.
RJ3/WRH	RJ3	0	O	DIG	LATJ<3> data output.
		1	I	ST	PORTJ<3> data input.
	WRH	x	O	DIG	External memory interface write high byte control output; takes priority over digital I/O.
RJ4/BA0	RJ4	0	O	DIG	LATJ<4> data output.
		1	I	ST	PORTJ<4> data input.
	BA0	x	O	DIG	External Memory Interface Byte Address 0 control output; takes priority over digital I/O.
RJ5/CE	RJ5	0	O	DIG	LATJ<5> data output.
		1	I	ST	PORTJ<5> data input.
	CE	x	O	DIG	External memory interface chip enable control output; takes priority over digital I/O.
RJ6/LB	RJ6	0	O	DIG	LATJ<6> data output.
		1	I	ST	PORTJ<6> data input.
	LB	x	O	DIG	External memory interface lower byte enable control output; takes priority over digital I/O.
RJ7/UB	RJ7	0	O	DIG	LATJ<7> data output.
		1	I	ST	PORTJ<7> data input.
	UB	x	O	DIG	External memory interface upper byte enable control output; takes priority over digital I/O.

Legend: O = Output, I = Input, DIG = Digital Output, ST = Schmitt Buffer Input,
x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 11-18: SUMMARY OF REGISTERS ASSOCIATED WITH PORTJ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
PORTJ	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	66
LATJ	LATJ Output Latch Register								66
TRISJ	PORTJ Data Direction Register								65

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REGISTER 18-1: TXSTA1: EUSART1 TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN ⁽¹⁾	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)
- bit 6 **TX9:** 9-Bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission
- bit 5 **TXEN:** Transmit Enable bit⁽¹⁾
1 = Transmit is enabled
0 = Transmit is disabled
- bit 4 **SYNC:** AUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode
- bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care.
- bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode.
- bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR is empty
0 = TSR is full
- bit 0 **TX9D:** 9th bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

19.4 AUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTA2<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the CK2 pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

19.4.1 AUSART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes are identical except in the case of the Sleep mode.

If two words are written to the TXREG2 and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- The second word will remain in TXREG2 register.
- Flag bit, TX2IF, will not be set.
- When the first word has been shifted out of TSR, the TXREG2 register will transfer the second word to the TSR and flag bit, TX2IF, will now be set.
- If enable bit, TX2IE, is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
- Clear bits, CREN and SREN.
- If interrupts are desired, set enable bit, TX2IE.
- If 9-bit transmission is desired, set bit, TX9.
- Enable the transmission by setting enable bit, TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- Start transmission by loading data to the TXREG2 register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 19-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	63
PIR3	—	—	RC2IF	TX2IF	—	—	—	CCP3IF	65
PIE3	—	—	RC2IE	TX2IE	—	—	—	CCP3IE	65
IPR3	—	—	RC2IP	TX2IP	—	—	—	CCP3IP	65
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	66
TXREG2	AUSART2 Transmit Register								66
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	66
SPBRG2	AUSART2 Baud Rate Generator Register Low Byte								66

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

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REGISTER 20-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0

bit 7

bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

ADFM: A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6

Unimplemented: Read as '0'

bit 5-3

ACQT<2:0>: A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD⁽¹⁾

bit 2-0

ADCS<2:0>: A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)⁽¹⁾

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)⁽¹⁾

010 = FOSC/32

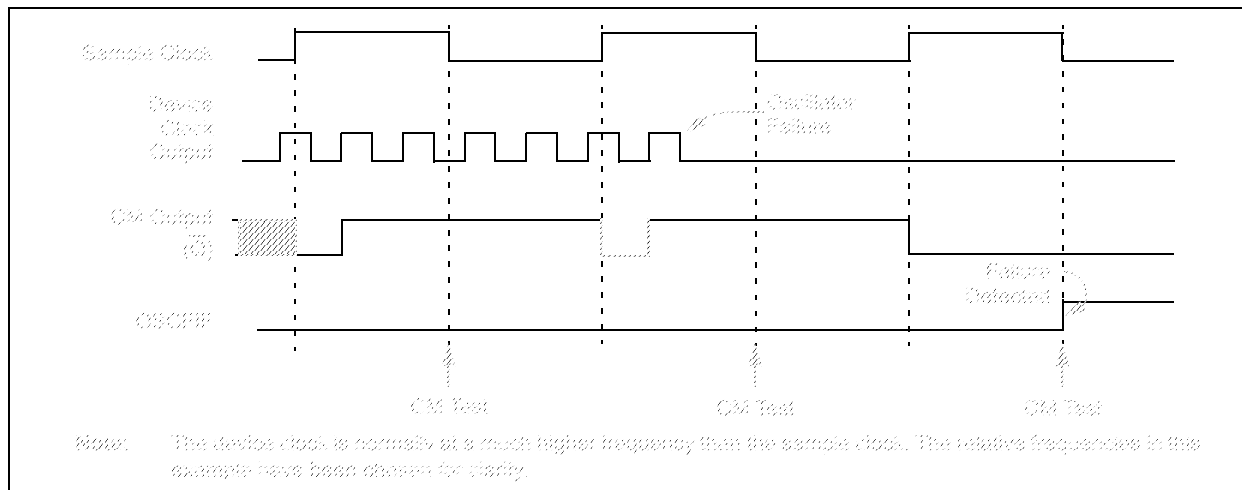
001 = FOSC/8

000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one T_{CY} (instruction cycle) is added before the A/D clock starts. This allows the **SLEEP** instruction to be executed before starting a conversion.

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FIGURE 24-4: FSCM TIMING DIAGRAM



24.4.3 FSCM INTERRUPTS IN POWER-MANAGED MODES

By entering a power-managed mode, the clock multiplexer selects the clock source selected by the OSCCON register. Fail-Safe Clock monitoring of the power-managed clock source resumes in the power-managed mode.

If an oscillator failure occurs during power-managed operation, the subsequent events depend on whether or not the oscillator failure interrupt is enabled. If enabled (OSCFIF = 1), code execution will be clocked by the INTOSC multiplexer. An automatic transition back to the failed clock source will not occur.

If the interrupt is disabled, the device will not exit the power-managed mode on oscillator failure. Instead, the device will continue to operate as before, but clocked by the INTOSC multiplexer. While in Idle mode, subsequent interrupts will cause the CPU to begin executing instructions while being clocked by the INTOSC multiplexer.

24.4.4 POR OR WAKE FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary device clock is in EC, RC or INTRC modes, monitoring can begin immediately following these events.

For oscillator modes involving a crystal or resonator (HS, HSPLL, LP or XT), the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FSCM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the device clock and functions until the primary clock is stable (the OST and PLL timers have timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note: The same logic that prevents false oscillator failure interrupts on POR, or wake from Sleep, will also prevent the detection of the oscillator's failure to start at all following these events. This can be avoided by monitoring the OSTS bit and using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

As noted in **Section 24.3.1 "Special Considerations for Using Two-Speed Start-up"**, it is also possible to select another clock configuration and enter an alternate power-managed mode while waiting for the primary clock to become stable. When the new powered-managed mode is selected, the primary clock is disabled.

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CPFSGT Compare f with W, skip if f > W

Syntax: CPFSGT f{,a}

Operands: $0 \leq f \leq 255$
 $a \in [0,1]$

Operation: (f) – (W),
 skip if (f) > (W)
 (unsigned comparison)

Status Affected: None

Encoding:

0110	010a	ffff	ffff
------	------	------	------

Description: Compares the contents of data memory location 'f' to the contents of the W by performing an unsigned subtraction. If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 25.2.3** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

```

HERE      CPFSGT REG, 0
NGREATER  :
GREATER   :
```

Before Instruction

```

PC      = Address (HERE)
W       = ?
```

After Instruction

```

If REG  > W;
PC      = Address (GREATER)
If REG  ≤ W;
PC      = Address (NGREATER)
```

CPFSLT Compare f with W, skip if f < W

Syntax: CPFSLT f{,a}

Operands: $0 \leq f \leq 255$
 $a \in [0,1]$

Operation: (f) – (W),
 skip if (f) < (W)
 (unsigned comparison)

Status Affected: None

Encoding:

0110	000a	ffff	ffff
------	------	------	------

Description: Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

```

HERE      CPFSLT REG, 1
NLESS    :
LESS     :
```

Before Instruction

```

PC      = Address (HERE)
W       = ?
```

After Instruction

```

If REG  < W;
PC      = Address (LESS)
If REG  ≥ W;
PC      = Address (NLESS)
```

25.2 Extended Instruction Set

In addition to the standard 75 instructions of the PIC18 instruction set, PIC18F6310/6410/8310/8410 devices also provide an optional extension to the core CPU functionality. The added features include eight additional instructions that augment Indirect and Indexed Addressing operations and the implementation of Indexed Literal Offset Addressing for many of the standard PIC18 instructions.

The additional features of the extended instruction set are disabled by default. To enable them, users must set the XINST Configuration bit.

The instructions in the extended set can all be classified as literal operations which either manipulate the File Select Registers, or use them for Indexed Addressing. Two of the instructions, ADDFSR and SUBFSR, each have an additional special instantiation for using FSR2. These versions (ADDULNK and SUBULNK) allow for automatic return after execution.

The extended instructions are specifically implemented to optimize re-entrant program code (that is, code that is recursive or that uses a software stack) written in high-level languages, particularly C. Among other things, they allow users working in high-level languages to perform certain operations on data structures more efficiently. These include:

- dynamic allocation and de-allocation of software stack space when entering and leaving subroutines
- Function Pointer invocation
- Software Stack Pointer manipulation
- manipulation of variables located in a software stack

A summary of the instructions in the extended instruction set is provided in Table 25-3. Detailed descriptions are provided in **Section 25.2.2 “Extended Instruction Set”**. The opcode field descriptions in Table 25-1 (page 298) apply to both the standard and extended PIC18 instruction sets.

Note: The instruction set extension and the Indexed Literal Offset Addressing mode were designed for optimizing applications written in C; the user may likely never use these instructions directly in assembler. The syntax for these commands is provided as a reference for users who may be reviewing code that has been generated by a compiler.

25.2.1 EXTENDED INSTRUCTION SYNTAX

Most of the extended instructions use indexed arguments, using one of the File Select Registers and some offset to specify a source or destination register. When an argument for an instruction serves as part of Indexed Addressing, it is enclosed in square brackets (“[]”). This is done to indicate that the argument is used as an index or offset. The MPASM Assembler will flag an error if it determines that an index or offset value is not bracketed.

When the extended instruction set is enabled, brackets are also used to indicate index arguments in byte-oriented and bit-oriented instructions. This is in addition to other changes in their syntax. For more details, see **Section 25.2.3.1 “Extended Instruction Syntax with Standard PIC18 Commands”**.

Note: In the past, square brackets have been used to denote optional arguments in the PIC18 and earlier instruction sets. In this text and going forward, optional arguments are denoted by braces (“{ }”).

TABLE 25-3: EXTENSIONS TO THE PIC18 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected
			MSb		LSb		
ADDFSR f, k	Add Literal to FSR	1	1110	1000	ffkk	kkkk	None
ADDULNK k	Add Literal to FSR2 and Return	2	1110	1000	11kk	kkkk	None
CALLW	Call Subroutine using WREG	2	0000	0000	0001	0100	None
MOVSF z _s , f _d	Move z _s (source) to 1st word f _d (destination) 2nd word	2	1110	1011	0zzz	zzzz	None
MOVSS z _s , z _d	Move z _s (source) to 1st word z _d (destination) 2nd word	2	1110	1011	1zzz	zzzz	None
PUSHL k	Store Literal at FSR2, Decrement FSR2	1	1110	1010	kkkk	kkkk	None
SUBFSR f, k	Subtract Literal from FSR	1	1110	1001	ffkk	kkkk	None
SUBULNK k	Subtract Literal from FSR2 and Return	2	1110	1001	11kk	kkkk	None

Note: All PIC18 instructions may take an optional label argument, preceding the instruction mnemonic, for use in symbolic addressing. If a label is used, the instruction syntax then becomes:
{label} instruction argument(s)

PIC18F6310/6410/8310/8410

SUBFSR Subtract Literal from FSR

Syntax: SUBFSR f, k
Operands: $0 \leq k \leq 63$
 $f \in [0, 1, 2]$
Operation: $FSRf - k \rightarrow FSRf$
Status Affected: None
Encoding:

1110	1001	ffkk	kkkk
------	------	------	------

Description: The 6-bit literal 'k' is subtracted from the contents of the FSR specified by 'f'.
Words: 1
Cycles: 1
Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: SUBFSR 2, 23h

Before Instruction

FSR2 = 03FFh

After Instruction

FSR2 = 03DCh

SUBULNK Subtract Literal from FSR2 and Return

Syntax: SUBULNK k
Operands: $0 \leq k \leq 63$
Operation: $FSR2 - k \rightarrow FSR2$
(TOS) $\rightarrow PC$
Status Affected: None
Encoding:

1110	1001	11kk	kkkk
------	------	------	------

Description: The 6-bit literal 'k' is subtracted from the contents of the FSR2. A RETURN is then executed by loading the PC with the TOS.

The instruction takes two cycles to execute; a NOP is performed during the second cycle.

This may be thought of as a special case of the SUBFSR instruction, where $f = 3$ (binary '11'); it operates only on FSR2.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination
No Operation	No Operation	No Operation	No Operation

Example: SUBULNK 23h

Before Instruction

FSR2 = 03FFh

PC = 0100h

After Instruction

FSR2 = 03DCh

PC = (TOS)

PIC18F6310/6410/8310/8410

FIGURE 27-7: CLKO AND I/O TIMING

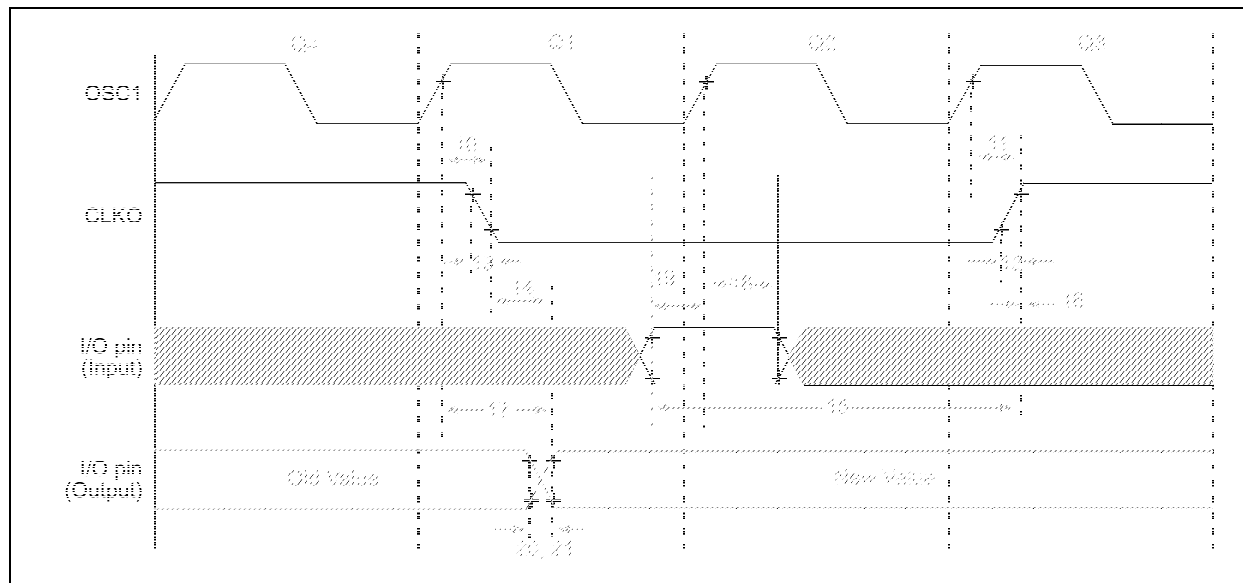


TABLE 27-9: CLKO AND I/O TIMING REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
10	TosH2ckL	OSC1 ↑ to CLK0 ↓		—	75	200	ns	(Note 1)
11	TosH2ckH	OSC1 ↑ to CLK0 ↑		—	75	200	ns	(Note 1)
12	TckR	CLK0 Rise Time		—	35	100	ns	(Note 1)
13	TckF	CLK0 Fall Time		—	35	100	ns	(Note 1)
14	TckL2ioV	CLK0 ↓ to Port Out Valid		—	—	0.5 Tcy + 20	ns	(Note 1)
15	TioV2ckH	Port In Valid before CLK0 ↑		0.25 Tcy + 25	—	—	ns	(Note 1)
16	TckH2ioI	Port In Hold after CLK0 ↑		0	—	—	ns	(Note 1)
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port Out Valid		—	50	150	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)	PIC18FXXXX	100	—	—	ns	VDD = 2.0V
18A			PIC18LFXXXX	200	—	—	ns	
19	TioV2osH	Port Input Valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20	TioR	Port Output Rise Time	PIC18FXXXX	—	10	25	ns	VDD = 2.0V
20A			PIC18LFXXXX	—	—	60	ns	
21	TioF	Port Output Fall Time	PIC18FXXXX	—	10	25	ns	VDD = 2.0V
21A			PIC18LFXXXX	—	—	60	ns	
22†	TINP	INTx pin High or Low Time		Tcy	—	—	ns	
23†	TRBP	RB<7:4> Change INTx High or Low Time		Tcy	—	—	ns	

† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode, where CLKO output is 4 x T_{osc}.

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FIGURE 27-14: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)

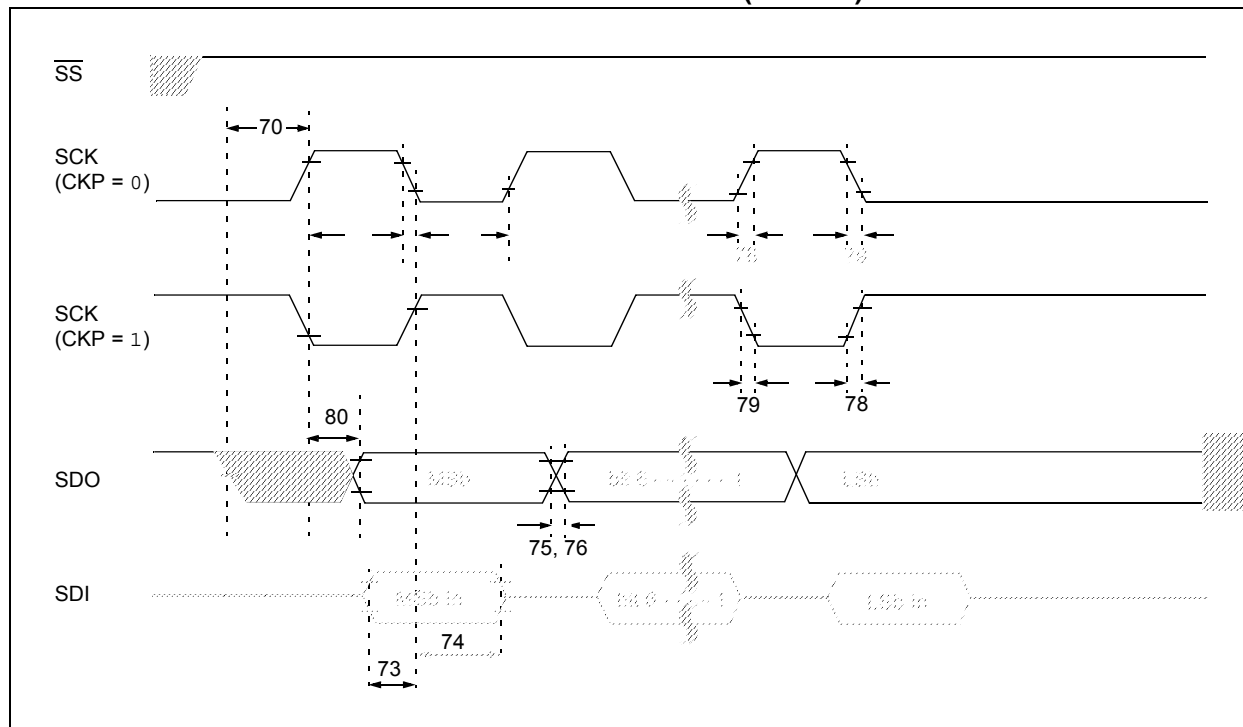


TABLE 27-15: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2sch, TssL2scL	$\overline{SS} \downarrow$ to SCK \downarrow or SCK \uparrow Input	Tcy	—	ns	
73	TdIV2sch, TdIV2scL	Setup Time of SDI Data Input to SCK Edge	100	—	ns	
74	Tsch2diL, TscL2diL	Hold Time of SDI Data Input to SCK Edge	40	—	ns	
75	TdoR	SDO Data Output Rise Time	PIC18FXXXX	25	ns	
			PIC18LFXXXX	45	ns	VDD = 2.0V
76	TdoF	SDO Data Output Fall Time	—	25	ns	
78	TscR	SCK Output Rise Time	PIC18FXXXX	25	ns	
			PIC18LFXXXX	45	ns	VDD = 2.0V
79	TscF	SCK Output Fall Time	—	25	ns	
80	Tsch2doV, TscL2doV	SDO Data Output Valid after SCK Edge	PIC18FXXXX	50	ns	
			PIC18LFXXXX	100	ns	VDD = 2.0V

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