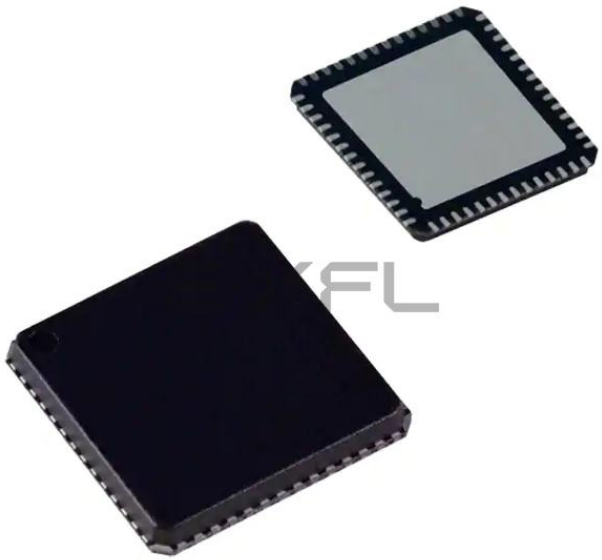

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 3x16b, 4x24b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc834bcpz

ADUC834* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

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EVALUATION KITS

- ADuC834 QuickStart Development System

DOCUMENTATION

Application Notes

- AN-1074: Understanding the Serial Download Protocol (Formerly uC004)
- AN-1139: Understanding the Parallel Programming Protocol
- AN-282: Fundamentals of Sampled Data Systems
- AN-644: Frequency Measurement Using Timer 2 on a MicroConverter ® (uC013)
- AN-645: Interfacing an HD44780 Character LCD to a MicroConverter ® (uC014)
- AN-660: XY-Matrix Keypad Interface to MicroConverter®
- AN-709: RTD Interfacing and Linearization Using an ADuC8xx MicroConverter®
- AN-759: Expanding the Number of DAC Outputs on the ADuC8xx and ADuC702x Families (uC012)
- UC-001: MicroConverter® I2C® Compatible Interface
- UC-002: Developing in C with the Keil uVision2 IDE
- UC-006: A 4-wire UART-to-PC Interface
- UC-007: User Download (ULOAD) Mode
- UC-008: Using the ADuC834 C-library
- UC-009: Addressing 16MB of External Data Memory
- UC-018: Uses of the Time Interval Counter

Data Sheet

- ADuC834: MicroConverter® Dual 16-/24- Bit SIgma-Delta ADCs with Embedded 62KB Flash MCU Data Sheet
- ADuC834: Silicon Errata Sheet

User Guides

- ADuC834 Quick Reference Guide
- UG-041: ADuC8xx Evaluation Kit Getting Started User Guide

TOOLS AND SIMULATIONS

- Sigma-Delta ADC Tutorial

REFERENCE MATERIALS

Technical Articles

- Integrated Route Taken to Pulse Oximetry

DESIGN RESOURCES

- ADUC834 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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TABLE OF CONTENTS

Parameter	ADuC834	Test Conditions/Comments	Unit
TRANSDUCER BURNOUT CURRENT SOURCES			
AIN+ Current	–100	AIN+ Is the Selected Positive Input to the Primary ADC	nA typ
AIN– Current	+100	AIN– Is the Selected Negative Input to the Auxiliary ADC	nA typ
Initial Tolerance @ 25°C	±10		% typ
Drift	0.03		%/°C typ
EXCITATION CURRENT SOURCES			
Output Current	–200	Available from Each Current Source	μA typ
Initial Tolerance @ 25°C	±10		% typ
Drift	200		ppm/°C typ
Initial Current Matching @ 25°C	±1	Matching between Both Current Sources	% typ
Drift Matching	20		ppm/°C typ
Line Regulation (AV_{DD})	1	AV_{DD} = 5 V + 5%	μA/V typ
Load Regulation	0.1		μA/V typ
Output Compliance[2]	AV_{DD} – 0.6		V max
	AGND		min
LOGIC INPUTS			
All Inputs Except SCLOCK, RESET, and XTAL1[2]			
V_{INL}, Input Low Voltage	0.8	DV_{DD} = 5 V	V max
	0.4	DV_{DD} = 3 V	V max
V_{INH}, Input High Voltage	2.0		V min
SCLOCK and RESET Only (Schmitt-Triggered Inputs)[2]			
V_{T+}	1.3/3	DV_{DD} = 5 V	V min/V max
	0.95/2.5	DV_{DD} = 3 V	V min/V max
V_{T-}	0.8/1.4	DV_{DD} = 5 V	V min/V max
	0.4/1.1	DV_{DD} = 3 V	V min/V max
$V_{T+} - V_{T-}$	0.3/0.85	DV_{DD} = 5 V	V min/V max
	0.3/0.85	DV_{DD} = 3 V	V min/V max
Input Currents			
Port 0, P1.2–P1.7, $\overline{EA}$	±10	V_{IN} = 0 V or V_{DD}	μA max
SCLOCK, MOSI, MISO, $\overline{SS}$[13]	–10 min, –40 max	V_{IN} = 0 V, DV_{DD} = 5 V, Internal Pull-Up	μA min/μA max
	±10	V_{IN} = V_{DD}, DV_{DD} = 5 V	μA max
RESET	±10	V_{IN} = 0 V, DV_{DD} = 5 V	μA max
	35 min, 105 max	V_{IN} = V_{DD}, DV_{DD} = 5 V, Internal Pull-Down	μA min/μA max
P1.0, P1.1, Ports 2 and 3	±10	V_{IN} = V_{DD}, DV_{DD} = 5 V	μA max
	–180	V_{IN} = 2 V, DV_{DD} = 5 V	μA min
	–660		μA max
	–20	V_{IN} = 450 mV, DV_{DD} = 5 V	μA min
	–75		μA max
Input Capacitance	5	All Digital Inputs	pF typ
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)			
Logic Inputs, XTAL1 Only[2]			
V_{INL}, Input Low Voltage	0.8	DV_{DD} = 5 V	V max
	0.4	DV_{DD} = 3 V	V max
V_{INH}, Input High Voltage	3.5	DV_{DD} = 5 V	V min
	2.5	DV_{DD} = 3 V	V min
XTAL1 Input Capacitance	18		pF typ
XTAL2 Output Capacitance	18		pF typ

SPECIFICATIONS (continued)

Parameter	ADuC834	Test Conditions/Comments	Unit
LOGIC OUTPUTS (Not Including XTAL2)[2]			
V_{OH}, Output High Voltage	2.4	V_{DD} = 5 V, I_{SOURCE} = 80 μA	V min
	2.4	V_{DD} = 3 V, I_{SOURCE} = 20 μA	V min
V_{OL}, Output Low Voltage[14]	0.4	I_{SINK} = 8 mA, SCLOCK, MOSI/SDATA	V max
	0.4	I_{SINK} = 10 mA, P1.0 and P1.1	V max
	0.4	I_{SINK} = 1.6 mA, All Other Outputs	V max
Floating State Leakage Current[2]	±10		μA max
Floating State Output Capacitance	5		pF typ
POWER SUPPLY MONITOR (PSM)			
AV_{DD} Trip Point Selection Range	2.63	Four Trip Points Selectable in This Range	V min
	4.63	Programmed via TPA1–0 in PSMCON	V max
AV_{DD} Power Supply Trip Point Accuracy	±3.0	T_{MAX} = 85°C	% max
	±4.0	T_{MAX} = 125°C	% max
DV_{DD} Trip Point Selection Range	2.63	Four Trip Points Selectable in This Range	V min
	4.63	Programmed via TPD1–0 in PSMCON	V max
DV_{DD} Power Supply Trip Point Accuracy	±3.0	T_{MAX} = 85°C	% max
	±4.0	T_{MAX} = 125°C	% max
WATCHDOG TIMER (WDT)			
Timeout Period	0	Nine Timeout Periods in This Range	ms min
	2000	Programmed via PRE3–0 in WDCON	ms max
MCU CORE CLOCK RATE		Clock Rate Generated via On-Chip PLL	
MCU Clock Rate[2]	98.3	Programmable via CD2–0 Bits in PLLCON SFR	kHz min
	12.58		MHz max
START-UP TIME			
At Power-On	300		ms typ
After External RESET in Normal Mode	3		ms typ
After WDT Reset in Normal Mode	3	Controlled via WDCON SFR	ms typ
From Idle Mode	10		μs typ
From Power-Down Mode			
Oscillator Running		OSC_PD Bit = 0 in PLLCON SFR	
Wake-Up with $\overline{INT0}$ Interrupt	20		μs typ
Wake-Up with SPI Interrupt	20		μs typ
Wake-Up with TIC Interrupt	20		μs typ
Wake-Up with External RESET	3		ms typ
Oscillator Powered Down		OSC_PD Bit = 1 in PLLCON SFR	
Wake-Up with $\overline{INT0}$ Interrupt	20		μs typ
Wake-Up with SPI Interrupt	20		μs typ
Wake-Up with External RESET	5		ms typ
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[15]			
Endurance[16]	100,000		Cycles min
Data Retention[17]	100		Years min

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

AV_{DD} to AGND	–0.3 V to +7 V
AV_{DD} to DGND	–0.3 V to +7 V
DV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
AGND to DGND[2]	–0.3 V to +0.3 V
AV_{DD} to DV_{DD}	–2 V to +5 V
Analog Input Voltage to AGND[3]	–0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (MQFP)	90°C/W
θ_{JA} Thermal Impedance (LFCSP Base Floating)	52°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

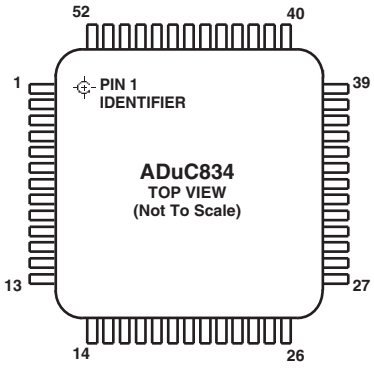
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]AGND and DGND are shorted internally on the ADuC834.

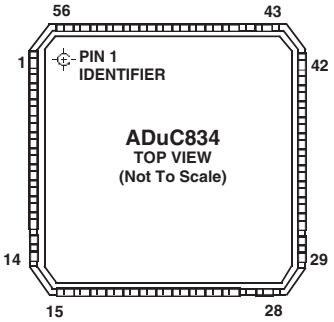
[3]Applies to P1.2 to P1.7 pins operating in analog or digital input modes.

PIN CONFIGURATION

52-Lead MQFP



56-Lead LFCSP



NOTES

1. EXPOSED PAD. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO THE METAL PLATE ON THE PCB AND TO DGND.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADuC834 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

When accessing the internal XRAM, the P0 and P2 port pins, as well as the $\overline{RD}$ and $\overline{WR}$ strobes, will not be output as per a standard 8051 MOVX instruction. This allows the user to use these port pins as standard I/O.

The upper 1792 bytes of the internal XRAM can be configured to be used as an extended 11-bit stack pointer. By default, the stack will operate exactly like an 8052 in that it will roll over from FFH to 00H in the general-purpose RAM. On the ADuC834 however, it is possible (by setting CFG834.7) to enable the 11-bit extended stack pointer. In this case, the stack will roll over from FFH in RAM to 0100H in XRAM. The 11-bit stack pointer is visible in the SP and SPH SFRs. The SP SFR is located at 81H as with a standard 8052. The SPH SFR is located at B7H. The 3 LSBs of this SFR contain the three extra bits necessary to extend the 8-bit stack pointer into an 11-bit stack pointer.

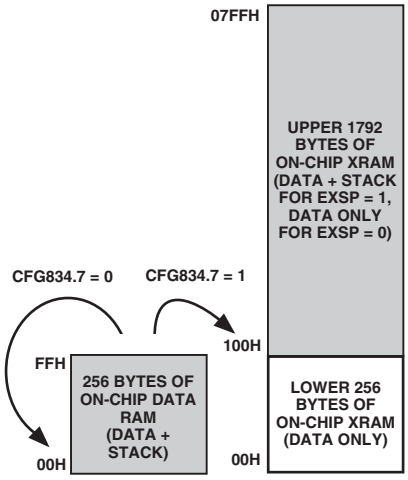


Figure 4. Extended Stack Pointer Operation

External Data Memory (External XRAM)
Just like a standard 8051 compatible core, the ADuC834 can access external data memory using a MOVX instruction. The MOVX instruction automatically outputs the various control strobes required to access the data memory.

The ADuC834 however, can access up to 16 Mbytes of external data memory. This is an enhancement of the 64 Kbytes external data memory space available on a standard 8051 compatible core.

The external data memory is discussed in more detail in the ADuC834 Hardware Design Considerations section.

SPECIAL FUNCTION REGISTERS (SFRS)
The SFR space is mapped into the upper 128 bytes of internal data memory space and accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC834 via the SFR area is shown in Figure 5.

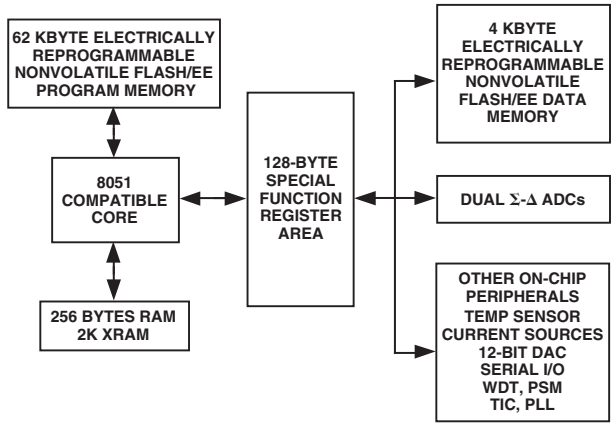


Figure 5. Programming Model

All registers, except the Program Counter (PC) and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

Accumulator SFR (ACC)
ACC is the Accumulator Register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the Accumulator as A.

B SFR (B)
The B Register is used with the ACC for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratchpad register.

Data Pointer (DPTR)
The Data Pointer is made up of three 8-bit registers, named DPP (page byte), DPH (high byte) and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions will automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL).

The ADuC834 supports dual data pointers. Refer to the Dual Data Pointer section in this data sheet.

Stack Pointer (SP and SPH)
The SP SFR is the stack pointer and is used to hold an internal RAM address that is called the 'top of the stack.' The SP Register is incremented before data is stored during PUSH and CALL executions. While the Stack may reside anywhere in on-chip RAM, the SP Register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

As mentioned earlier, the ADuC834 offers an extended 11-bit stack pointer. The three extra bits to make up the 11-bit stack pointer are the 3 LSBs of the SPH byte located at B7H.

Program Status Word (PSW)
The PSW SFR contains several bits reflecting the current status of the CPU as detailed in Table I.

SFR Address	D0H
Power-On Default Value	00H
Bit Addressable	Yes

Table I. PSW SFR Bit Designations

Bit	Name	Description		
7	CY	Carry Flag		
6	AC	Auxiliary Carry Flag		
5	F0	General-Purpose Flag		
4	RS1	Register Bank Select Bits		
3	RS0	RS1	RS0	Selected Bank
		0	0	0
		0	1	1
		1	0	2
		1	1	3
2	OV	Overflow Flag		
1	F1	General-Purpose Flag		
0	P	Parity Bit		

Power Control SFR (PCON)
The PCON SFR contains bits for power-saving options and general-purpose status flags as shown in Table II.

The TIC (wake-up/RTC timer) can be used to accurately wake up the ADuC834 from power-down at regular intervals. To use the TIC to wake up the ADuC834 from power-down, the OSC_PD bit in the PLLCON SFR must be clear and the TIC must be enabled.

SFR Address	87H
Power-On Default Value	00H
Bit Addressable	No

Table II. PCON SFR Bit Designations

Bit	Name	Description
7	SMOD	Double UART Baud Rate
6	SERIPD	SPI Power-Down Interrupt Enable
5	INT0PD	$\overline{\text{INT0}}$ Power-Down Interrupt Enable
4	ALEOFF	Disable ALE Output
3	GF1	General-Purpose Flag Bit
2	GF0	General-Purpose Flag Bit
1	PD	Power-Down Mode Enable
0	IDL	Idle Mode Enable

ADuC834 CONFIGURATION SFR (CFG834)
The CFG834 SFR contains the necessary bits to configure the internal XRAM and the extended SP. By default it configures the user into 8051 mode, i.e., extended SP is disabled, internal XRAM is disabled.

SFR Address	AFH
Power-On Default Value	00H
Bit Addressable	No

Table III. CFG834 SFR Bit Designations

Bit	Name	Description
7	EXSP	Extended SP Enable. If this bit is set, the stack will roll over from SPH/SP = 00FFH to 0100H. If this bit is clear, the SPH SFR will be disabled and the stack will roll over from SP = FFH to SP = 00H
6	—	Reserved for Future Use
5	—	Reserved for Future Use
4	—	Reserved for Future Use
3	—	Reserved for Future Use
2	—	Reserved for Future Use
1	—	Reserved for Future Use
0	XRAMEN	XRAM Enable Bit. If this bit is set, the internal XRAM will be mapped into the lower 2 Kbytes of the external address space. If this bit is clear, the internal XRAM will not be accessible and the external data memory will be mapped into the lower 2 Kbytes of external data memory. (See Figure 3.)

COMPLETE SFR MAP

Figure 6 shows a full SFR memory map and the SFR contents after RESET. NOT USED indicates unoccupied SFR locations. Unoccupied locations in the SFR address space are not implemented; i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations that are reserved for future use are shaded (RESERVED) and should not be accessed by user software.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RSI D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH	PT0 B9H 0	PX0 B8H 0	BITS
$\overline{RD}$ B7H 1	$\overline{WR}$ B6H 1	T1 B5H 1	T0 B4H 1	$\overline{INT1}$ B3H 1	$\overline{INT0}$ B2H 1	TXD B1H 1	RXD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	T1 99H 0	R1 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

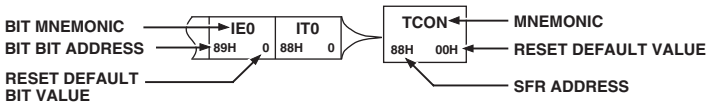
SPICON F8H 04H	RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
B F0H 00H	RESERVED	RESERVED	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
I2CCON E8H 00H	GN0L[1] E9H 55H	GN0M[1] EAH 55H	GN0H[1] EBH 53H	GN1L[1] ECH 9AH	GN1H[1] EDH 59H	RESERVED	RESERVED
ACC E0H 00H	OF0L E1H 00H	OF0M E2H 00H	OF0H E3H 80H	OF1L E4H 00H	OF1H E5H 80H	RESERVED	RESERVED
ADCSTAT D8H 00H	ADC0L D9H 00H	ADC0M DAH 00H	ADC0H DBH 00H	ADC1L DCH 00H	ADC1H DDH 00H	RESERVED	PSMCON DFH DEH
PSW D0H 00H	ADCMODE D1H 00H	ADC0CON D2H 07H	ADC1CON D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 03H
T2CON C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON C0H 10H	RESERVED	CHIPID C2H 2×H	RESERVED	RESERVED	RESERVED	EADRL C6H 00H	EADRH C7H 00H
IP B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3 B0H FFH	PWM0L B1H 00H	PWM0H B2H 00H	PWM1L B3H 00H	PWM1H B4H 00H	RESERVED	RESERVED	SPH B7H 00H
IE A8H 00H	IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	PWMCON AEH 00H	CFG834 AFH 00H
P2 A0H FFH	TIMECON A1H 00H	HTHSEC[2] A2H 00H	SEC[2] A3H 00H	MIN[2] A4H 00H	HOUR[2] A5H 00H	INTVAL A6H 00H	DPCON A7H 00H
SCON 98H 00H	SBUF 99H 00H	RESERVED	RESERVED	NOT USED	T3FD 9DH 00H	T3CON 9EH 00H	RESERVED
P1 90H FFH	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
TCON 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

NOTES

[1]CALIBRATION COEFFICIENTS ARE PRECONFIGURED AT POWER-UP TO FACTORY CALIBRATED VALUES.

[2]THESE SFRS MAINTAIN THEIR PRERESET VALUES AFTER A RESET IF TIMECON.0 = 1.

SFR MAP KEY:



SFR NOTE:
SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT-ADDRESSABLE.

Figure 6. Special Function Register Locations and Their Reset Default Values

PRIMARY AND AUXILIARY ADC NOISE PERFORMANCE

Tables X, XI, and XII show the output rms noise in μV and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates on both the primary and auxiliary ADCs. The numbers are typical and are generated at a differential input voltage of 0 V. The output update rate is selected via the Sinc Filter (SF) SFR. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit.

The QuickStart Development system PC software comes complete with an ADC noise evaluation tool. This tool can be easily used with the evaluation board to see these figures from silicon.

Table X. Primary ADC, Typical Output RMS Noise (μV)
Typical Output RMS Noise vs. Input Range and Update Rate; Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table XI. Primary ADC, Peak-to-Peak Resolution (Bits)
Peak-to-Peak Resolution vs. Input Range and Update Rate; Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13.5	14	15	16	17	17.5	18	18.5
255	5.35	14	15	16	17	18	18.5	19	19.5

Typical RMS Resolution vs. Input Range and Update Rate: RMS Resolution in Bits*

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	14.7	15.7	16.7	17.7	17.7	18.2	18.7	18.7
69	19.79	16.2	16.7	17.7	18.7	19.7	20.2	20.7	21.2
255	5.35	16.7	17.7	18.7	19.7	20.7	21.2	21.7	22.2

*Based on a six-sigma limit, the rms resolution is 2.7 bits greater than the peak-to-peak resolution.

Table XII. Auxiliary ADC

Typical Output RMS Noise vs. Update Rate*
Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range 2.5 V
13	105.3	10.75
69	19.79	2.00
255	5.35	1.15

*ADC converting in Bipolar mode

Peak-to-Peak Resolution vs. Update Rate[1]
Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range 2.5 V
13	105.3	16[2]
69	19.79	16
255	5.35	16

NOTES
[1]ADC converting in Bipolar mode
[2]In Unipolar mode, peak-to-peak resolution at 105 Hz is 15 bits.

Reference Input

The ADuC834's reference inputs, REFIN(+) and REFIN(–), provide a differential reference input capability. The common-mode range for these differential inputs is from AGND to AV_{DD}. The nominal reference voltage, V_{REF} (REFIN(+) – REFIN(–)), for specified operation is 2.5 V with the primary and auxiliary reference enable bits set in the respective ADC0CON and/or ADC1CON SFRs.

The part is also functional (although not specified for performance) when the XREF0 or XREF1 bits are 0, which enables the on-chip internal band gap reference. In this mode, the ADCs will see the internal reference of 1.25 V, therefore halving all input ranges. As a result of using the internal reference voltage, a noticeable degradation in peak-to-peak resolution will result. Therefore, for best performance, operation with an external reference is strongly recommended.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed as the application is ratiometric. If the ADuC834 is not used in a ratiometric application, a low noise reference should be used. Recommended reference voltage sources for the ADuC834 include the AD780, REF43, and REF192.

It should also be noted that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources, like those recommended above (e.g., AD780), will typically have low output impedances and therefore decoupling capacitors on the REFIN(+) input would be recommended. Deriving the reference input voltage across an external resistor, as shown in Figure 66, will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN(+) and REFIN(–) pins would not be recommended in this type of circuit configuration.

Burnout Currents

The primary ADC on the ADuC834 contains two 100 nA constant current generators, one sourcing current from AV_{DD} to AIN(+), and one sinking from AIN(–) to AGND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the Burnout Current Enable (BO) bit in the ICON SFR (see Table IX). These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. Once the burnout currents are turned on, they will flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resultant voltage measured is full-scale, it indicates that the transducer has gone open-circuit. If the voltage measured is 0 V, it indicates that the transducer has short circuited. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit in the ICON SFR. The current sources work over the normal absolute input voltage range specifications.

Excitation Currents

The ADuC834 also contains two identical, 200 μA constant current sources. Both source current from AV_{DD} to Pin 3 (IEXC1) or Pin 4 (IEXC2). These current sources are controlled via bits in the ICON SFR shown in Table IX. They can be configured to source 200 μA individually to both pins or a combination of both currents, i.e., 400 μA, to either of the selected pins. These current sources can be used to excite external resistive bridge or RTD sensors.

Reference Detect

The ADuC834 includes on-chip circuitry to detect if the part has a valid reference for conversions or calibrations. If the voltage between the external REFIN(+) and REFIN(–) pins goes below 0.3 V or either the REFIN(+) or REFIN(–) inputs is open circuit, the ADuC834 detects that it no longer has a valid reference. In this case, the NOXREF bit of the ADCSTAT SFR is set to a 1. If the ADuC834 is performing normal conversions and the NOXREF bit becomes active, the conversion results revert to all 1s. It is not necessary to continuously monitor the status of the NOXREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC Data Register is all 1s.

If the ADuC834 is performing either an offset or gain calibration and the NOXREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the appropriate ERR0 or ERR1 bits in the ADCSTAT SFR are set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR0 or ERR1 bit should be checked at the end of the calibration cycle.

Σ-Δ Modulator

A Σ-Δ ADC generally consists of two main blocks, an analog modulator and a digital filter. In the case of the ADuC834 ADCs, the analog modulators consist of a difference amplifier, an integrator block, a comparator, and a feedback DAC as illustrated in Figure 10.

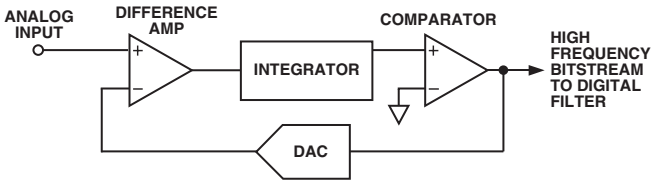


Figure 10. Σ-Δ Modulator Simplified Block Diagram

PWM MODES OF OPERATION

Mode 0: PWM Disabled

The PWM is disabled, allowing P1.0 and P1.1 be used as normal.

Mode 1: Single-Variable Resolution PWM

In Mode 1, both the pulse length and the cycle time (period) are programmable in user code, allowing the resolution of the PWM to be variable.

PWM1H/L sets the period of the output waveform. Reducing PWM1H/L reduces the resolution of the PWM output but increases the maximum output rate of the PWM (e.g., setting PWM1H/L to 65536 gives a 16-bit PWM with a maximum output rate of 192 Hz (12.583 MHz/65536). Setting PWM1H/L to 4096 gives a 12-bit PWM with a maximum output rate of 3072 Hz (12.583 MHz/4096)).

PWM0H/L sets the duty cycle of the PWM output waveform, as shown in Figure 27.

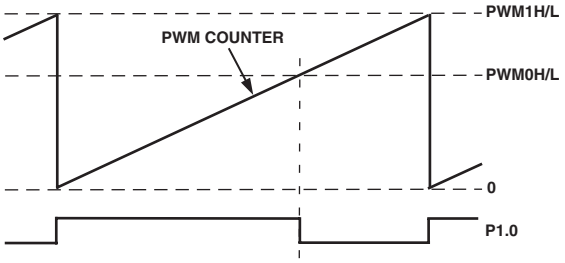


Figure 27. PWM in Mode 1

Mode 2: Twin 8-Bit PWM

In Mode 2, the duty cycle of the PWM outputs and the resolution of the PWM outputs are both programmable. The maximum resolution of the PWM output is eight bits.

PWM1L sets the period for both PWM outputs. Typically this will be set to 255 (FFh) to give an 8-bit PWM, although it is possible to reduce this as necessary. A value of 100 could be loaded here to give a percentage PWM (i.e., the PWM is accurate to 1%).

The outputs of the PWM at P1.0 and P1.1 are shown in the diagram below. As can be seen, the output of PWM0 (P1.0) goes low when the PWM counter equals PWM0L. The output of PWM1 (P1.1) goes high when the PWM counter equals PWM1H and goes low again when the PWM counter equals PWM0H. Setting PWM1H to 0 ensures that both PWM outputs start simultaneously.

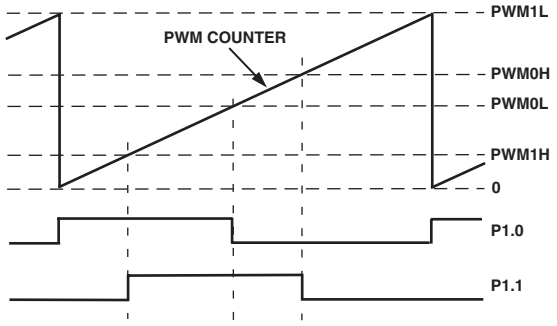


Figure 28. PWM Mode 2

Mode 3: Twin 16-Bit PWM

In Mode 3, the PWM counter is fixed to count from 0 to 65536 giving a fixed 16-bit PWM. Operating from the 12.58 MHz core clock results in a PWM output rate of 192 Hz. The duty cycle of the PWM outputs at P1.0 and P1.1 are independently programmable.

As shown below, while the PWM counter is less than PWM0H/L, the output of PWM0 (P1.0) is high. Once the PWM counter equals PWM0H/L, then PWM0 (P1.0) goes low and remains low until the PWM counter rolls over.

Similarly, while the PWM counter is less than PWM1H/L, the output of PWM1 (P1.1) is high. Once the PWM counter equals PWM1H/L, then PWM1 (P1.1) goes low and remains low until the PWM counter rolls over.

In this mode, both PWM outputs are synchronized (i.e., once the PWM counter rolls over to 0, both PWM0 (P1.0) and PWM1 (P1.1) will go high).

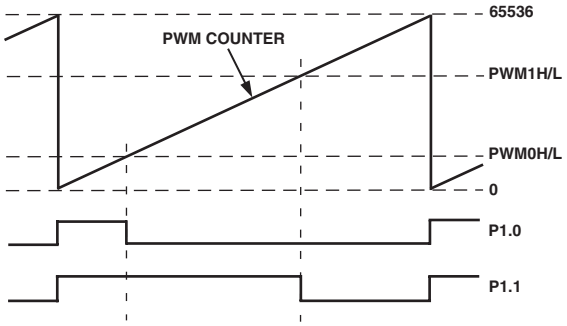


Figure 29. PWM Mode 3

TIME INTERVAL COUNTER (WAKE-UP/RTC TIMER)

A time interval counter (TIC) is provided on-chip for:

- periodically waking the part up from power-down
- implementing a Real-Time Clock
- counting longer intervals than the standard 8051 compatible timers are capable of

The TIC is capable of timeout intervals ranging from 1/128th second to 255 hours. Furthermore, this counter is clocked by the crystal oscillator rather than the PLL and thus has the ability to remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required.

The TIC counter can easily be used to generate a real-time clock. The hardware will count in seconds, minutes, and hours; however, user software will have to count in days, months, and years. The current time can be written to the timebase SFRs (HTHSEC, SEC, MIN, and HOUR) while TCEN is low. When the RTC timer is enabled (TCEN is set), the TCEN bit itself and the HTHSEC, SEC, MIN, and HOUR Registers are not reset to 00H after a hardware or watchdog timer reset. This is to prevent the need to recalibrate the real-time clock after a reset. However, these registers will be reset to 00H after a power cycle (independent of TCEN) or after any reset if TCEN is clear.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow will clock the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. (See IEIP2 SFR description under Interrupt System in this data sheet.) If the ADuC834 is in power-down mode, again with TIC interrupt enabled, the TII bit will wake up the device and resume code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described below with a block diagram of the TIC shown in Figure 33.

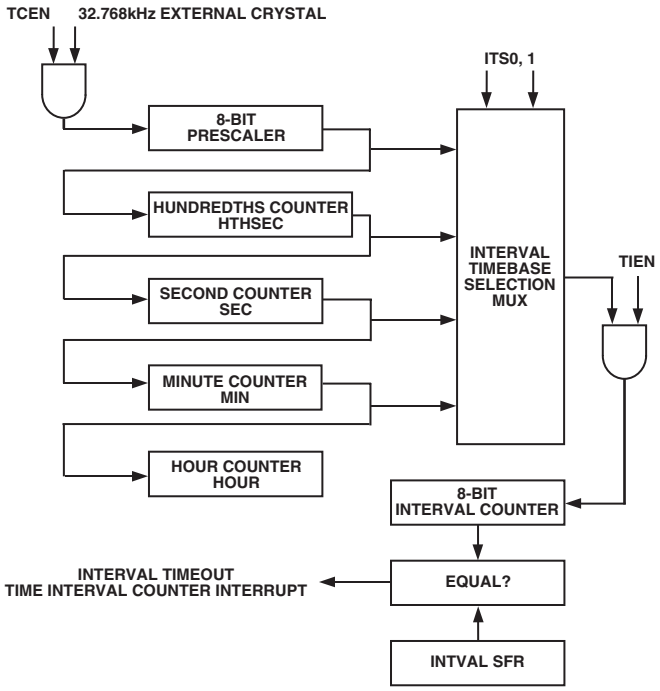


Figure 33. TIC, Simplified Block Diagram

Table XVIII. TIMECON SFR Bit Designations

Bit	Name	Description
7	—	Reserved for Future Use
6	—	Reserved for Future Use. For future product code compatibility, this bit should be written as a '1.'
5	ITS1	Interval Timebase Selection Bits
4	ITS0	Written by user to determine the interval counter update rate. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	STI	Single Time Interval Bit. Set by user to generate a single interval timeout. If set, a timeout will clear the TIEN bit. Cleared by user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. Set when the 8-bit Interval Counter matches the value in the INTVAL SFR. Cleared by user software.
1	TIEN	Time Interval Enable Bit. *Set* by user to enable the 8-bit time interval counter. Cleared by user to disable and clear the contents of the 8-bit interval counter. To ensure that the 8-bit interval counter is cleared TIEN must be held low for at least 30.5 μs (32 kHz).
0	TCEN	Time Clock Enable Bit. Set by user to enable the time clock to the time interval counters. Cleared by user to disable the 32 kHz clock to the TIC and clear the 8-bit prescaler and the HTHSEC, SEC, MIN and HOURS SFRs. To ensure that these registers are cleared, TCEN must be held low for at least 30.5 μs (32 kHz). The time registers (HTHSEC, SEC, MIN, and HOUR) can only be written while TCEN is low.

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC834 enters an erroneous state, possibly due to a programming error, electrical noise, or RFI. The watchdog function can be disabled by clearing the WDE (Watchdog Enable) bit in the Watchdog Control (WDCON) SFR. When enabled; the watchdog circuit will generate a system reset or interrupt (WDS) if the user program fails to set the Watchdog (WDE) bit within a predetermined amount of time (see PRE3–0 bits in WDCON). The watchdog timer itself is a 16-bit counter that is clocked at 32.768 kHz. The watchdog timeout interval can be adjusted via the PRE3–0 bits in WDCON. Full control and status of the watchdog timer function can be controlled via the Watchdog Timer Control SFR (WDCON). The WDCON SFR can only be written by user software if the double write sequence described in WDWR below is initiated on every write access to the WDCON SFR.

WDCON	**Watchdog Timer Control Register**
SFR Address	C0H
Power-On Default Value	10H
Bit Addressable	Yes

Table XIX. WDCON SFR Bit Designations

Bit	Name	Description
7	PRE3	Watchdog Timer Prescale Bits.
6	PRE2	The Watchdog timeout period is given by the equation: $t_{WD} = (2^{PRE} \times (2^9/f_{PLL}))$
5	PRE1	($0 \le PRE \le 7$; f_{PLL} = 32.768 kHz)
4	PRE0	PRE3 PRE2 PRE1 PRE0 Timeout Period (ms) Action 0 0 0 0 15.6 Reset or Interrupt 0 0 0 1 31.2 Reset or Interrupt 0 0 1 0 62.5 Reset or Interrupt 0 0 1 1 125 Reset or Interrupt 0 1 0 0 250 Reset or Interrupt 0 1 0 1 500 Reset or Interrupt 0 1 1 0 1000 Reset or Interrupt 0 1 1 1 2000 Reset or Interrupt 1 0 0 0 0.0 Immediate Reset PRE3–0 > 1001 Reserved
3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog will generate an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR $\overline{EA}$ instruction and it is also a fixed, high-priority interrupt. If the watchdog is not being used to monitor the system, it can alternatively be used as a timer. The prescaler is used to set the timeout period in which an interrupt will be generated. (See also Note 1, Table XXXIX in the Interrupt System section.)
2	WDS	Watchdog Status Bit. Set by the Watchdog Controller to indicate that a watchdog timeout has occurred. Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit. Set by user to enable the watchdog and clear its counters. If a 1 is not written to this bit within the watchdog timeout period, the watchdog will generate a reset or interrupt, depending on WDIR. Cleared under the following conditions, User writes 0, Watchdog Reset (WDIR = 0); Hardware Reset; PSM Interrupt.

0	WDWR	Watchdog Write Enable Bit.
		To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the very next instruction must be a write instruction to the WDCON SFR. For example:
		`CLR EA ; disable interrupts while writing`
		`; to WDT`
		`SETB WDWR ; allow write to WDCON`
		`MOV WDCON, #72h ; enable WDT for 2.0s timeout`
		`SETB EA ; enable interrupts again (if rqd)`

TCON **Timer/Counter 0 and 1 Control Register**
SFR Address 88H
Power-On Default Value 00H
Bit Addressable Yes

Table XXVII. TCON SFR Bit Designations

Bit	Name	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the Program Counter (PC) vectors to the interrupt service routine.
6	TR1	Timer 1 Run Control Bit. Set by user to turn on Timer/Counter 1. Cleared by user to turn off Timer/Counter 1.
5	TF0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	TR0	Timer 0 Run Control Bit. Set by user to turn on Timer/Counter 0. Cleared by user to turn off Timer/Counter 0.
3	IE1*	External Interrupt 1 ($\overline{INT1}$) Flag. Set by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT1}$, depending on bit IT1 state. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware.
2	IT1*	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge-sensitive detection (i.e., 1-to-0 transition). Cleared by software to specify level-sensitive detection (i.e., zero level).
1	IE0*	External Interrupt 0 ($\overline{INT0}$) Flag. Set by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT0}$, depending on bit IT0 state. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware.
0	IT0*	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge-sensitive detection (i.e., 1-to-0 transition). Cleared by software to specify level-sensitive detection (i.e., zero level).

*These bits are not used in the control of timer/counter 0 and 1, but are used instead in the control and monitoring of the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Timer/Counter 0 and 1 Data Registers
Both timer 0 and timer 1 consist of two 8-bit registers. These can be used as independent registers or combined to be a single 16-bit register, depending on the timer mode configuration.

TH0 and TL0
Timer 0 high byte and low byte. SFR Address = 8CH, 8AH, respectively.

TH1 and TL1
Timer 1 high byte and low byte. SFR Address = 8DH, 8BH, respectively.

UART SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the first byte will be lost. The physical interface to the serial data network is via Pins RxD(P3.0) and TxD(P3.1), while the SFR interface to the UART comprises the following registers:

SBUF

The serial port receive and transmit registers are both accessed through the SBUF SFR (SFR address = 99H). Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

SCON	UART Serial Port Control Registers
SFR Address	98H
Power-On Default Value	00H
Bit Addressable	Yes

Table XXX. SCON SFR Bit Designations

Bit	Name	Description
7	SM0	UART Serial Mode Select Bits.
6	SM1	These bits select the Serial Port operating mode as follows: SM0 SM1 Selected Operating Mode 0 0 Mode 0: Shift Register, fixed baud rate (f_{CORE}/12) 0 1 Mode 1: 8-bit UART, variable baud rate 1 0 Mode 2: 9-bit UART, fixed baud rate (f_{CORE}/64) or (f_{CORE}/32) 1 1 Mode 3: 9-bit UART, variable baud rate
5	SM2	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI will not be activated if a valid stop bit was not received. If SM2 is cleared, RI will be set as soon as the byte of data has been received. In Modes 2 or 3, if SM2 is set, RI will not be activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI will be set as soon as the byte of data has been received.
4	REN	Serial Port Receive Enable Bit. Set by user software to enable serial port reception. Cleared by user software to disable serial port reception.
3	TB8	Serial Port Transmit (Bit 9). The data loaded into TB8 will be the ninth data bit that will be transmitted in Modes 2 and 3.
2	RB8	Serial Port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	TI	Serial Port Transmit Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. TI must be cleared by user software.
0	RI	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. RI must be cleared by software.

UART OPERATING MODES

Mode 0: 8-Bit Shift Register Mode

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The 8 bits are transmitted with the least-significant bit (LSB) first, as shown in Figure 54.

Reception is initiated when the Receive Enable bit (REN) is 1 and the Receive Interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line and the clock pulses are output from the TxD line.

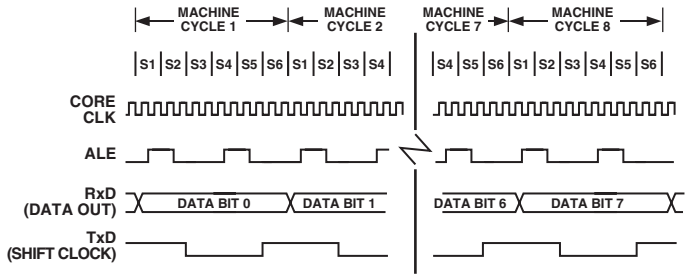


Figure 54. UART Serial Port Transmission, Mode 0

INTERRUPT SYSTEM

The ADuC834 provides a total of 11 interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs. These are the IE (Interrupt Enable) Register, the IP (Interrupt Priority Register) and the IEIP2 (Secondary Interrupt Enable/Priority SFR) Registers. Their bit definitions are given in the Tables XXXV– XXXVII.

IE	**Interrupt Enable Register**
SFR Address	A8H
Power-On Default Value	00H
Bit Addressable	Yes

Table XXXV. IE SFR Bit Designations

Bit	Name	Description
7	EA	Written by User to Enable '1' or Disable '0' All Interrupt Sources
6	EADC	Written by User to Enable '1' or Disable '0' ADC Interrupt
5	ET2	Written by User to Enable '1' or Disable '0' Timer 2 Interrupt
4	ES	Written by User to Enable '1' or Disable '0' UART Serial Port Interrupt
3	ET1	Written by User to Enable '1' or Disable '0' Timer 1 Interrupt
2	EX1	Written by User to Enable '1' or Disable '0' External Interrupt 1
1	ET0	Written by User to Enable '1' or Disable '0' Timer 0 Interrupt
0	EX0	Written by User to Enable '1' or Disable '0' External Interrupt 0

IP	**Interrupt Priority Register**
SFR Address	B8H
Power-On Default Value	00H
Bit Addressable	Yes

Table XXXVI. IP SFR Bit Designations

Bit	Name	Description
7	—	Reserved for Future Use
6	PADC	Written by User to Select ADC Interrupt Priority ('1' = High; '0' = Low)
5	PT2	Written by User to Select Timer 2 Interrupt Priority ('1' = High; '0' = Low)
4	PS	Written by User to Select UART Serial Port Interrupt Priority ('1' = High; '0' = Low)
3	PT1	Written by User to Select Timer 1 Interrupt Priority ('1' = High; '0' = Low)
2	PX1	Written by User to Select External Interrupt 1 Priority ('1' = High; '0' = Low)
1	PT0	Written by User to Select Timer 0 Interrupt Priority ('1' = High; '0' = Low)
0	PX0	Written by User to Select External Interrupt 0 Priority ('1' = High; '0' = Low)

IEIP2	**Secondary Interrupt Enable and Priority Register**
SFR Address	A9H
Power-On Default Value	A0H
Bit Addressable	No

Table XXXVII. IEIP2 SFR Bit Designations

Bit	Name	Description
7	—	Reserved for Future Use
6	PTI	Written by User to Select TIC Interrupt Priority ('1' = High; '0' = Low)
5	PPSM	Written by User to Select Power Supply Monitor Interrupt Priority ('1' = High; '0' = Low)
4	PSI	Written by User to Select SPI/I^2C Serial Port Interrupt Priority ('1' = High; '0' = Low)
3	—	Reserved. This Bit Must Be '0.'
2	ETI	Written by User to Enable '1' or Disable '0' TIC Interrupt
1	EPSM	Written by User to Enable '1' or Disable '0' Power Supply Monitor Interrupt
0	ESI	Written by User to Enable '1' or Disable '0' SPI/I^2C Serial Port Interrupt

Parameter		12.58 MHz Core_Clk Min	12.58 MHz Core_Clk Max	Variable Core_Clk Min	Variable Core_Clk Max	Unit	Figure
EXTERNAL PROGRAM MEMORY							
t_{LHLL}	ALE Pulsewidth	119		$2t_{CORE} - 40$		ns	71
t_{AVLL}	Address Valid to ALE Low	39		$t_{CORE} - 40$		ns	71
t_{LLAX}	Address Hold after ALE Low	49		$t_{CORE} - 30$		ns	71
t_{LLIV}	ALE Low to Valid Instruction In		218		$4t_{CORE} - 100$	ns	71
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	49		$t_{CORE} - 30$		ns	71
t_{PLPH}	$\overline{PSEN}$ Pulsewidth	193		$3t_{CORE} - 45$		ns	71
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		133		$3t_{CORE} - 105$	ns	71
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		0		ns	71
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		54		$t_{CORE} - 25$	ns	71
t_{AVIV}	Address to Valid Instruction In		292		$5t_{CORE} - 105$	ns	71
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		25		25	ns	71
t_{PHAX}	Address Hold after $\overline{PSEN}$ High	0		0		ns	71

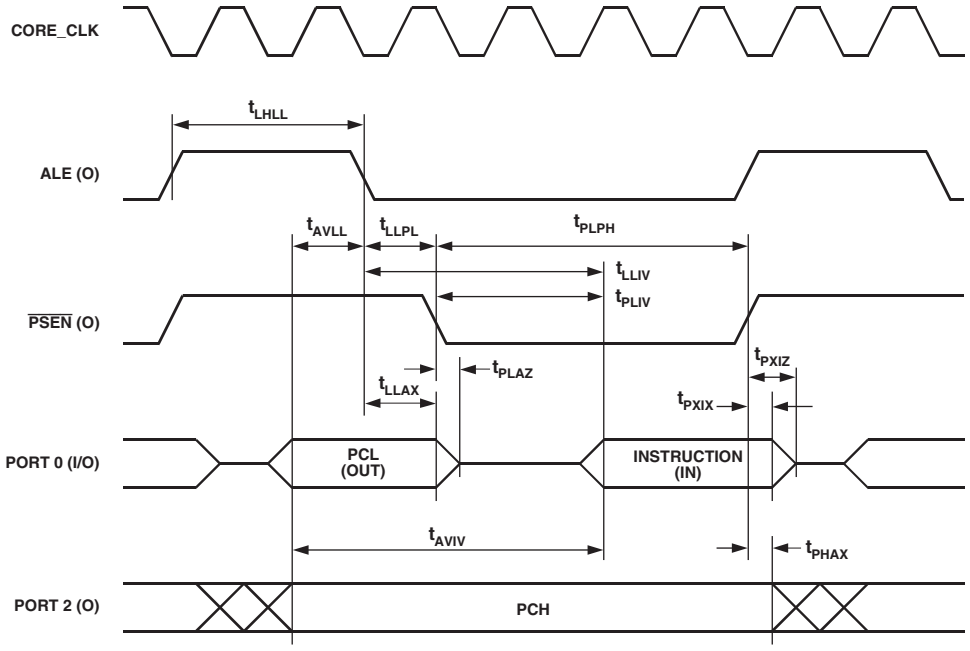


Figure 71. External Program Memory Read Cycle

Parameter		12.58 MHz Core_Clk Min	Max	Variable Core_Clk Min	Max	Unit	Figure
EXTERNAL DATA MEMORY READ CYCLE							
t_{RLRH}	$\overline{RD}$ Pulsewidth	377		$6t_{CORE} - 100$		ns	72
t_{AVLL}	Address Valid after ALE Low	39		$t_{CORE} - 40$		ns	72
t_{LLAX}	Address Hold after ALE Low	44		$t_{CORE} - 35$		ns	72
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		232		$5t_{CORE} - 165$	ns	72
t_{RHDX}	Data and Address Hold after $\overline{RD}$	0		0		ns	72
t_{RHDZ}	Data Float after $\overline{RD}$		89		$2t_{CORE} - 70$	ns	72
t_{LLDV}	ALE Low to Valid Data In		486		$8t_{CORE} - 150$	ns	72
t_{AVDV}	Address to Valid Data In		550		$9t_{CORE} - 165$	ns	72
t_{LLWL}	ALE Low to $\overline{RD}$ Low	188	288	$3t_{CORE} - 50$	$3t_{CORE} + 50$	ns	72
t_{AVWL}	Address Valid to $\overline{RD}$ Low	188		$4t_{CORE} - 130$		ns	72
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns	72
t_{WHLH}	$\overline{RD}$ High to ALE High	39	119	$t_{CORE} - 40$	$t_{CORE} + 40$	ns	72

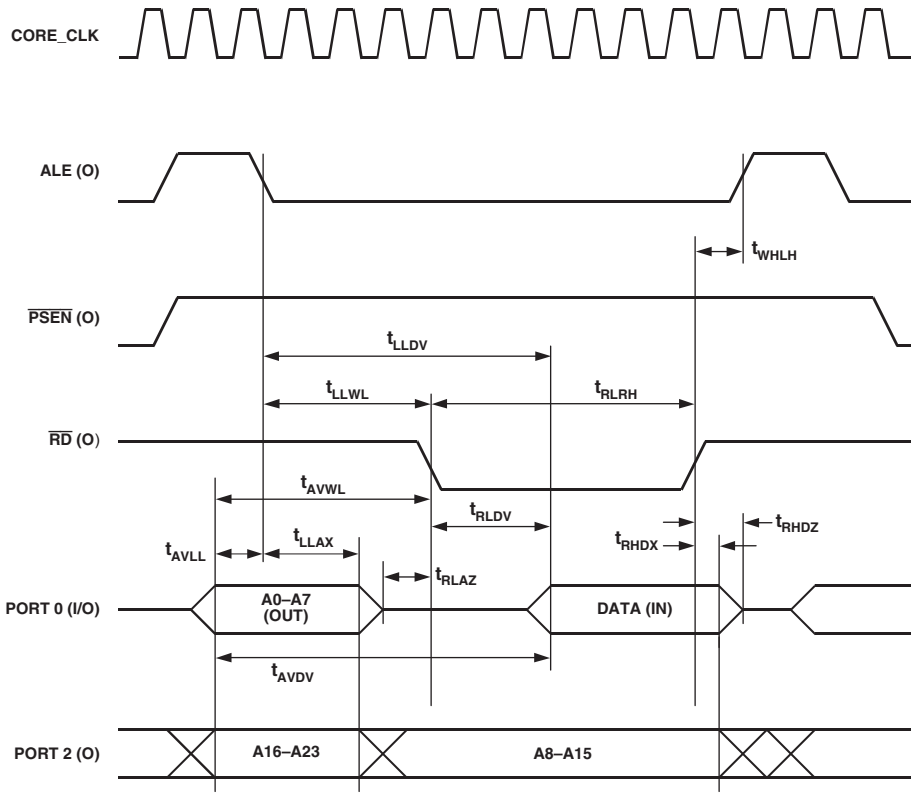


Figure 72. External Data Memory Read Cycle

Parameter		12.58 MHz Core_Clk Min	Typ	Max	Variable Core_Clk Min	Typ	Max	Unit	Figure
UART TIMING (Shift Register Mode)									
t_{XLXL}	Serial Port Clock Cycle Time		0.95			$12t_{CORE}$		μs	74
t_{QVXH}	Output Data Setup to Clock	662			$10t_{CORE} - 133$			ns	74
t_{DVXH}	Input Data Setup to Clock	292			$2t_{CORE} + 133$			ns	74
t_{XHDX}	Input Data Hold after Clock	0			0			ns	74
t_{XHQX}	Output Data Hold after Clock	42			$2t_{CORE} - 117$			ns	74

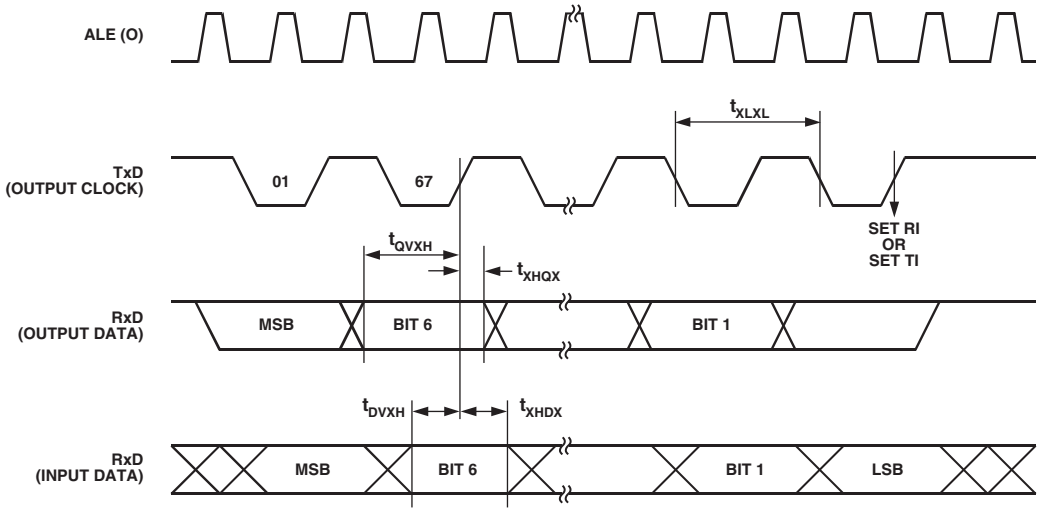


Figure 74. UART Timing in Shift Register Mode

REVISION HISTORY

4/16—Rev. A to Rev. B

Changes to 56-Lead LFCSP Pin Configuration Figure 9
Changes to Pin Function Descriptions Table 12
Updated Outline Dimensions 80
Moved Ordering Guide 80
Changes to Ordering Guide 80

4/03—Rev. 0 to Rev. A

Updated Outline Dimensions 80

2/03—Revision 0: Initial Version

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