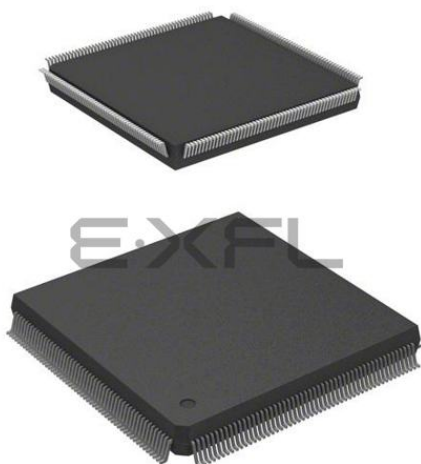




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	147
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a3pe600-2pqg208i

Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II)

ProASIC3E banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the [FlashPro User's Guide](#) for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify ([Figure 1-3 on page 1-7](#)).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 – I/O is set to drive out logic High
 - 0 – I/O is set to drive out logic Low
 - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
 - Z -Tri-State: I/O is tristated

Specify I/O States During Programming

Load from file... Save to file... ☐ Show BSR Details

	Port Name	Macro Cell	Pin Number	I/O State (Output Only)
	BIST	ADLIB:INBUF	T2	1
	BYPASS_IO	ADLIB:INBUF	K1	1
	CLK	ADLIB:INBUF	B1	1
	ENDOUT	ADLIB:INBUF	J16	1
	LED	ADLIB:OUTBUF	M3	0
	MONITOR[0]	ADLIB:OUTBUF	B5	0
	MONITOR[1]	ADLIB:OUTBUF	C7	Z
	MONITOR[2]	ADLIB:OUTBUF	D9	Z
	MONITOR[3]	ADLIB:OUTBUF	D7	Z
	MONITOR[4]	ADLIB:OUTBUF	A11	Z
	OEa	ADLIB:INBUF	E4	Z
	OEb	ADLIB:INBUF	F1	Z
	OSC_EN	ADLIB:INBUF	K3	Z
	PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
	PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
	PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
	PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
	PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

Help OK Cancel

Figure 1-3 • I/O States During Programming Window

- Click OK to return to the FlashPoint – Programming File Generator window.
I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-33 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	−0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	−0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	−0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

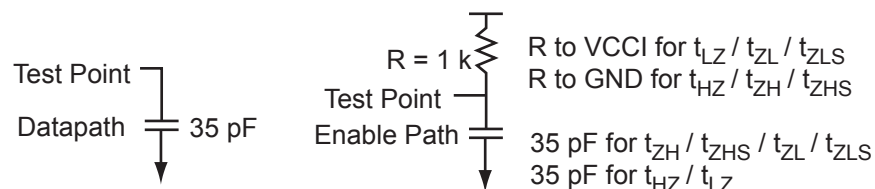


Figure 2-8 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	2.5	1.2	—	35

Note: *Measuring point = Vtrip. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-66 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
15 mA	-0.3	VREF - 0.2	VREF + 0.2	3.6	0.54	VCCI - 0.62	15	15	87	83	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

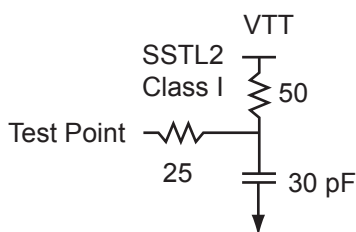


Figure 2-18 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-68 • SSTL 2 Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
-1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
-2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Timing Characteristics

Table 2-80 • LVDS

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.87	0.04	1.82	ns
-1	0.56	1.59	0.04	1.55	ns
-2	0.49	1.40	0.03	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-23](#). The input and output buffer delays are available in the LVDS section in [Table 2-80](#).

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

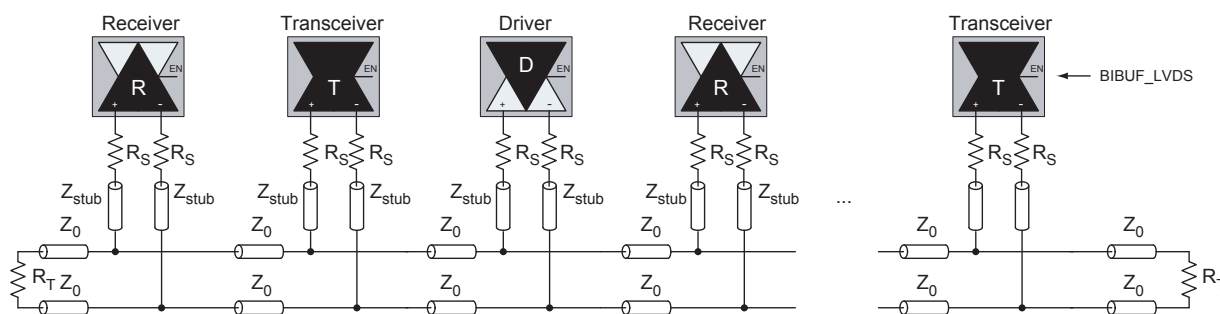


Figure 2-23 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

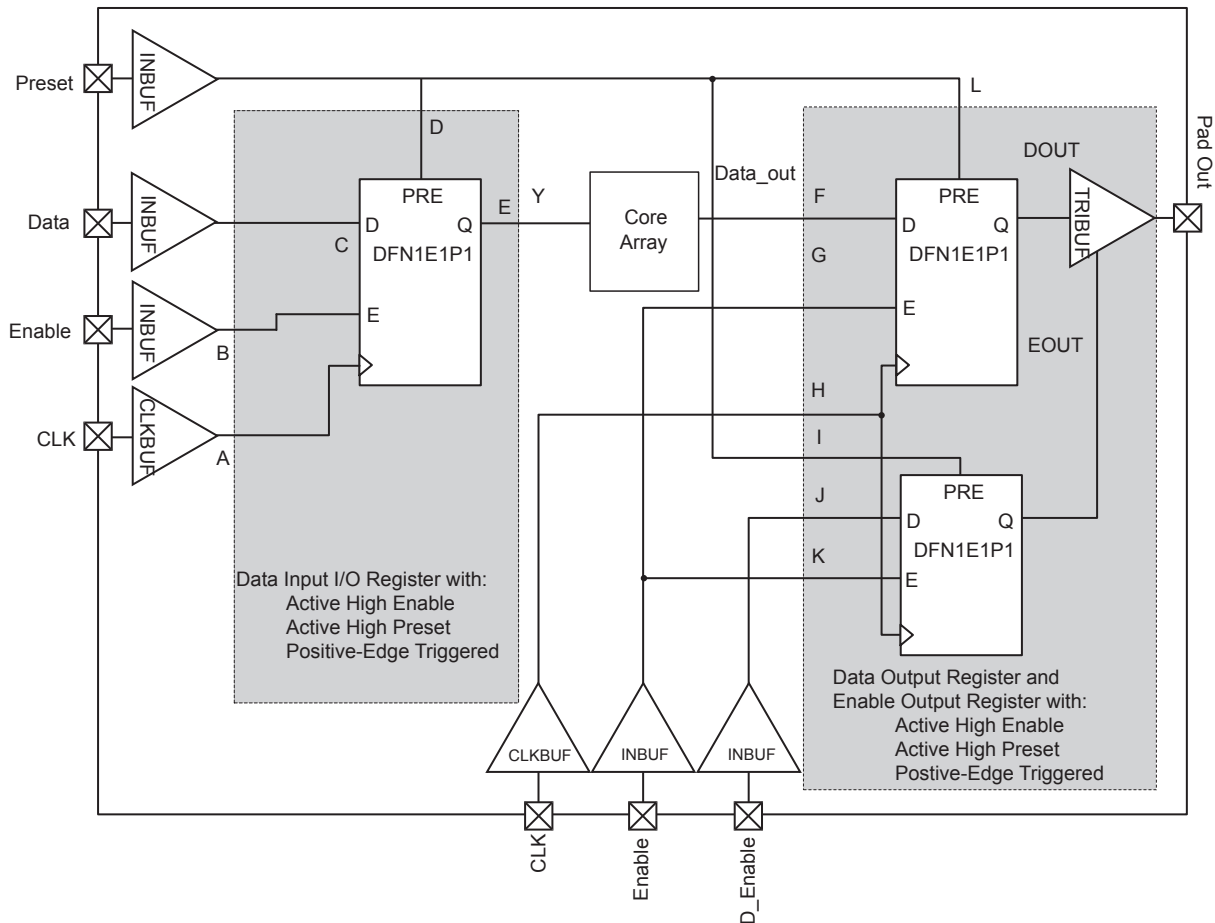


Figure 2-25 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Output DDR Module

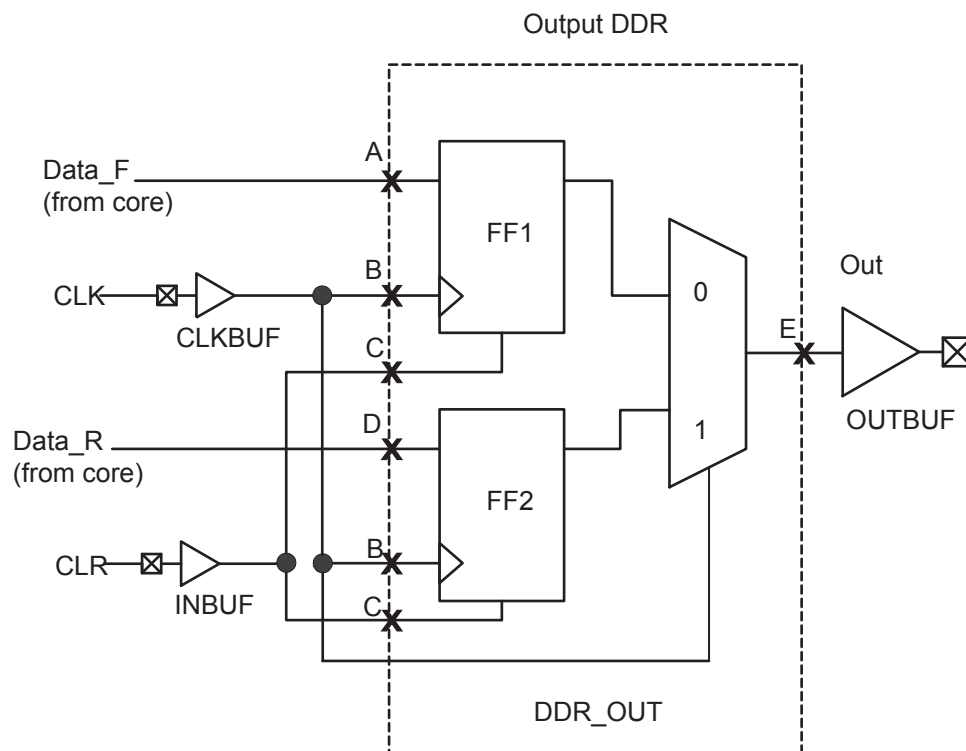


Figure 2-32 • Output DDR Timing Model

Table 2-91 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [Fusion](#), [IGLOO®/e](#), and [ProASIC3/E Macro Library Guide](#).

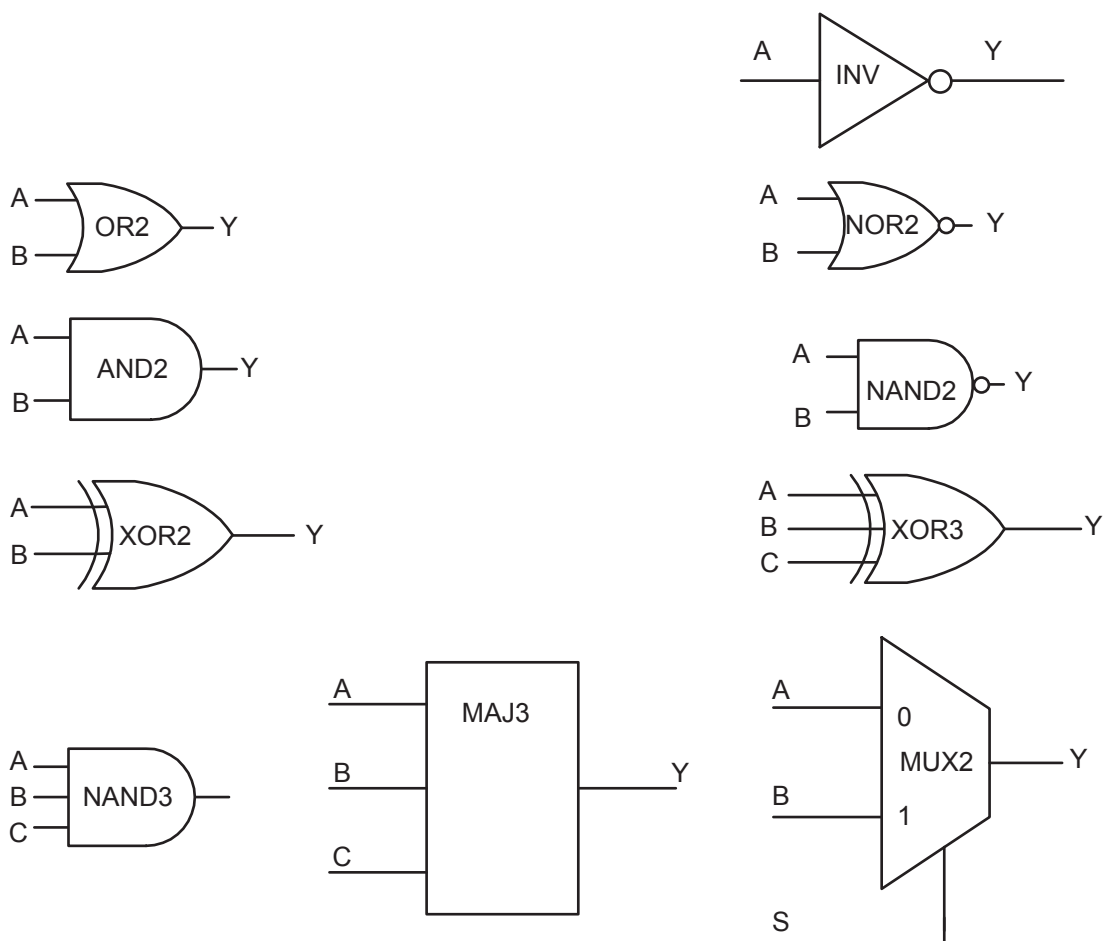


Figure 2-34 • Sample of Combinatorial Cells

FIFO

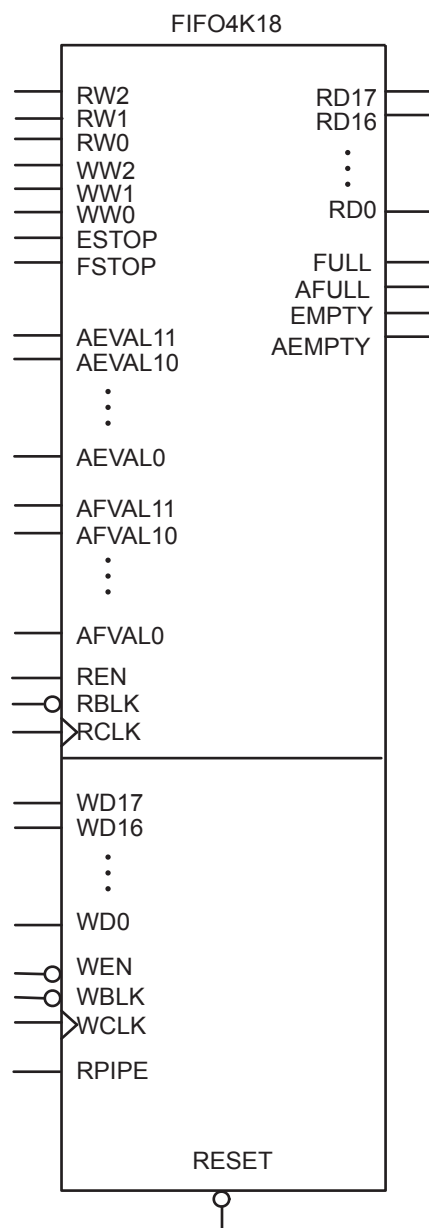


Figure 2-46 • FIFO Model

PQ208	
Pin Number	A3PE1500 Function
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO220PSB7V3
5	GAA2/IO221PDB7V3
6	IO221NDB7V3
7	GAC2/IO219PDB7V3
8	IO219NDB7V3
9	IO215PDB7V3
10	IO215NDB7V3
11	IO212PDB7V2
12	IO212NDB7V2
13	IO208PDB7V2
14	IO208NDB7V2
15	IO204PSB7V1
16	VCC
17	GND
18	VCCIB7
19	IO200PDB7V1
20	IO200NDB7V1
21	IO196PSB7V0
22	GFC1/IO192PSB7V0
23	GFB1/IO191PDB7V0
24	GFB0/IO191NDB7V0
25	VCOMPLF
26	GFA0/IO190NPB6V2
27	VCCPLF
28	GFA1/IO190PPB6V2
29	GND
30	GFA2/IO189PDB6V2
31	IO189NDB6V2
32	GFB2/IO188PPB6V2
33	GFC2/IO187PPB6V2
34	IO188NPB6V2
35	IO187NPB6V2
36	VCC

PQ208	
Pin Number	A3PE1500 Function
37	IO184PDB6V2
38	IO184NDB6V2
39	IO180PSB6V1
40	VCCIB6
41	GND
42	IO176PDB6V1
43	IO176NDB6V1
44	GEC1/IO169PDB6V0
45	GEC0/IO169NDB6V0
46	GEB1/IO168PPB6V0
47	GEA1/IO167PPB6V0
48	GEB0/IO168NPB6V0
49	GEA0/IO167NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO166NDB5V3
56	GEA2/IO166PDB5V3
57	IO165NDB5V3
58	GEB2/IO165PDB5V3
59	IO164NDB5V3
60	GEC2/IO164PDB5V3
61	IO163PSB5V3
62	VCCIB5
63	IO161PSB5V3
64	IO157NDB5V2
65	GND
66	IO157PDB5V2
67	IO153NDB5V2
68	IO153PDB5V2
69	IO149NDB5V1
70	IO149PDB5V1
71	VCC
72	VCCIB5

PQ208	
Pin Number	A3PE1500 Function
73	IO145NDB5V1
74	IO145PDB5V1
75	IO143NDB5V1
76	IO143PDB5V1
77	IO137NDB5V0
78	IO137PDB5V0
79	IO135NDB5V0
80	IO135PDB5V0
81	GND
82	IO131NDB4V2
83	IO131PDB4V2
84	IO129NDB4V2
85	IO129PDB4V2
86	IO127NDB4V2
87	IO127PDB4V2
88	VCC
89	VCCIB4
90	IO121NDB4V1
91	IO121PDB4V1
92	IO119NDB4V1
93	IO119PDB4V1
94	IO113NDB4V0
95	GDC2/IO113PDB4V0
96	IO112NDB4V0
97	GND
98	GDB2/IO112PDB4V0
99	GDA2/IO111PSB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	VPUMP
107	GNDQ
108	TDO

PQ208	
Pin Number	A3PE3000 Function
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO308PSB7V4
5	GAA2/IO309PDB7V4
6	IO309NDB7V4
7	GAC2/IO307PDB7V4
8	IO307NDB7V4
9	IO303PDB7V3
10	IO303NDB7V3
11	IO299PDB7V3
12	IO299NDB7V3
13	IO295PDB7V2
14	IO295NDB7V2
15	IO291PSB7V2
16	VCC
17	GND
18	VCCIB7
19	IO285PDB7V1
20	IO285NDB7V1
21	IO279PSB7V0
22	GFC1/IO275PSB7V0
23	GFB1/IO274PDB7V0
24	GFB0/IO274NDB7V0
25	VCOMPLF
26	GFA0/IO273NPB6V4
27	VCCPLF
28	GFA1/IO273PPB6V4
29	GND
30	GFA2/IO272PDB6V4
31	IO272NDB6V4
32	GFB2/IO271PPB6V4
33	GFC2/IO270PPB6V4
34	IO271NPB6V4
35	IO270NPB6V4
36	VCC
37	IO252PDB6V2
38	IO252NDB6V2
39	IO248PSB6V1

PQ208	
Pin Number	A3PE3000 Function
40	VCCIB6
41	GND
42	IO244PDB6V1
43	IO244NDB6V1
44	GEC1/IO236PDB6V0
45	GEC0/IO236NDB6V0
46	GEB1/IO235PPB6V0
47	GEA1/IO234PPB6V0
48	GEB0/IO235NPB6V0
49	GEA0/IO234NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO233NDB5V4
56	GEA2/IO233PDB5V4
57	IO232NDB5V4
58	GEB2/IO232PDB5V4
59	IO231NDB5V4
60	GEC2/IO231PDB5V4
61	IO230PSB5V4
62	VCCIB5
63	IO218NDB5V3
64	IO218PDB5V3
65	GND
66	IO214PSB5V2
67	IO212NDB5V2
68	IO212PDB5V2
69	IO208NDB5V1
70	IO208PDB5V1
71	VCC
72	VCCIB5
73	IO202NDB5V1
74	IO202PDB5V1
75	IO198NDB5V0
76	IO198PDB5V0
77	IO197NDB5V0
78	IO197PDB5V0

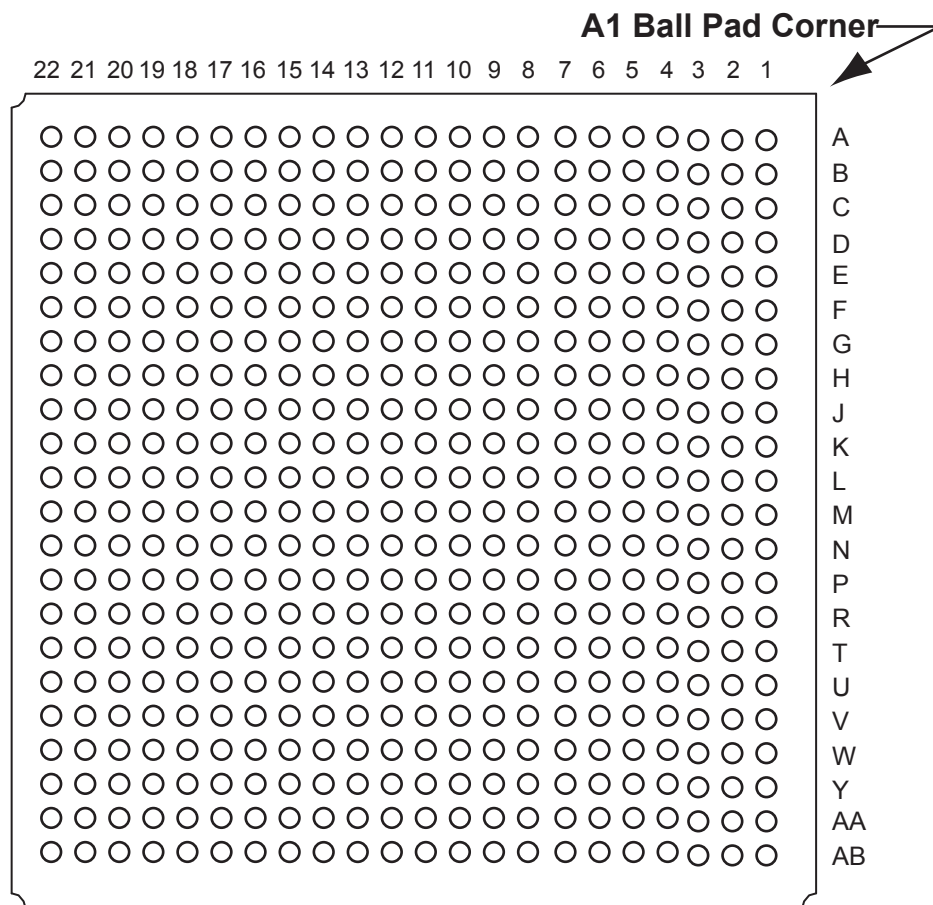
PQ208	
Pin Number	A3PE3000 Function
79	IO194NDB5V0
80	IO194PDB5V0
81	GND
82	IO184NDB4V3
83	IO184PDB4V3
84	IO180NDB4V3
85	IO180PDB4V3
86	IO176NDB4V2
87	IO176PDB4V2
88	VCC
89	VCCIB4
90	IO170NDB4V2
91	IO170PDB4V2
92	IO166NDB4V1
93	IO166PDB4V1
94	IO156NDB4V0
95	GDC2/IO156PDB4V0
96	IO154NPB4V0
97	GND
98	GDB2/IO155PSB4V0
99	GDA2/IO154PPB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	VPUMP
107	GNDQ
108	TDO
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO153NPB3V4
113	GDB0/IO152NPB3V4
114	GDA1/IO153PPB3V4
115	GDB1/IO152PPB3V4
116	GDC0/IO151NDB3V4
117	GDC1/IO151PDB3V4

PQ208	
Pin Number	A3PE3000 Function
118	IO134NDB3V2
119	IO134PDB3V2
120	IO132NDB3V2
121	IO132PDB3V2
122	GND
123	VCCIB3
124	GCC2/IO117PSB3V0
125	GCB2/IO116PSB3V0
126	NC
127	IO115NDB3V0
128	GCA2/IO115PDB3V0
129	GCA1/IO114PPB3V0
130	GND
131	VCCPLC
132	GCA0/IO114NPB3V0
133	VCOMPLC
134	GCB0/IO113NDB2V3
135	GCB1/IO113PDB2V3
136	GCC1/IO112PSB2V3
137	IO110NDB2V3
138	IO110PDB2V3
139	IO106PSB2V3
140	VCCIB2
141	GND
142	VCC
143	IO99NDB2V2
144	IO99PDB2V2
145	IO96NDB2V1
146	IO96PDB2V1
147	IO91NDB2V1
148	IO91PDB2V1
149	IO88NDB2V0
150	IO88PDB2V0
151	GBC2/IO84PSB2V0
152	GBA2/IO82PSB2V0
153	GBB2/IO83PSB2V0
154	VMV2
155	GNDQ
156	GND

PQ208	
Pin Number	A3PE3000 Function
157	VMV1
158	GNDQ
159	GBA1/IO81PDB1V4
160	GBA0/IO81NDB1V4
161	GBB1/IO80PDB1V4
162	GND
163	GBB0/IO80NDB1V4
164	GBC1/IO79PDB1V4
165	GBC0/IO79NDB1V4
166	IO74PDB1V4
167	IO74NDB1V4
168	IO70PDB1V3
169	IO70NDB1V3
170	VCCIB1
171	VCC
172	IO56PSB1V1
173	IO55PDB1V1
174	IO55NDB1V1
175	IO54PDB1V1
176	IO54NDB1V1
177	IO40PDB0V4
178	GND
179	IO40NDB0V4
180	IO37PDB0V4
181	IO37NDB0V4
182	IO35PDB0V4
183	IO35NDB0V4
184	IO32PDB0V3
185	IO32NDB0V3
186	VCCIB0
187	VCC
188	IO28PDB0V3
189	IO28NDB0V3
190	IO24PDB0V2
191	IO24NDB0V2
192	IO21PSB0V2
193	IO16PDB0V1
194	IO16NDB0V1
195	GND

PQ208	
Pin Number	A3PE3000 Function
196	IO11PDB0V1
197	IO11NDB0V1
198	IO08PDB0V0
199	IO08NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG484	
Pin Number	A3PE1500 Function
H19	IO67PDB2V1
H20	VCC
H21	VMV2
H22	IO74PSB2V2
J1	IO212NDB7V2
J2	IO212PDB7V2
J3	VMV7
J4	IO206PDB7V1
J5	IO204PDB7V1
J6	IO210PDB7V2
J7	IO215NDB7V3
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO60NDB2V0
J17	IO65NDB2V1
J18	IO65PDB2V1
J19	IO75PPB2V2
J20	GNDQ
J21	IO77PDB2V2
J22	IO79PDB2V3
K1	IO200NDB7V1
K2	IO200PDB7V1
K3	GNDQ
K4	IO206NDB7V1
K5	IO204NDB7V1
K6	IO210NDB7V2
K7	GFC1/IO192PPB7V0
K8	VCCIB7
K9	VCC
K10	GND

FG484	
Pin Number	A3PE1500 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO85PPB2V3
K17	IO73NDB2V2
K18	IO73PDB2V2
K19	IO81NPB2V3
K20	IO75NPB2V2
K21	IO77NDB2V2
K22	IO79NDB2V3
L1	NC
L2	IO196PDB7V0
L3	IO196NDB7V0
L4	GFB0/IO191NPB7V0
L5	GFA0/IO190NDB6V2
L6	GFB1/IO191PPB7V0
L7	VCOMPLF
L8	GFC0/IO192NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO85NPB2V3
L16	GCB1/IO86PPB2V3
L17	GCA0/IO87NPB3V0
L18	VCOMPLC
L19	GCB0/IO86NPB2V3
L20	IO81PPB2V3
L21	IO83NDB2V3
L22	IO83PDB2V3
M1	GNDQ
M2	IO185NPB6V2

FG484	
Pin Number	A3PE1500 Function
M3	IO189NDB6V2
M4	GFA2/IO189PDB6V2
M5	GFA1/IO190PDB6V2
M6	VCCPLF
M7	IO188NDB6V2
M8	GFB2/IO188PDB6V2
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO89PPB3V0
M16	GCA1/IO87PPB3V0
M17	GCC2/IO90PPB3V0
M18	VCCPLC
M19	GCA2/IO88PDB3V0
M20	IO88NDB3V0
M21	IO93PDB3V0
M22	NC
N1	IO185PPB6V2
N2	IO183NDB6V2
N3	VMV6
N4	GFC2/IO187PPB6V2
N5	IO184PPB6V2
N6	IO186PDB6V2
N7	IO186NDB6V2
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO89NPB3V0

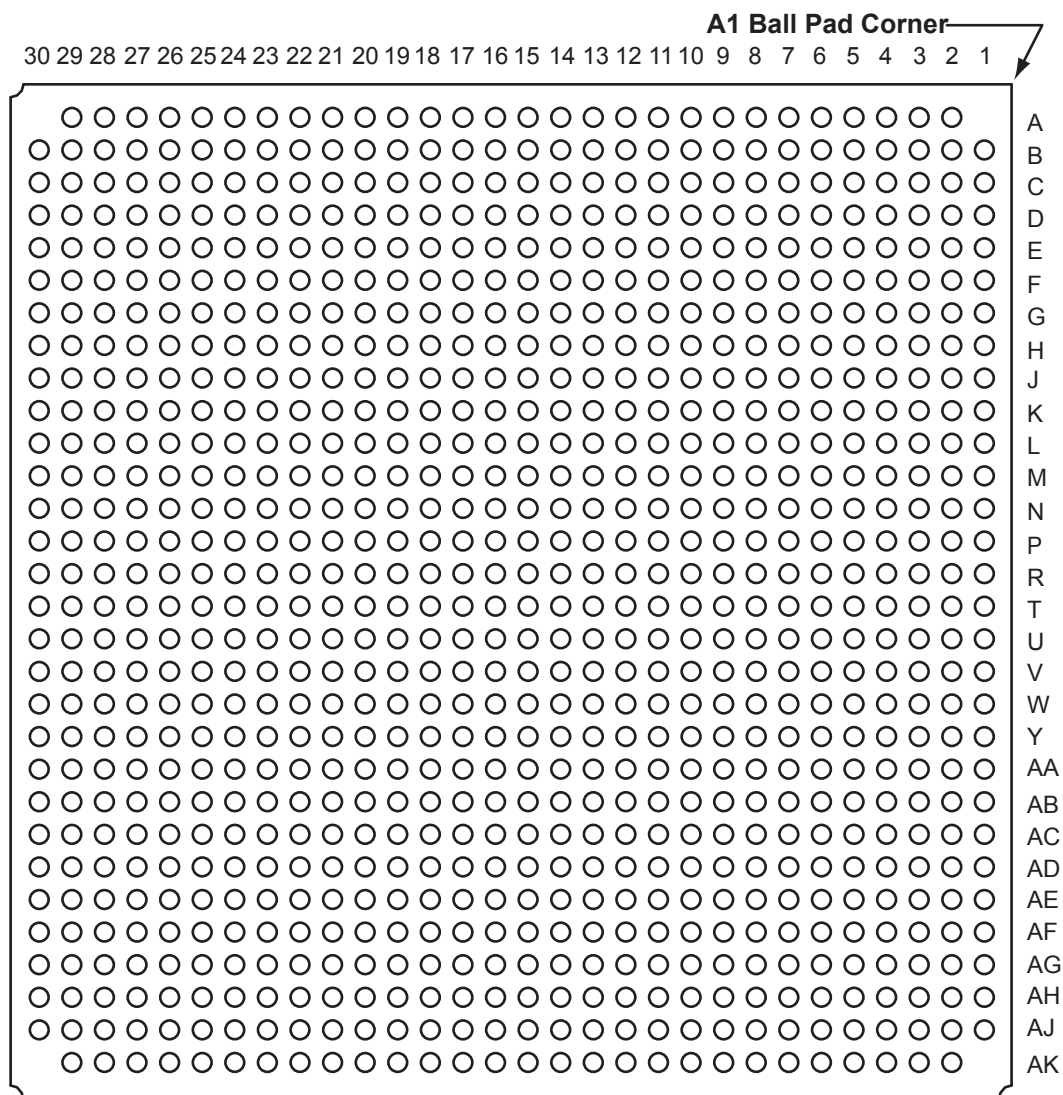
FG484		FG484		FG484	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
C21	IO94PPB2V1	E13	IO58NDB1V2	G5	IO297PDB7V2
C22	VCCIB2	E14	IO58PDB1V2	G6	GAC2/IO307PDB7V4
D1	IO293PDB7V2	E15	GBC1/IO79PDB1V4	G7	VCOMPLA
D2	IO303NDB7V3	E16	GBB0/IO80NDB1V4	G8	GNDQ
D3	IO305NDB7V3	E17	GNDQ	G9	IO26NDB0V3
D4	GND	E18	GBA2/IO82PDB2V0	G10	IO26PDB0V3
D5	GAA0/IO00NDB0V0	E19	IO86NDB2V0	G11	IO36PDB0V4
D6	GAA1/IO00PDB0V0	E20	GND	G12	IO42PDB1V0
D7	GAB0/IO01NDB0V0	E21	IO90NDB2V1	G13	IO50PDB1V1
D8	IO20PDB0V2	E22	IO98PDB2V2	G14	IO60NDB1V2
D9	IO22PDB0V2	F1	IO299NPB7V3	G15	GNDQ
D10	IO30PDB0V3	F2	IO301NDB7V3	G16	VCOMPLB
D11	IO38NDB0V4	F3	IO301PDB7V3	G17	GBB2/IO83PDB2V0
D12	IO52NDB1V1	F4	IO308NDB7V4	G18	IO92PDB2V1
D13	IO52PDB1V1	F5	IO309NDB7V4	G19	IO92NDB2V1
D14	IO66NDB1V3	F6	VMV7	G20	IO102PDB2V2
D15	IO66PDB1V3	F7	VCCPLA	G21	IO102NDB2V2
D16	GBB1/IO80PDB1V4	F8	GAC0/IO02NDB0V0	G22	IO105NDB2V2
D17	GBA0/IO81NDB1V4	F9	GAC1/IO02PDB0V0	H1	IO286PSB7V1
D18	GBA1/IO81PDB1V4	F10	IO32NDB0V3	H2	IO291NPB7V2
D19	GND	F11	IO32PDB0V3	H3	VCC
D20	IO88PDB2V0	F12	IO44PDB1V0	H4	IO295NDB7V2
D21	IO90PDB2V1	F13	IO50NDB1V1	H5	IO297NDB7V2
D22	IO94NPB2V1	F14	IO60PDB1V2	H6	IO307NDB7V4
E1	IO293NDB7V2	F15	GBC0/IO79NDB1V4	H7	IO287PDB7V1
E2	IO299PPB7V3	F16	VCCPLB	H8	VMV0
E3	GND	F17	VMV2	H9	VCCIB0
E4	GAB2/IO308PDB7V4	F18	IO82NDB2V0	H10	VCCIB0
E5	GAA2/IO309PDB7V4	F19	IO86PDB2V0	H11	IO36NDB0V4
E6	GNDQ	F20	IO96PDB2V1	H12	IO42NDB1V0
E7	GAB1/IO01PDB0V0	F21	IO96NDB2V1	H13	VCCIB1
E8	IO20NDB0V2	F22	IO98NDB2V2	H14	VCCIB1
E9	IO22NDB0V2	G1	IO289NDB7V1	H15	VMV1
E10	IO30NDB0V3	G2	IO289PDB7V1	H16	GBC2/IO84PDB2V0
E11	IO38PDB0V4	G3	IO291PPB7V2	H17	IO83NDB2V0
E12	IO44NDB1V0	G4	IO295PDB7V2	H18	IO100NDB2V2

FG676	
Pin Number	A3PE1500 Function
C9	IO10PDB0V1
C10	IO16PDB0V2
C11	IO20PDB0V2
C12	IO24PDB0V3
C13	IO23PDB0V2
C14	IO28PDB0V3
C15	IO31PDB0V3
C16	IO32NDB1V0
C17	IO36NDB1V0
C18	IO37NDB1V0
C19	IO45NDB1V1
C20	IO42PPB1V1
C21	IO46NPB1V1
C22	IO48NPB1V2
C23	GBB0/IO56NPB1V3
C24	VMV1
C25	GBC2/IO60PDB2V0
C26	IO60NDB2V0
D1	IO218NDB7V3
D2	IO218PDB7V3
D3	GND
D4	VMV7
D5	IO221NDB7V3
D6	GAC0/IO02NDB0V0
D7	GAC1/IO02PDB0V0
D8	IO05NDB0V0
D9	IO08PDB0V1
D10	IO12NDB0V1
D11	IO18NDB0V2
D12	IO17NDB0V2
D13	IO25NDB0V3
D14	IO29NDB0V3
D15	IO33NDB1V0
D16	IO40PDB1V1
D17	IO43NDB1V1
D18	IO47PDB1V1

FG676	
Pin Number	A3PE1500 Function
D19	IO45PDB1V1
D20	IO46PPB1V1
D21	IO48PPB1V2
D22	GBA0/IO57NPB1V3
D23	GNDQ
D24	GBB1/IO56PPB1V3
D25	GBB2/IO59PDB2V0
D26	IO59NDB2V0
E1	IO212PDB7V2
E2	IO211NDB7V2
E3	IO211PDB7V2
E4	IO220NPB7V3
E5	GNDQ
E6	GAB2/IO220PPB7V3
E7	GAB1/IO01PDB0V0
E8	IO05PDB0V0
E9	IO08NDB0V1
E10	IO12PDB0V1
E11	IO18PDB0V2
E12	IO17PDB0V2
E13	IO25PDB0V3
E14	IO29PDB0V3
E15	IO33PDB1V0
E16	IO40NDB1V1
E17	IO43PDB1V1
E18	IO47NDB1V1
E19	IO54NDB1V3
E20	IO52NDB1V2
E21	IO52PDB1V2
E22	VCCPLB
E23	GBA1/IO57PPB1V3
E24	IO63PDB2V0
E25	IO63NDB2V0
E26	IO68PDB2V1
F1	IO212NDB7V2
F2	IO203PPB7V1

FG676	
Pin Number	A3PE1500 Function
F3	IO213NDB7V2
F4	IO213PDB7V2
F5	GND
F6	VCCPLA
F7	GAB0/IO01NDB0V0
F8	GNDQ
F9	IO03PDB0V0
F10	IO13PDB0V1
F11	IO15PDB0V1
F12	IO19PDB0V2
F13	IO21PDB0V2
F14	IO27NDB0V3
F15	IO35PDB1V0
F16	IO39NDB1V0
F17	IO51PDB1V2
F18	IO53PDB1V2
F19	IO54PDB1V3
F20	VMV2
F21	VCOMPLB
F22	IO61PDB2V0
F23	IO61NDB2V0
F24	IO66PDB2V1
F25	IO66NDB2V1
F26	IO68NDB2V1
G1	IO203NPB7V1
G2	IO207NDB7V2
G3	IO207PDB7V2
G4	IO216NDB7V3
G5	IO216PDB7V3
G6	VCOMPLA
G7	VMV0
G8	VCC
G9	IO03NDB0V0
G10	IO13NDB0V1
G11	IO15NDB0V1
G12	IO19NDB0V2

FG896



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
AC21	IO164PDB4V1	AD27	GDA0/IO153NDB3V4	AF3	VCCIB6
AC22	IO162PPB4V1	AD28	GDC0/IO151NDB3V4	AF4	IO220NPB5V3
AC23	GND	AD29	GDC1/IO151PDB3V4	AF5	VCC
AC24	VCOMPLD	AD30	GND	AF6	IO228NDB5V4
AC25	IO150NDB3V4	AE1	IO242PPB6V1	AF7	VCCIB5
AC26	IO148NDB3V4	AE2	VCC	AF8	IO230PDB5V4
AC27	GDA1/IO153PDB3V4	AE3	IO239PDB6V0	AF9	IO229NDB5V4
AC28	IO145NDB3V3	AE4	IO239NDB6V0	AF10	IO229PDB5V4
AC29	IO143NDB3V3	AE5	VMV6	AF11	IO214PPB5V2
AC30	IO137NDB3V2	AE6	GND	AF12	IO208NDB5V1
AD1	GND	AE7	GNDQ	AF13	IO208PDB5V1
AD2	IO242NPB6V1	AE8	IO230NDB5V4	AF14	IO200PDB5V0
AD3	IO240NDB6V0	AE9	IO224NPB5V3	AF15	IO196NDB5V0
AD4	GEC0/IO236NDB6V0	AE10	IO214NPB5V2	AF16	IO186NDB4V4
AD5	VCCIB6	AE11	IO212NDB5V2	AF17	IO186PDB4V4
AD6	GNDQ	AE12	IO212PDB5V2	AF18	IO180NDB4V3
AD7	VCC	AE13	IO202NPB5V1	AF19	IO180PDB4V3
AD8	VMV5	AE14	IO200NDB5V0	AF20	IO168NDB4V1
AD9	VCCIB5	AE15	IO196PDB5V0	AF21	IO168PDB4V1
AD10	IO224PPB5V3	AE16	IO190NDB4V4	AF22	IO160NDB4V0
AD11	IO218NPB5V3	AE17	IO184PDB4V3	AF23	IO158NPB4V0
AD12	IO216PPB5V2	AE18	IO184NDB4V3	AF24	VCCIB4
AD13	IO210PPB5V2	AE19	IO172PDB4V2	AF25	IO154NPB4V0
AD14	IO202PPB5V1	AE20	IO172NDB4V2	AF26	VCC
AD15	IO194PDB5V0	AE21	IO166NDB4V1	AF27	TDO
AD16	IO190PDB4V4	AE22	IO160PDB4V0	AF28	VCCIB3
AD17	IO182NPB4V3	AE23	GNDQ	AF29	GNDQ
AD18	IO176NDB4V2	AE24	VMV4	AF30	GND
AD19	IO176PDB4V2	AE25	GND	AG1	IO238NPB6V0
AD20	IO170PPB4V2	AE26	GDB0/IO152NDB3V4	AG2	VCC
AD21	IO166PDB4V1	AE27	GDB1/IO152PDB3V4	AG3	IO232NPB5V4
AD22	VCCIB4	AE28	VMV3	AG4	GND
AD23	TCK	AE29	VCC	AG5	IO220PPB5V3
AD24	VCC	AE30	IO149PDB3V4	AG6	IO228PDB5V4
AD25	TRST	AF1	GND	AG7	IO231NDB5V4
AD26	VCCIB3	AF2	IO238PPB6V0	AG8	GEC2/IO231PDB5V4

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
M23	IO104PPB2V2	N29	IO107PDB2V3	R5	GFB0/IO274NPB7V0
M24	IO102PDB2V2	N30	IO107NDB2V3	R6	IO271NDB6V4
M25	IO102NDB2V2	P1	IO276NDB7V0	R7	GFB2/IO271PDB6V4
M26	IO95PDB2V1	P2	IO278NDB7V0	R8	IO269PDB6V4
M27	IO97NDB2V1	P3	IO280NDB7V0	R9	IO269NDB6V4
M28	IO101NDB2V2	P4	IO284NDB7V1	R10	VCCIB7
M29	IO103NDB2V2	P5	IO279NDB7V0	R11	VCC
M30	IO119PDB3V0	P6	GFC1/IO275PDB7V0	R12	GND
N1	IO276PDB7V0	P7	GFC0/IO275NDB7V0	R13	GND
N2	IO278PDB7V0	P8	IO277PDB7V0	R14	GND
N3	IO280PDB7V0	P9	IO277NDB7V0	R15	GND
N4	IO284PDB7V1	P10	VCCIB7	R16	GND
N5	IO279PDB7V0	P11	VCC	R17	GND
N6	IO285NDB7V1	P12	GND	R18	GND
N7	IO287NDB7V1	P13	GND	R19	GND
N8	IO281NDB7V0	P14	GND	R20	VCC
N9	IO281PDB7V0	P15	GND	R21	VCCIB2
N10	VCCIB7	P16	GND	R22	GCC0/IO112NDB2V3
N11	VCC	P17	GND	R23	GCB2/IO116PDB3V0
N12	GND	P18	GND	R24	IO118PDB3V0
N13	GND	P19	GND	R25	IO111PPB2V3
N14	GND	P20	VCC	R26	IO122PPB3V1
N15	GND	P21	VCCIB2	R27	GCA0/IO114NPB3V0
N16	GND	P22	GCC1/IO112PDB2V3	R28	VCOMPLC
N17	GND	P23	IO110PDB2V3	R29	GCB1/IO113PPB2V3
N18	GND	P24	IO110NDB2V3	R30	IO115NPB3V0
N19	GND	P25	IO109PPB2V3	T1	IO270NDB6V4
N20	VCC	P26	IO111NPB2V3	T2	VCCPLF
N21	VCCIB2	P27	IO105PDB2V2	T3	GFA2/IO272PPB6V4
N22	IO106NDB2V3	P28	IO105NDB2V2	T4	GFA1/IO273PDB6V4
N23	IO106PDB2V3	P29	GCC2/IO117PDB3V0	T5	IO272NPB6V4
N24	IO108PDB2V3	P30	IO117NDB3V0	T6	IO267NDB6V4
N25	IO108NDB2V3	R1	GFC2/IO270PDB6V4	T7	IO267PDB6V4
N26	IO95NDB2V1	R2	GFB1/IO274PPB7V0	T8	IO265PDB6V3
N27	IO99NDB2V2	R3	VCOMPLF	T9	IO263PDB6V3
N28	IO99PDB2V2	R4	GFA0/IO273NDB6V4	T10	VCCIB6

