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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

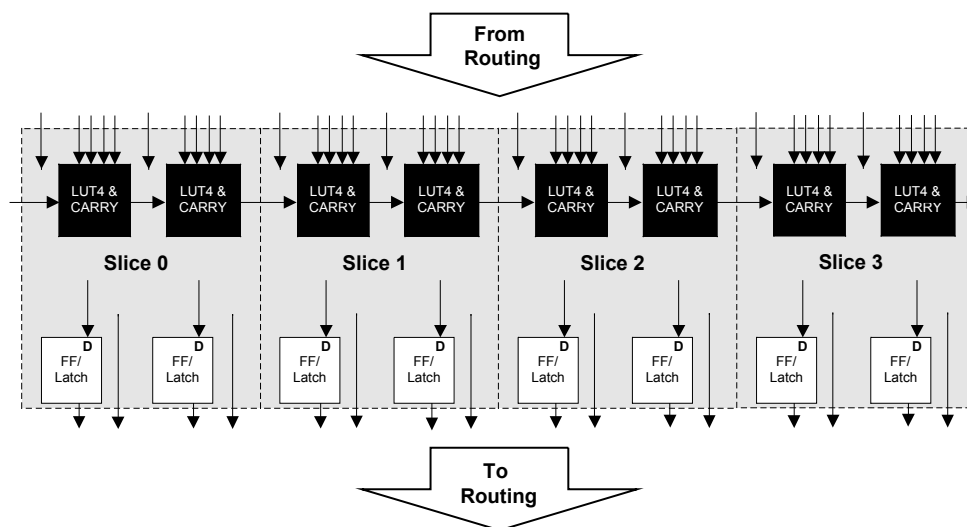
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10200
Total RAM Bits	282624
Number of I/O	288
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec10e-3f484i

PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-8. Per Quadrant Primary Clock Selection

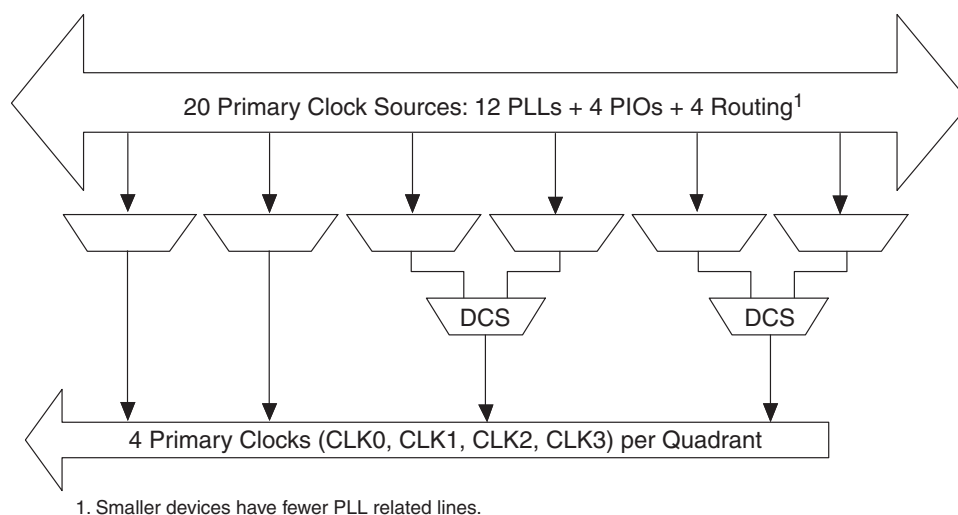


Figure 2-9. Per Quadrant Secondary Clock Selection

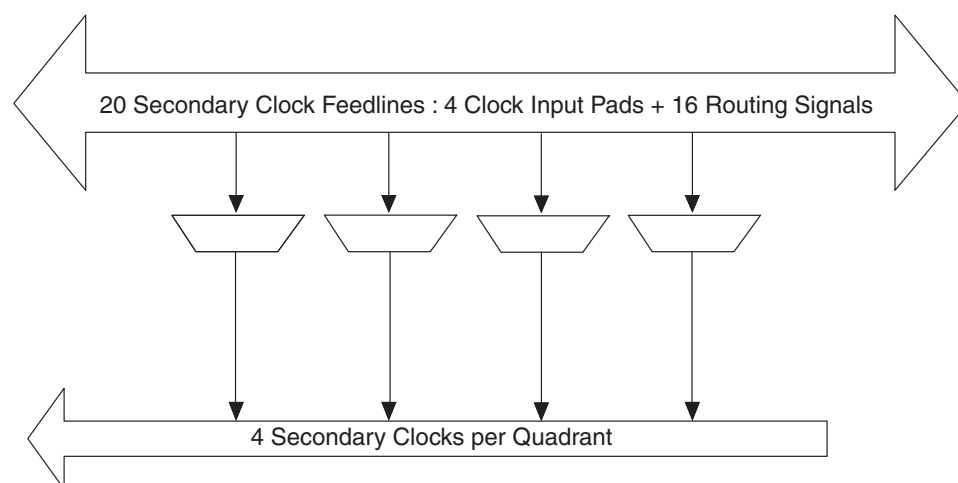
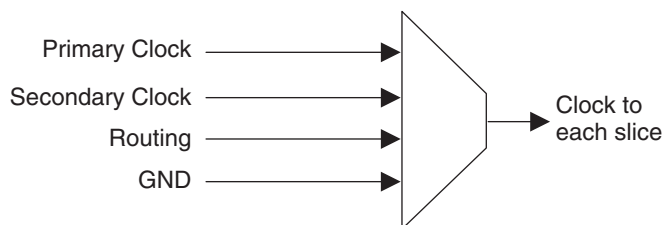


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from CLKOP (PLL Internal), from clock net (CLKOP) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

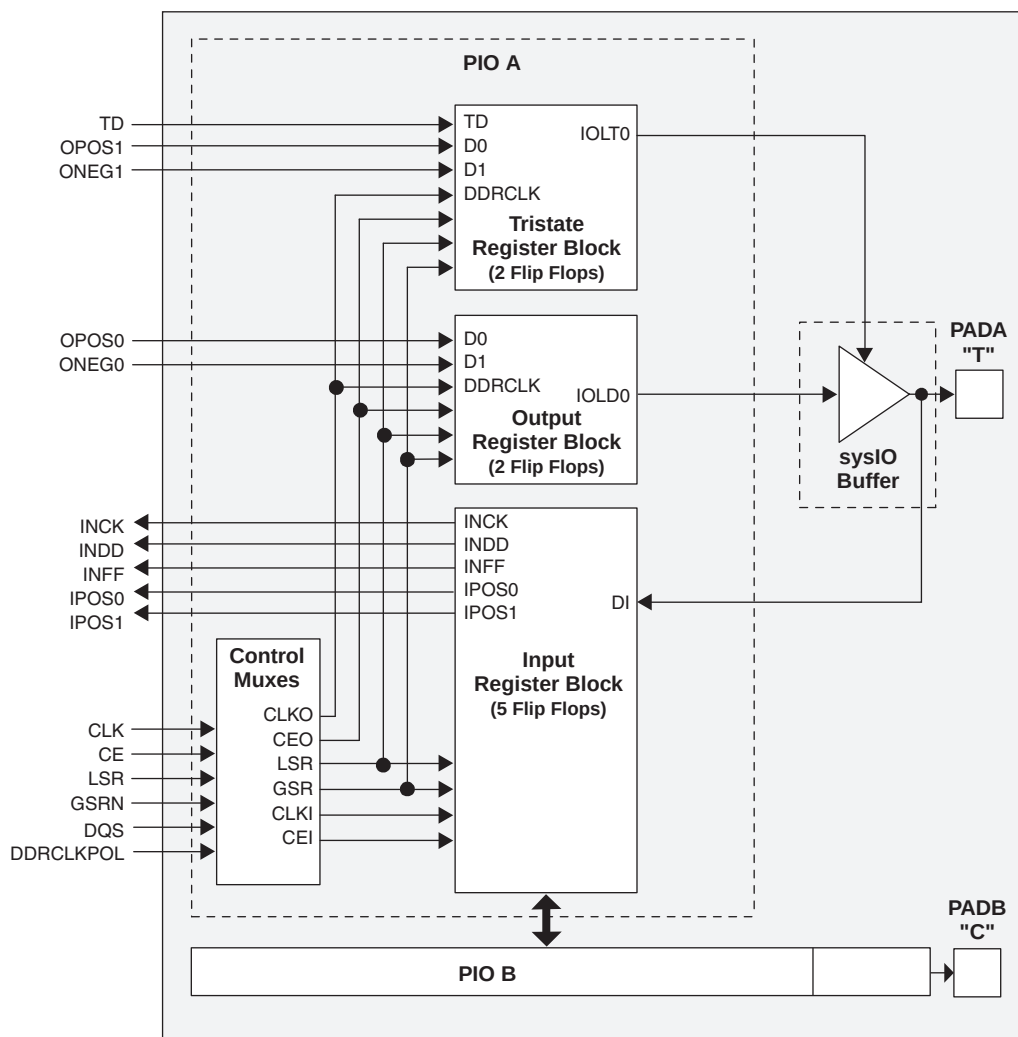
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either pro-

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

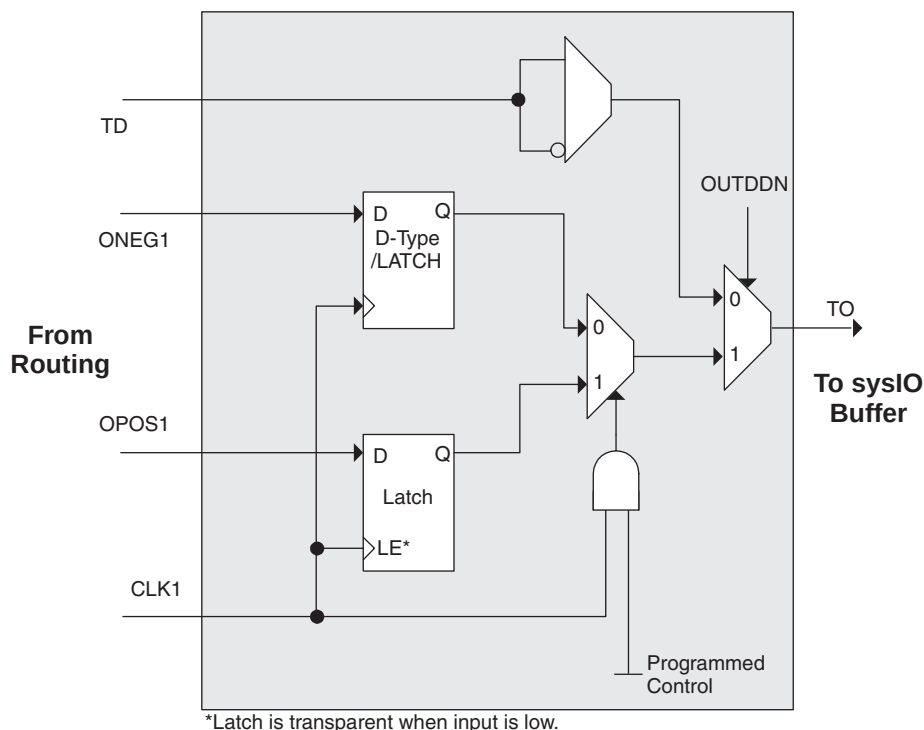
Figure 2-24. PIC Diagram



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Figure 2-31. Tristate Register Block



Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

DC Electrical Characteristics

Over Recommended Operating Conditions

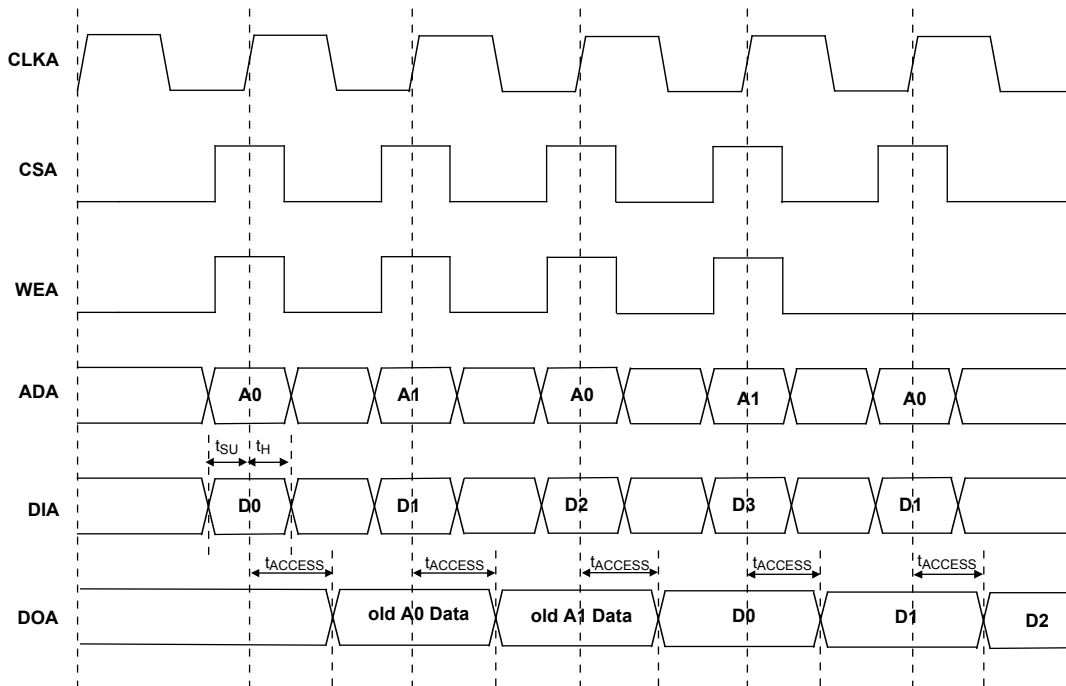
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}^1	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
$I_{IH}^{1,3}$	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) \leq V_{IH} \leq 3.6V$	—	—	40	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHLH}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	μA
V_{BHT}	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25°C, $f = 1.0MHz$

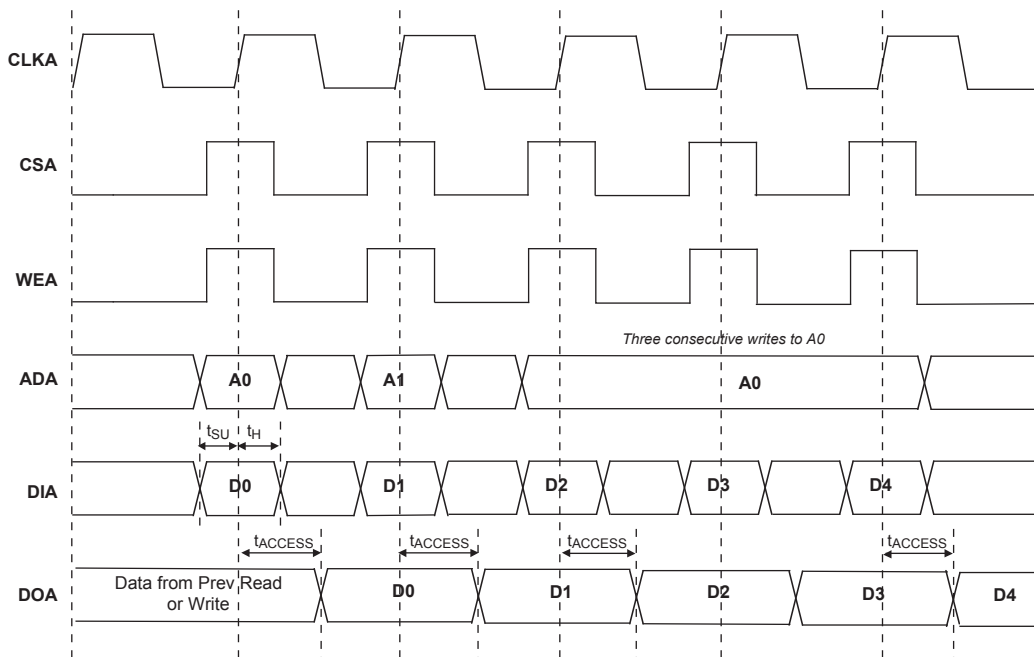
3. For top and bottom general purpose I/O pins, when V_{IH} is higher than V_{CCIO} , a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For left and right I/O banks, V_{IH} must be less than or equal to V_{CCIO} .

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	210	MHz
f_{VCO}	PLL VCO Frequency		420	—	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default Duty Cycle Elected ³	45	50	55	%
t_{PH}^4	Output Phase Accuracy		—	—	0.05	UI
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100\text{MHz}$	—	—	+/- 125	ps
		$f_{OUT} < 100\text{MHz}$	—	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	1	—	—	ns
t_{LOCK}^2	PLL Lock-in Time		—	—	150	μs
t_{PA}	Programmable Delay Unit		100	250	450	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width		10	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.

Timing v.G 0.30

Pin Information Summary (Cont.)

		LFEC/EC15		LFEC/EC20		LFEC/EC33	
Pin Type		256-fpBGA	484-fpBGA	484-fpBGA	672-fpBGA	484-fpBGA	672-fpBGA
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V _{CC}		10	20	20	32	16	28
V _{CCAUX}		2	12	12	20	12	20
V _{CCPLL}		0	0	0	0	4	4
V _{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V _{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFEC1, LFEC3, LFEC6/EC6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFEC1				LFEC3				LFEC6/EC6			
	Pin Function	Bank	LVD S	Dual Function	Pin Function	Bank	LVD S	Dual Function	Pin Function	Bank	LVD S	Dual Function
50	PB8B	5	C	VREF1_5	PB16B	5	C	VREF1_5	PB16B	5	C	VREF1_5
51	PB9A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0	PB17A	5	T	PCLKT5_0
52	GND5	5			GND5	5			GND5	5		
53	PB9B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0	PB17B	5	C	PCLKC5_0
54	VCCAUX	-			VCCAUX	-			VCCAUX	-		
55	VCCIO4	4			VCCIO4	4			VCCIO4	4		
56	PB10A	4	T	WRITEN	PB18A	4	T	WRITEN	PB18A	4	T	WRITEN
57	PB10B	4	C	CS1N	PB18B	4	C	CS1N	PB18B	4	C	CS1N
58	PB11A	4	T	VREF1_4	PB19A	4	T	VREF1_4	PB19A	4	T	VREF1_4
59	PB11B	4	C	CSN	PB19B	4	C	CSN	PB19B	4	C	CSN
60	PB12A	4	T	VREF2_4	PB20A	4	T	VREF2_4	PB20A	4	T	VREF2_4
61	PB12B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7	PB20B	4	C	D0/SPID7
62	PB13A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5	PB21A	4	T	D2/SPID5
63	GND4	4			GND4	4			GND4	4		
64	PB13B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6	PB21B	4	C	D1/SPID6
65	PB14A	4	T	BDQS14	PB22A	4	T	BDQS22	PB22A	4	T	BDQS22
66	PB14B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4	PB22B	4	C	D3/SPID4
67	PB15A	4	T		PB23A	4	T		PB23A	4	T	
68	PB15B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3	PB23B	4	C	D4/SPID3
69	PB16B	4		D5/SPID2	PB24B	4		D5/SPID2	PB24B	4		D5/SPID2
70	PB17B	4		D6/SPID1	PB25B	4		D6/SPID1	PB25B	4		D6/SPID1
71	VCCIO4	4			VCCIO4	4			VCCIO4	4		
72*	GND3 GND4	-			GND3 GND4	-			GND3 GND4	-		
73	VCCIO3	3			VCCIO3	3			VCCIO3	3		
74	PR14A	3		VREF1_3	PR18A	3		VREF1_3	PR27A	3		VREF1_3
75	PR12B	3	C		PR16B	3	C		PR25B	3	C	
76	PR12A	3	T		PR16A	3	T		PR25A	3	T	
77	PR11B	3	C		PR15B	3	C		PR24B	3	C	
78	PR11A	3	T	RDQS11	PR15A	3	T	RDQS15	PR24A	3	T	RDQS24
79	PR10B	3	C	RLM0_PLLC_FB_A	PR14B	3	C	RLM0_PLLC_FB_A	PR23B	3	C	RLM0_PLLC_FB_A
80	GND3	3			GND3	3			GND3	3		
81	PR10A	3	T	RLM0_PLLT_FB_A	PR14A	3	T	RLM0_PLLT_FB_A	PR23A	3	T	RLM0_PLLT_FB_A
82	PR9B	3	C	RLM0_PLLC_IN_A	PR13B	3	C	RLM0_PLLC_IN_A	PR22B	3	C	RLM0_PLLC_IN_A
83	PR9A	3	T	RLM0_PLLT_IN_A	PR13A	3	T	RLM0_PLLT_IN_A	PR22A	3	T	RLM0_PLLT_IN_A
84	VCCIO3	3			VCCIO3	3			VCCIO3	3		
85	PR8B	3	C	DI/CSSPIN	PR12B	3	C	DI/CSSPIN	PR21B	3	C	DI/CSSPIN
86	PR8A	3	T	DOU/CSON	PR12A	3	T	DOU/CSON	PR21A	3	T	DOU/CSON
87	PR7B	3	C	BUSY/SISPI	PR11B	3	C	BUSY/SISPI	PR20B	3	C	BUSY/SISPI
88	PR7A	3	T	D7/SPID0	PR11A	3	T	D7/SPID0	PR20A	3	T	D7/SPID0
89	CFG2	3			CFG2	3			CFG2	3		
90	CFG1	3			CFG1	3			CFG1	3		
91	CFG0	3			CFG0	3			CFG0	3		
92	VCC	-			VCC	-			VCC	-		
93	PROGRAMN	3			PROGRAMN	3			PROGRAMN	3		
94	CCLK	3			CCLK	3			CCLK	3		
95	INITN	3			INITN	3			INITN	3		
96	GND	-			GND	-			GND	-		
97	DONE	3			DONE	3			DONE	3		
98	GND	-			GND	-			GND	-		

LFEC1, LFEC3 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
127	CFG0	3			CFG0	3		
128	VCC	-			VCC	-		
129	PROGRAMN	3			PROGRAMN	3		
130	CCLK	3			CCLK	3		
131	INITN	3			INITN	3		
132	GND	-			GND	-		
133	DONE	3			DONE	3		
134	GND	-			GND	-		
135	VCC	-			VCC	-		
136	NC	-			VCCAUX	-		
137	PR5B	2	C	PCLKC2_0	PR9B	2	C	PCLKC2_0
138	NC	-			GND2	2		
139	PR5A	2	T	PCLKT2_0	PR9A	2	T	PCLKT2_0
140	PR4B	2	C		PR8B	2	C	
141	PR4A	2	T		PR8A	2	T	
142	PR3B	2	C		PR7B	2	C	
143	PR3A	2	T		PR7A	2	T	
144	NC	-			PR6B	2	C	
145	NC	-			VCCIO2	2		
146	NC	-			PR6A	2	T	RDQS6
147	NC	-			PR5B	2	C	
148	NC	-			PR5A	2	T	
149	NC	-			PR4B	2	C	
150	NC	-			PR4A	2	T	
151	NC	-			NC	-		
152	NC	-			NC	-		
153	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
154	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
155	VCCIO2	2			VCCIO2	2		
156*	GND1 GND2	-			GND1 GND2	-		
157	VCCIO1	1			VCCIO1	1		
158	NC	-			NC	-		
159	PT17B	1	C		PT25B	1	C	
160	PT17A	1	T		PT25A	1	T	
161	PT16B	1	C		PT24B	1	C	
162	PT16A	1	T		PT24A	1	T	
163	PT15B	1	C		PT23B	1	C	
164	PT15A	1	T		PT23A	1	T	
165	PT14B	1	C		PT22B	1	C	
166	PT14A	1	T	TDQS14	PT22A	1	T	TDQS22
167	PT13B	1	C		PT21B	1	C	
168	GND1	1			GND1	1		

LFEC6/EC6, LFEC6/EC10 Logic Signal Connections: 208 PQFP

Pin Number	LFEC6/LFEC6				LFEC10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			VCC	-		
6	NC	-			GND	-		
7	PL3B	7			PL12B	7		
8	PL4A	7	T		PL13A	7	T	
9	PL4B	7	C		PL13B	7	C	
10	PL5A	7	T		PL14A	7	T	
11	PL5B	7	C		PL14B	7	C	
12	PL6A	7	T	LDQS6	PL15A	7	T	LDQS15
13	VCCIO7	7			VCCIO7	7		
14	PL6B	7	C		PL15B	7	C	
15	PL7A	7	T		PL16A	7	T	
16	PL7B	7	C		PL16B	7	C	
17	PL8A	7	T		PL17A	7	T	
18	GND7	7			GND7	7		
19	PL8B	7	C		PL17B	7	C	
20	PL9A	7	T	PCLKT7_0	PL18A	7	T	PCLKT7_0
21	PL9B	7	C	PCLKC7_0	PL18B	7	C	PCLKC7_0
22	VCCAUX	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	VCC	-			VCC	-		
25	GND	-			GND	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL20A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A
34	PL20B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A
35	PL21A	6	T	LLM0_PLLT_FB_A	PL30A	6	T	LLM0_PLLT_FB_A
36	PL21B	6	C	LLM0_PLLC_FB_A	PL30B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL22A	6	T		PL31A	6	T	
39	PL22B	6	C		PL31B	6	C	
40	PL23A	6	T		PL32A	6	T	
41	GND6	6			GND6	6		
42	PL23B	6	C		PL32B	6	C	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
D7	PT11B	0	C		PT11B	0	C	
C7	PT11A	0	T		PT11A	0	T	
A7	PT10B	0	C		PT10B	0	C	
A6	PT10A	0	T		PT10A	0	T	
E7	PT9B	0	C		PT9B	0	C	
GND	GND0	0			GND0	0		
E6	PT9A	0	T		PT9A	0	T	
D6	PT8B	0	C		PT8B	0	C	
C6	PT8A	0	T		PT8A	0	T	
B6	PT7B	0	C		PT7B	0	C	
B5	PT7A	0	T		PT7A	0	T	
A5	PT6B	0	C		PT6B	0	C	
A4	PT6A	0	T	TDQS6	PT6A	0	T	TDQS6
A3	PT5B	0	C		PT5B	0	C	
A2	PT5A	0	T		PT5A	0	T	
B2	PT4B	0	C		PT4B	0	C	
B3	PT4A	0	T		PT4A	0	T	
D5	PT3B	0	C		PT3B	0	C	
C5	PT3A	0	T		PT3A	0	T	
C4	PT2B	0	C		PT2B	0	C	
B4	PT2A	0	T		PT2A	0	T	
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND7	7		
D4	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
D3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
GND	GND7	7			GND7	7		
C3	PL12A	7	T		PL16A	7	T	
C2	PL12B	7	C		PL16B	7	C	
B1	PL13A	7	T		PL17A	7	T	
C1	PL13B	7	C		PL17B	7	C	
E3	PL14A	7	T		PL18A	7	T	
GND	GND7	7			GND7	7		
-	-	-			GND7	7		
E4	PL14B	7	C		PL18B	7	C	
F4	PL15A	7	T	LDQS15	PL19A	7	T	LDQS19
F5	PL15B	7	C		PL19B	7	C	
G4	PL16A	7	T		PL20A	7	T	
G3	PL16B	7	C		PL20B	7	C	
D2	PL17A	7	T		PL21A	7	T	
D1	PL17B	7	C		PL21B	7	C	
E1	PL18A	7	T	PCLKT7_0	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND7	7		
E2	PL18B	7	C	PCLKC7_0	PL22B	7	C	PCLKC7_0
F3	XRES	6			XRES	6		
G5	PL20A	6	T		PL24A	6	T	
H5	PL20B	6	C		PL24B	6	C	
F2	PL21A	6	T		PL25A	6	T	
F1	PL21B	6	C		PL25B	6	C	
H4	PL22A	6	T		PL26A	6	T	
H3	PL22B	6	C		PL26B	6	C	
G2	PL23A	6	T		PL27A	6	T	
GND	GND6	6			GND6	6		
G1	PL23B	6	C		PL27B	6	C	
J4	PL24A	6	T	LDQS24	PL28A	6	T	LDQS28
J3	PL24B	6	C		PL28B	6	C	
J5	PL25A	6	T		PL29A	6	T	
K5	PL25B	6	C		PL29B	6	C	
H2	PL26A	6	T		PL30A	6	T	
H1	PL26B	6	C		PL30B	6	C	
J2	PL27A	6	T		PL31A	6	T	
GND	GND6	6			GND6	6		
J1	PL27B	6	C		PL31B	6	C	
K4	TCK	6			TCK	6		
K3	TDI	6			TDI	6		

LFEC20/EC20 and LFEC20/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFEC20/LFEC20					LFEC20/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR17A	2	T	RUM0_PLLT_FB_A
G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR16B	2	C	RUM0_PLLC_IN_A
G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR16A	2	T	RUM0_PLLT_IN_A
F20	PR7B	2	C		F20	PR15B	2	C	
F19	PR7A	2	T		F19	PR15A	2	T	
E20	PR6B	2	C		E20	PR14B	2	C	
D20	PR6A	2	T	RDQS6	D20	PR14A	2	T	RDQS14
C21	PR5B	2	C		C21	PR13B	2	C	
GND	-	-			GND	GND2	2		
C20	PR5A	2	T		C20	PR13A	2	T	
F18	PR4B	2	C		F18	PR12B	2	C	
E18	PR4A	2	T		E18	PR12A	2	T	
B22	PR3B	2	C		B22	PR11B	2	C	
B21	PR3A	2	T		B21	PR11A	2	T	
GND	-	-			GND	GND2	2		
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
GND	-	-			GND	GND1	1		
G17	PT57B	1	C		G17	PT57B	1	C	
GND	-	-			GND	GND1	1		
F17	PT57A	1	T		F17	PT57A	1	T	
D18	PT56B	1	C		D18	PT56B	1	C	
C18	PT56A	1	T		C18	PT56A	1	T	
C19	PT55B	1	C		C19	PT55B	1	C	
B20	PT55A	1	T		B20	PT55A	1	T	
D17	PT54B	1	C		D17	PT54B	1	C	
C16	PT54A	1	T	TDQS54	C16	PT54A	1	T	TDQS54
B19	PT53B	1	C		B19	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
A20	PT53A	1	T		A20	PT53A	1	T	
E17	PT52B	1	C		E17	PT52B	1	C	
C17	PT52A	1	T		C17	PT52A	1	T	
F16	PT51B	1	C		F16	PT51B	1	C	
E16	PT51A	1	T		E16	PT51A	1	T	
F15	PT50B	1	C		F15	PT50B	1	C	
D16	PT50A	1	T		D16	PT50A	1	T	
B18	PT49B	1	C		B18	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
A19	PT49A	1	T		A19	PT49A	1	T	
B17	PT48B	1	C		B17	PT48B	1	C	
A18	PT48A	1	T		A18	PT48A	1	T	
B16	PT47B	1	C		B16	PT47B	1	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AC13	PB32B	5	C	VREF1_5	AC13	PB32B	5	C	VREF1_5
AF14	PB33A	5	T	PCLKT5_0	AF14	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AE14	PB33B	5	C	PCLKC5_0	AE14	PB33B	5	C	PCLKC5_0
AA13	PB34A	4	T	WRITEN	AA13	PB34A	4	T	WRITEN
AB13	PB34B	4	C	CS1N	AB13	PB34B	4	C	CS1N
AD14	PB35A	4	T	VREF1_4	AD14	PB35A	4	T	VREF1_4
AA14	PB35B	4	C	CSN	AA14	PB35B	4	C	CSN
AC14	PB36A	4	T	VREF2_4	AC14	PB36A	4	T	VREF2_4
AB14	PB36B	4	C	D0/SPID7	AB14	PB36B	4	C	D0/SPID7
AF15	PB37A	4	T	D2/SPID5	AF15	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AE15	PB37B	4	C	D1/SPID6	AE15	PB37B	4	C	D1/SPID6
AD15	PB38A	4	T	BDQS38	AD15	PB38A	4	T	BDQS38
AC15	PB38B	4	C	D3/SPID4	AC15	PB38B	4	C	D3/SPID4
AF16	PB39A	4	T		AF16	PB39A	4	T	
Y14	PB39B	4	C	D4/SPID3	Y14	PB39B	4	C	D4/SPID3
AE16	PB40A	4	T		AE16	PB40A	4	T	
AB15	PB40B	4	C	D5/SPID2	AB15	PB40B	4	C	D5/SPID2
AF17	PB41A	4	T		AF17	PB41A	4	T	
GND	GND4	4			GND	GND4	4		
AE17	PB41B	4	C	D6/SPID1	AE17	PB41B	4	C	D6/SPID1
Y15	PB42A	4	T		Y15	PB42A	4	T	
AA15	PB42B	4	C		AA15	PB42B	4	C	
AD17	PB43A	4	T		AD17	PB43A	4	T	
Y16	PB43B	4	C		Y16	PB43B	4	C	
AD18	PB44A	4	T		AD18	PB44A	4	T	
AC16	PB44B	4	C		AC16	PB44B	4	C	
AE18	PB45A	4	T		AE18	PB45A	4	T	
GND	GND4	4			GND	GND4	4		
AF18	PB45B	4	C		AF18	PB45B	4	C	
AD16	PB46A	4	T	BDQS46	AD16	PB46A	4	T	BDQS46
AB16	PB46B	4	C		AB16	PB46B	4	C	
AF19	PB47A	4	T		AF19	PB47A	4	T	
AA16	PB47B	4	C		AA16	PB47B	4	C	
AA17	PB48A	4	T		AA17	PB48A	4	T	
Y17	PB48B	4	C		Y17	PB48B	4	C	
AF21	PB49A	4	T		AF21	PB49A	4	T	
GND	GND4	4			GND	GND4	4		
AF20	PB49B	4	C		AF20	PB49B	4	C	
AE21	PB50A	4	T		AE21	PB50A	4	T	
AC17	PB50B	4	C		AC17	PB50B	4	C	

Conventional Packaging
LatticeEC Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208C	112	-3	PQFP	208	COM	1.5K
LFEC1E-4Q208C	112	-4	PQFP	208	COM	1.5K
LFEC1E-5Q208C	112	-5	PQFP	208	COM	1.5K
LFEC1E-3T144C	97	-3	TQFP	144	COM	1.5K
LFEC1E-4T144C	97	-4	TQFP	144	COM	1.5K
LFEC1E-5T144C	97	-5	TQFP	144	COM	1.5K
LFEC1E-3T100C	67	-3	TQFP	100	COM	1.5K
LFEC1E-4T100C	67	-4	TQFP	100	COM	1.5K
LFEC1E-5T100C	67	-5	TQFP	100	COM	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256C	160	-3	fpBGA	256	COM	3.1K
LFEC3E-4F256C	160	-4	fpBGA	256	COM	3.1K
LFEC3E-5F256C	160	-5	fpBGA	256	COM	3.1K
LFEC3E-3Q208C	145	-3	PQFP	208	COM	3.1K
LFEC3E-4Q208C	145	-4	PQFP	208	COM	3.1K
LFEC3E-5Q208C	145	-5	PQFP	208	COM	3.1K
LFEC3E-3T144C	97	-3	TQFP	144	COM	3.1K
LFEC3E-4T144C	97	-4	TQFP	144	COM	3.1K
LFEC3E-5T144C	97	-5	TQFP	144	COM	3.1K
LFEC3E-3T100C	67	-3	TQFP	100	COM	3.1K
LFEC3E-4T100C	67	-4	TQFP	100	COM	3.1K
LFEC3E-5T100C	67	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFEC6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFEC6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFEC6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFEC6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFEC6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFEC6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFEC6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFEC6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFEC6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFEC6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFEC6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFEC10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFEC10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFEC10E-3F256C	195	-3	fpBGA	256	COM	10.2K

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP6E-3FN484C	224	-3	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-4FN484C	224	-4	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-5FN484C	224	-5	Lead-Free fpBGA	484	COM	6.1K
LFCEP6E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	6.1K
LFCEP6E-3QN208C	147	-3	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-4QN208C	147	-4	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-5QN208C	147	-5	Lead-Free PQFP	208	COM	6.1K
LFCEP6E-3TN144C	97	-3	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-4TN144C	97	-4	Lead-Free TQFP	144	COM	6.1K
LFCEP6E-5TN144C	97	-5	Lead-Free TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP10E-3FN484C	288	-3	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-4FN484C	288	-4	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-5FN484C	288	-5	Lead-Free fpBGA	484	COM	10.2K
LFCEP10E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	10.2K
LFCEP10E-3QN208C	147	-3	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-4QN208C	147	-4	Lead-Free PQFP	208	COM	10.2K
LFCEP10E-5QN208C	147	-5	Lead-Free PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP15E-3FN484C	352	-3	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-4FN484C	352	-4	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-5FN484C	352	-5	Lead-Free fpBGA	484	COM	15.3K
LFCEP15E-3FN256C	195	-3	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-4FN256C	195	-4	Lead-Free fpBGA	256	COM	15.3K
LFCEP15E-5FN256C	195	-5	Lead-Free fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP20E-3FN672C	400	-3	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-4FN672C	400	-4	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-5FN672C	400	-5	Lead-Free fpBGA	672	COM	19.7K
LFCEP20E-3FN484C	400	-3	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-4FN484C	400	-4	Lead-Free fpBGA	484	COM	19.7K
LFCEP20E-5FN484C	400	-5	Lead-Free fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFCEP33E-3FN672C	496	-3	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-4FN672C	496	-4	Lead-Free fpBGA	672	COM	32.8K
LFCEP33E-5FN672C	496	-5	Lead-Free fpBGA	672	COM	32.8K

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFECP33E-3FN484C	360	-3	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-4FN484C	360	-4	Lead-Free fpBGA	484	COM	32.8K
LFECP33E-5FN484C	360	-5	Lead-Free fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC1E-3QN208I	112	-3	Lead-Free PQFP	208	IND	1.5K
LFEC1E-4QN208I	112	-4	Lead-Free PQFP	208	IND	1.5K
LFEC1E-3TN144I	97	-3	Lead-Free TQFP	144	IND	1.5K
LFEC1E-4TN144I	97	-4	Lead-Free TQFP	144	IND	1.5K
LFEC1E-3TN100I	67	-3	Lead-Free TQFP	100	IND	1.5K
LFEC1E-4TN100I	67	-4	Lead-Free TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC3E-3FN256I	160	-3	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-4FN256I	160	-4	Lead-Free fpBGA	256	IND	3.1K
LFEC3E-3QN208I	145	-3	Lead-Free PQFP	208	IND	3.1K
LFEC3E-4QN208I	145	-4	Lead-Free PQFP	208	IND	3.1K
LFEC3E-3TN144I	97	-3	Lead-Free TQFP	144	IND	3.1K
LFEC3E-4TN144I	97	-4	Lead-Free TQFP	144	IND	3.1K
LFEC3E-3TN100I	67	-3	Lead-Free TQFP	100	IND	3.1K
LFEC3E-4TN100I	67	-4	Lead-Free TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K

LatticeEC Industrial (Continued)

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC20E-3FN672I	400	-3	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-4FN672I	400	-4	Lead-Free fpBGA	672	IND	19.7K
LFEC20E-3FN484I	400	-3	Lead-Free fpBGA	484	IND	19.7K
LFEC20E-4FN484I	400	-4	Lead-Free fpBGA	484	IND	19.7K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC33E-3FN672I	496	-3	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-4FN672I	496	-4	Lead-Free fpBGA	672	IND	32.8K
LFEC33E-3FN484I	360	-3	Lead-Free fpBGA	484	IND	32.8K
LFEC33E-4FN484I	360	-4	Lead-Free fpBGA	484	IND	32.8K

LatticeECP Industrial

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC6E-3FN484I	224	-3	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-4FN484I	224	-4	Lead-Free fpBGA	484	IND	6.1K
LFEC6E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	6.1K
LFEC6E-3QN208I	147	-3	Lead-Free PQFP	208	IND	6.1K
LFEC6E-4QN208I	147	-4	Lead-Free PQFP	208	IND	6.1K
LFEC6E-3TN144I	97	-3	Lead-Free TQFP	144	IND	6.1K
LFEC6E-4TN144I	97	-4	Lead-Free TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC10E-3FN484I	288	-3	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-4FN484I	288	-4	Lead-Free fpBGA	484	IND	10.2K
LFEC10E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	10.2K
LFEC10E-3QN208I	147	-3	Lead-Free PQFP	208	IND	10.2K
LFEC10E-4QN208I	147	-4	Lead-Free PQFP	208	IND	10.2K

Part Number	I/Os	Grade	Package	Pins/Balls	Temp.	LUTs
LFEC15E-3FN484I	352	-3	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-4FN484I	352	-4	Lead-Free fpBGA	484	IND	15.3K
LFEC15E-3FN256I	195	-3	Lead-Free fpBGA	256	IND	15.3K
LFEC15E-4FN256I	195	-4	Lead-Free fpBGA	256	IND	15.3K



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Data Sheet

For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeECP-DSP sysDSP Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com