Lattice Semiconductor Corporation - LFEC10E-3FN256I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10200
Total RAM Bits	282624
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec10e-3fn256i

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SPR16x2	ROM16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

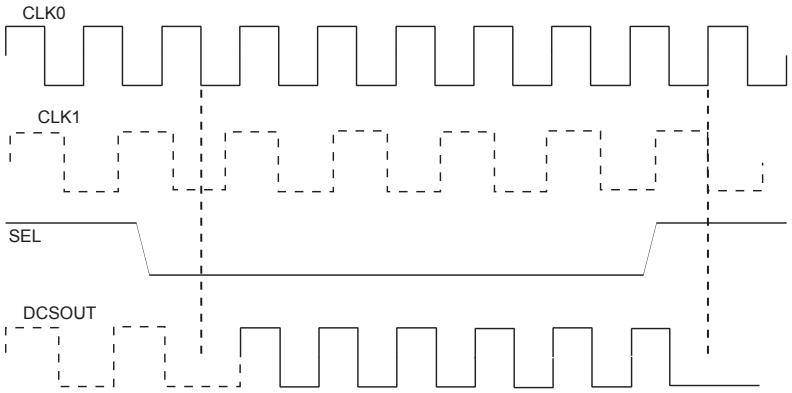
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-5 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information about using RAM in LatticeECP/EC devices, please see the list of technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-14. DCS Waveforms



sysMEM Memory

The LatticeECP/EC devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

IPexpress™

The user can access the sysDSP block via the IPexpress configuration tool, included with the ispLEVER design tool suite. IPexpress has options to configure each DSP module (or group of modules) or through direct HDL instantiation. Additionally Lattice has partnered Mathworks to support instantiation in the Simulink tool, which is a Graphical Simulation Environment. Simulink works with ispLEVER and dramatically shortens the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IPs planned for LatticeECP DSP are: Bit Correlators, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/ Decoder, Turbo Encoder/Decoders and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IPs.

Resources Available in the LatticeECP Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP family. Table 2-10 shows the maximum available EBR RAM Blocks in each of the LatticeECP family. EBR blocks, together with Distributed RAM can be used to store variables locally for the fast DSP operations.

Table 2-9. Number of DSP Blocks in LatticeECP Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
LFECP6	4	32	16	4
LFECP10	5	40	20	5
LFECP15	6	48	24	6
LFECP20	7	56	28	7
LFECP33	8	64	32	8

Table 2-10. Embedded SRAM in LatticeECP Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
LFECP6	10	92
LFECP10	30	276
LFECP15	38	350
LFECP20	46	424
LFECP33	54	498

DSP Performance of the LatticeECP Family

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP family.

Table 2-11. DSP Block Performance of LatticeECP Family

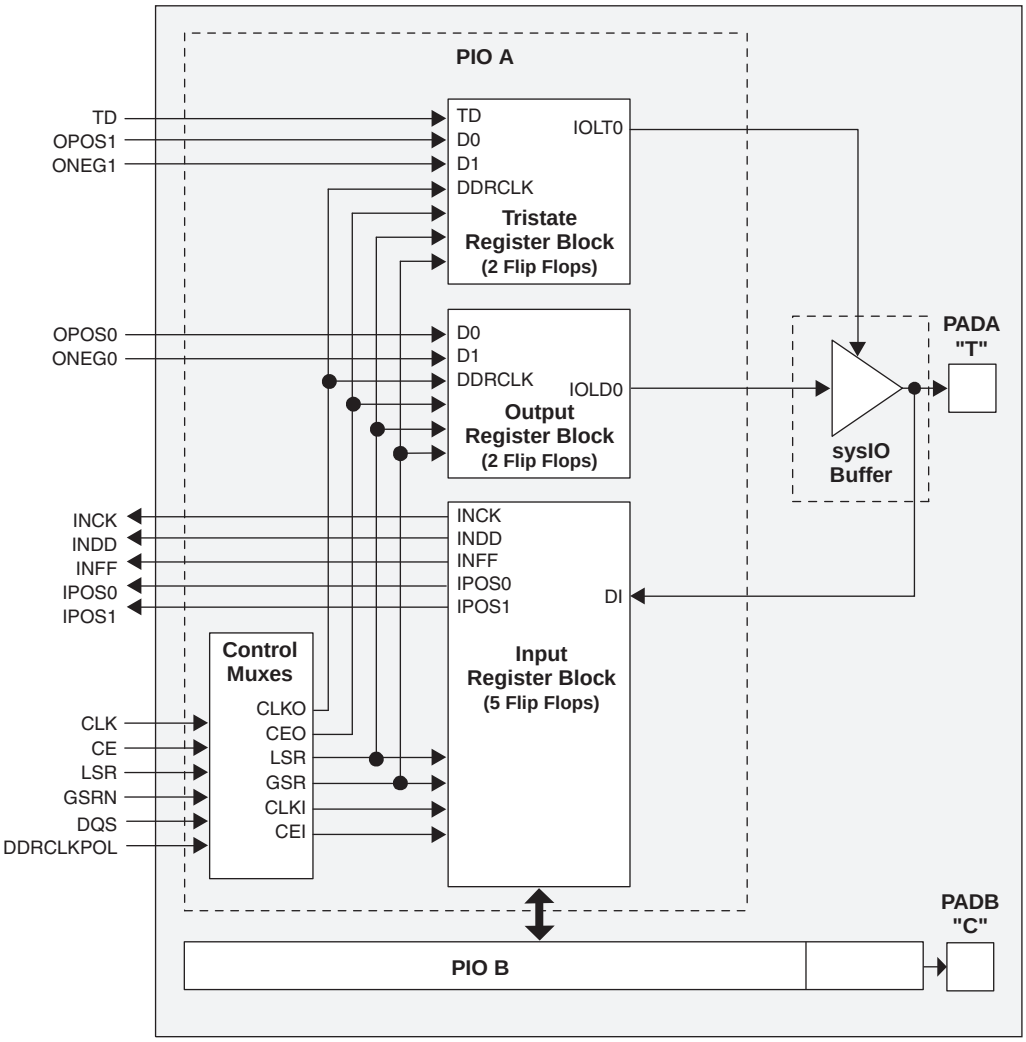
Device	DSP Block	DSP Performance MMAC
LFECP6	4	3680
LFECP10	5	4600
LFECP15	6	5520
LFECP20	7	6440
LFECP33	8	7360

For further information about the sysDSP block, please see the list of technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O Buffers which are then connected to the PADs as shown in Figure 2-24. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysI/O buffer, and receives input from the buffer.

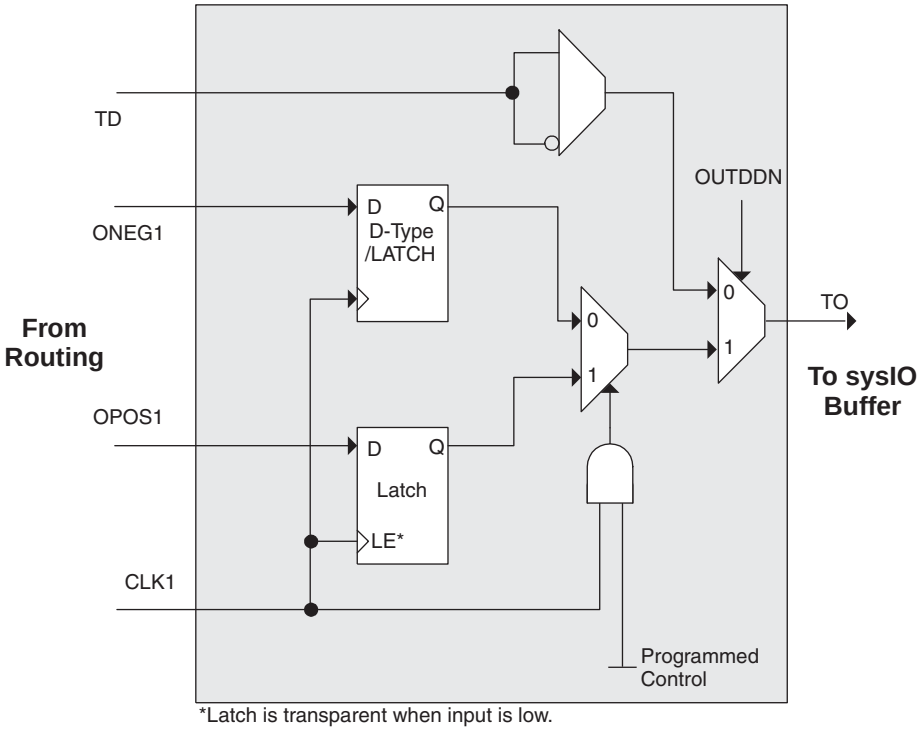
Figure 2-24. PIC Diagram



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-25 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Figure 2-31. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-32. DQS Local Bus.

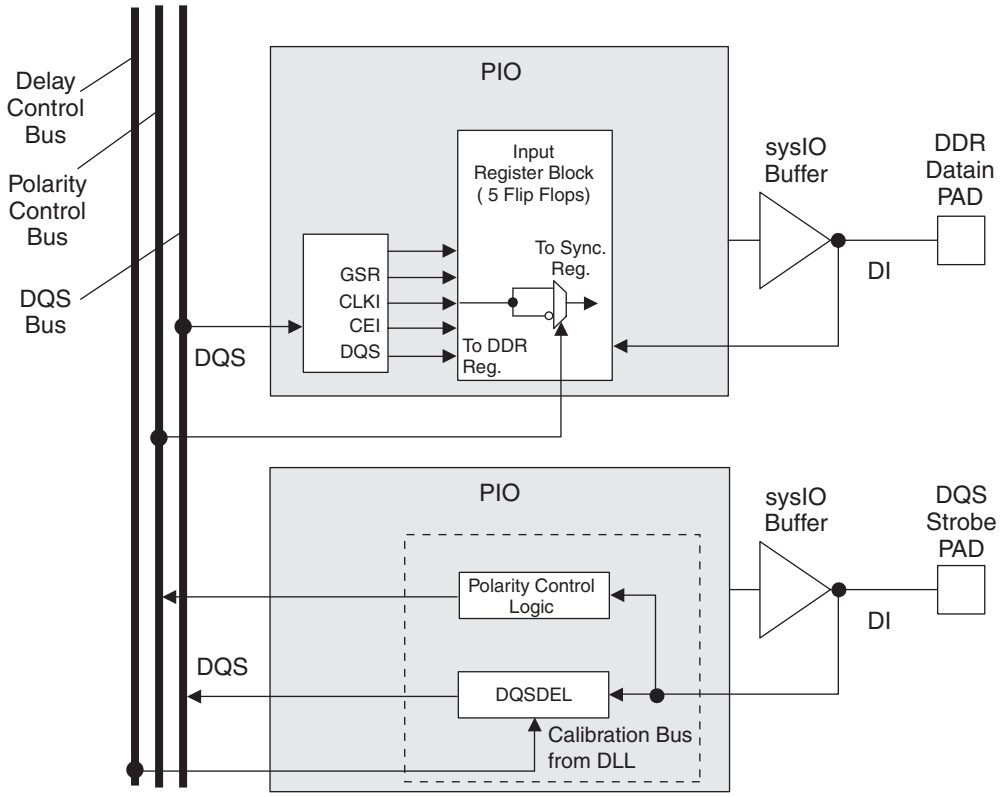
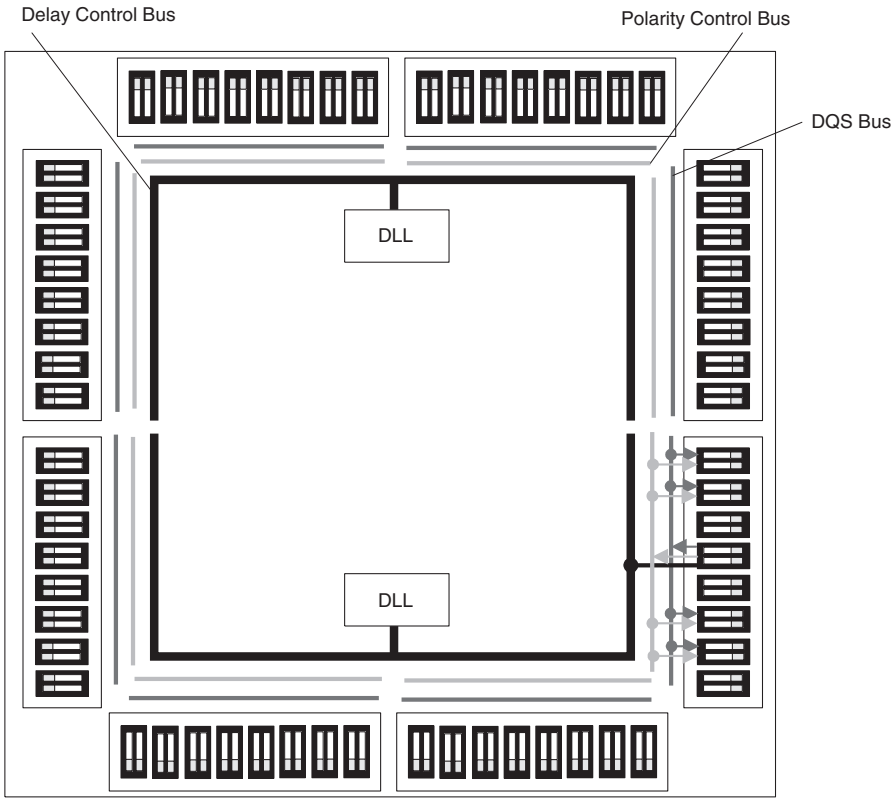


Figure 2-33. DLL Calibration Bus and DQS/DQS Transition Distribution



LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
t_{SOE}	CSSPIN Active Setup Time	300		—	ns
t_{CSPID}	CSSPIN Low to First Clock Edge Setup Time	300+3cyc		600+6cyc	ns
f_{MAXSPI}	Max Frequency for SPI	—		25	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	1		—	ns

Timing v.G 0.30

Master Clock

Clock Mode	Min.	Typ.	Max.	Units
2.5MHz	1.75	2.5	3.25	MHz
5 MHz	3.78	5.4	7.02	MHz
10 MHz	7	10	13	MHz
15 MHz	10.5	15	19.5	MHz
20 MHz	14	20	26	MHz
25 MHz	18.2	26	33.8	MHz
30 MHz	21	30	39	MHz
35 MHz	23.8	34	44.2	MHz
40 MHz	28.7	41	53.3	MHz
45 MHz	31.5	45	58.5	MHz
50 MHz	35.7	51	66.3	MHz
55 MHz	38.5	55	71.5	MHz
60 MHz	42	60	78	MHz
Duty Cycle	40	—	60	%

Timing v.G 0.30

Pin Information Summary

Pin Type		LFEC1			LFEC3				LFECP6/EC6				LFECP/EC10		
		100-TQFP	144-TQFP	208-PQFP	100-TQFP	144-TQFP	208-PQFP	256-fpBGA	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	208-PQFP	256-fpBGA	484-fpBGA
Single Ended User I/O		67	97	112	67	97	145	160	97	147	195	224	147	195	288
Differential Pair User I/O		29	46	56	29	46	72	80	46	72	97	112	72	97	144
Configuration	Dedicated	13	13	13	13	13	13	13	13	13	13	13	13	13	13
	Muxed	48	48	48	48	48	48	48	48	48	48	48	56	56	56
TAP		5	5	5	5	5	5	5	5	5	5	5	5	5	5
Dedicated (total without supplies)		80	110	160	80	110	160	208	110	160	208	373	160	208	373
V_{CC}		2	3	3	2	3	3	10	4	4	10	20	6	10	20
V_{CCAUX}		2	2	2	4	4	4	4	2	4	2	12	4	2	12
V_{CCPLL}		0	0	0	0	0	0	0	0	0	0	0	0	0	0
V_{CCIO}	Bank0	1	2	2	1	2	3	2	2	3	2	4	3	2	4
	Bank1	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank2	1	1	1	2	2	2	2	1	2	2	4	2	2	4
	Bank3	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank4	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank5	1	2	2	1	2	2	2	2	3	2	4	3	2	4
	Bank6	1	2	2	1	2	2	2	2	2	2	4	2	2	4
	Bank7	1	1	1	2	2	2	2	1	2	2	4	2	2	4
GND, GND0-GND7		8	13	13	8	13	16	20	14	18	20	44	20	20	44
NC		0	2	51	0	2	9	35	0	4	0	139	0	0	75
Single Ended/ Differential I/O Pair per Bank	Bank 0	11/5	14/7	16/8	11/5	14/7	26/13	32/16	14/7	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 1	11/5	13/6	16/8	11/5	13/6	16/8	16/8	13/6	17/8	18/9	32/16	17/8	18/9	32/16
	Bank 2	3/1	8/4	8/4	3/1	8/4	14/7	16/8	8/4	14/7	16/8	16/8	14/7	16/8	32/16
	Bank 3	8/4	13/6	16/8	8/4	13/6	16/8	16/8	13/6	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 4	12/4	14/6	16/8	12/4	14/6	16/8	16/8	14/6	17/8	17/8	32/16	17/8	17/8	32/16
	Bank 5	9/4	13/6	16/8	9/4	13/6	26/13	32/16	13/6	26/13	32/16	32/16	26/13	32/16	48/24
	Bank 6	5/2	14/7	16/8	5/2	14/7	16/8	16/8	14/7	16/8	32/16	32/16	16/8	32/16	32/16
	Bank 7	8/4	8/4	8/4	8/4	8/4	15/7	16/8	8/4	15/7	16/8	16/8	15/7	16/8	32/16
V_{CCJ}		1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

Pin Information Summary (Cont.)

Pin Type		LFECP/EC15		LFECP20/EC20		LFECP/EC33	
		256-fpBGA	484-fpBGA	484-fpBGA	672-fpBGA	484-fpBGA	672-fpBGA
Single Ended User I/O		195	352	360	400	360	496
Differential Pair User I/O		97	176	180	200	180	248
Configuration	Dedicated	13	13	13	13	13	13
	Muxed	56	56	56	56	56	56
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		208	373	373	509	373	509
V_{CC}		10	20	20	32	16	28
V_{CCAUX}		2	12	12	20	12	20
V_{CCPLL}		0	0	0	0	4	4
V_{CCIO}	Bank0	2	4	4	6	4	6
	Bank1	2	4	4	6	4	6
	Bank2	2	4	4	6	4	6
	Bank3	2	4	4	6	4	6
	Bank4	2	4	4	6	4	6
	Bank5	2	4	4	6	4	6
	Bank6	2	4	4	6	4	6
	Bank7	2	4	4	6	4	6
GND, GND0-GND7		20	44	44	63	44	63
NC		0	11	3	96	3	0
Single Ended/ Differential I/O Pair per Bank	Bank0	32/16	48/24	48/24	64/32	48/24	64/32
	Bank1	18/9	48/24	48/24	48/24	48/24	64/32
	Bank2	16/8	40/20	40/20	40/20	40/20	56/28
	Bank3	32/16	40/20	44/22	48/24	44/22	64/32
	Bank4	17/8	48/24	48/24	48/24	48/24	64/32
	Bank5	32/16	48/24	48/24	64/32	48/24	64/32
	Bank6	32/16	40/20	44/22	48/24	44/22	64/32
	Bank7	16/8	40/20	40/20	40/20	40/20	56/28
V_{CCJ}		1	1	1	1	1	1

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
43	PL24A	6	T	LDQS24	PL33A	6	T	LDQS33
44	PL24B	6	C		PL33B	6	C	
45	PL25A	6	T		PL34A	6	T	
46	PL25B	6	C		PL34B	6	C	
47	PL26A	6	T		PL35A	6	T	
48	PL26B	6	C		PL35B	6	C	
49	PL27A	6	T	VREF1_6	PL36A	6	T	VREF1_6
50	PL27B	6	C	VREF2_6	PL36B	6	C	VREF2_6
51	VCCIO6	6			VCCIO6	6		
52*	GND5 GND6	-			GND5 GND6	-		
53	VCCIO5	5			VCCIO5	5		
54	PB2A	5	T		PB2A	5	T	
55	PB2B	5	C		PB2B	5	C	
56	PB3A	5	T		PB3A	5	T	
57	PB3B	5	C		PB3B	5	C	
58	PB4A	5	T		PB4A	5	T	
59	PB4B	5	C		PB4B	5	C	
60	PB5A	5	T		PB5A	5	T	
61	PB5B	5	C		PB5B	5	C	
62	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
63	PB6B	5	C		PB6B	5	C	
64	VCCIO5	5			VCCIO5	5		
65	PB10A	5	T		PB18A	5	T	
66	PB10B	5	C		PB18B	5	C	
67	PB11A	5	T		PB19A	5	T	
68	PB11B	5	C		PB19B	5	C	
69	PB12A	5	T		PB20A	5	T	
70	PB12B	5	C		PB20B	5	C	
71	PB13A	5	T		PB21A	5	T	
72	GND5	5			GND5	5		
73	PB13B	5	C		PB21B	5	C	
74	VCCIO5	5			VCCIO5	5		
75	PB14A	5	T	BDQS14	PB22A	5	T	BDQS22
76	PB14B	5	C		PB22B	5	C	
77	PB15A	5	T		PB23A	5	T	
78	PB15B	5	C		PB23B	5	C	
79	PB16A	5	T	VREF2_5	PB24A	5	T	VREF2_5
80	PB16B	5	C	VREF1_5	PB24B	5	C	VREF1_5
81	PB17A	5	T	PCLKT5_0	PB25A	5	T	PCLKT5_0
82	GND5	5			GND5	5		
83	PB17B	5	C	PCLKC5_0	PB25B	5	C	PCLKC5_0
84	VCCAUX	-			VCCAUX	-		

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
E5	VCC	-			VCC	-		
E8	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M5	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
B15	VCCAUX	-			VCCAUX	-		
R2	VCCAUX	-			VCCAUX	-		
F7	VCCIO0	0			VCCIO0	0		
F8	VCCIO0	0			VCCIO0	0		
F10	VCCIO1	1			VCCIO1	1		
F9	VCCIO1	1			VCCIO1	1		
G11	VCCIO2	2			VCCIO2	2		
H11	VCCIO2	2			VCCIO2	2		
J11	VCCIO3	3			VCCIO3	3		
K11	VCCIO3	3			VCCIO3	3		
L10	VCCIO4	4			VCCIO4	4		
L9	VCCIO4	4			VCCIO4	4		
L7	VCCIO5	5			VCCIO5	5		
L8	VCCIO5	5			VCCIO5	5		
J6	VCCIO6	6			VCCIO6	6		
K6	VCCIO6	6			VCCIO6	6		
G6	VCCIO7	7			VCCIO7	7		
H6	VCCIO7	7			VCCIO7	7		
F6	VCC	-			VCC	-		
F11	VCC	-			VCC	-		
L11	VCC	-			VCC	-		
L6	VCC	-			VCC	-		

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7			GND	GND7	7		
D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7	D4	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
C3	NC	-			C3	PL3A	7	T		C3	PL3A	7	T	
B2	NC	-			B2	PL3B	7	C		B2	PL3B	7	C	
E5	NC	-			E5	PL4A	7	T		E5	PL4A	7	T	
F5	NC	-			F5	PL4B	7	C		F5	PL4B	7	C	
D3	NC	-			D3	PL5A	7	T		D3	PL5A	7	T	
C2	NC	-			C2	PL5B	7	C		C2	PL5B	7	C	
F4	NC	-			F4	PL6A	7	T	LDQS6	F4	PL6A	7	T	LDQS6
G4	NC	-			G4	PL6B	7	C		G4	PL6B	7	C	
E3	NC	-			E3	PL7A	7	T		E3	PL7A	7	T	
D2	NC	-			D2	PL7B	7	C		D2	PL7B	7	C	
B1	NC	-			B1	PL8A	7	T	LUM0_PLLT_IN_A	B1	PL8A	7	T	LUM0_PLLT_IN_A
C1	NC	-			C1	PL8B	7	C	LUM0_PLLC_IN_A	C1	PL8B	7	C	LUM0_PLLC_IN_A
F3	NC	-			F3	PL9A	7	T	LUM0_PLLT_FB_A	F3	PL9A	7	T	LUM0_PLLT_FB_A
GND	-	-			GND	GND7	7			GND	GND7	7		
E2	NC	-			E2	PL9B	7	C	LUM0_PLLC_FB_A	E2	PL9B	7	C	LUM0_PLLC_FB_A
G5	NC	-			G5	NC	-			G5	PL11A	7	T	
H6	NC	-			H6	NC	-			H6	PL11B	7	C	
G3	NC	-			G3	NC	-			G3	PL12A	7	T	
H4	NC	-			H4	NC	-			H4	PL12B	7	C	
J5	NC	-			J5	NC	-			J5	PL13A	7	T	
H5	NC	-			H5	NC	-			H5	PL13B	7	C	
F2	NC	-			F2	NC	-			F2	PL14A	7	T	
GND	-	-			GND	-	-			GND	GND7	7		
F1	NC	-			F1	NC	-			F1	PL14B	7	C	
E1	NC	-			E1	PL11A	7	T		E1	PL15A	7	T	
D1	NC	-			D1	PL11B	7	C		D1	PL15B	7	C	
H3	PL3A	7	T		H3	PL12A	7	T		H3	PL16A	7	T	
G2	PL3B	7	C		G2	PL12B	7	C		G2	PL16B	7	C	
H2	PL4A	7	T		H2	PL13A	7	T		H2	PL17A	7	T	
G1	PL4B	7	C		G1	PL13B	7	C		G1	PL17B	7	C	
J4	PL5A	7	T		J4	PL14A	7	T		J4	PL18A	7	T	
GND	-	-			GND	GND7	7			GND	GND7	7		
J3	PL5B	7	C		J3	PL14B	7	C		J3	PL18B	7	C	
J2	PL6A	7	T	LDQS6	J2	PL15A	7	T	LDQS15	J2	PL19A	7	T	LDQS19
H1	PL6B	7	C		H1	PL15B	7	C		H1	PL19B	7	C	
K4	PL7A	7	T		K4	PL16A	7	T		K4	PL20A	7	T	
K5	PL7B	7	C		K5	PL16B	7	C		K5	PL20B	7	C	
K3	PL8A	7	T		K3	PL17A	7	T		K3	PL21A	7	T	
K2	PL8B	7	C		K2	PL17B	7	C		K2	PL21B	7	C	
J1	PL9A	7	T	PCLKT7_0	J1	PL18A	7	T	PCLKT7_0	J1	PL22A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7			GND	GND7	7		
K1	PL9B	7	C	PCLKC7_0	K1	PL18B	7	C	PCLKC7_0	K1	PL22B	7	C	PCLKC7_0
L3	XRES	6			L3	XRES	6			L3	XRES	6		
L4	PL11A	6	T		L4	PL20A	6	T		L4	PL24A	6	T	
L5	PL11B	6	C		L5	PL20B	6	C		L5	PL24B	6	C	
L2	PL12A	6	T		L2	PL21A	6	T		L2	PL25A	6	T	
L1	PL12B	6	C		L1	PL21B	6	C		L1	PL25B	6	C	

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
V12	PB16B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5	V12	PB24B	5	C	VREF1_5
AB10	PB17A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0	AB10	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5			GND	GND5	5		
AB11	PB17B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0	AB11	PB25B	5	C	PCLKC5_0
Y12	PB18A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN	Y12	PB26A	4	T	WRITEN
U11	PB18B	4	C	CS1N	U11	PB26B	4	C	CS1N	U11	PB26B	4	C	CS1N
W12	PB19A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4	W12	PB27A	4	T	VREF1_4
U12	PB19B	4	C	CSN	U12	PB27B	4	C	CSN	U12	PB27B	4	C	CSN
W13	PB20A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4	W13	PB28A	4	T	VREF2_4
U13	PB20B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7	U13	PB28B	4	C	D0/SPID7
AA12	PB21A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5	AA12	PB29A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB12	PB21B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6	AB12	PB29B	4	C	D1/SPID6
T13	PB22A	4	T	BDQS22	T13	PB30A	4	T	BDQS30	T13	PB30A	4	T	BDQS30
V13	PB22B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4	V13	PB30B	4	C	D3/SPID4
W14	PB23A	4	T		W14	PB31A	4	T		W14	PB31A	4	T	
U14	PB23B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3	U14	PB31B	4	C	D4/SPID3
Y13	PB24A	4	T		Y13	PB32A	4	T		Y13	PB32A	4	T	
V14	PB24B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2	V14	PB32B	4	C	D5/SPID2
AA13	PB25A	4	T		AA13	PB33A	4	T		AA13	PB33A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB13	PB25B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1	AB13	PB33B	4	C	D6/SPID1
AA14	PB26A	4	T		AA14	PB34A	4	T		AA14	PB34A	4	T	
Y14	PB26B	4	C		Y14	PB34B	4	C		Y14	PB34B	4	C	
Y15	PB27A	4	T		Y15	PB35A	4	T		Y15	PB35A	4	T	
W15	PB27B	4	C		W15	PB35B	4	C		W15	PB35B	4	C	
V15	PB28A	4	T		V15	PB36A	4	T		V15	PB36A	4	T	
T14	PB28B	4	C		T14	PB36B	4	C		T14	PB36B	4	C	
AB14	PB29A	4	T		AB14	PB37A	4	T		AB14	PB37A	4	T	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
AB15	PB29B	4	C		AB15	PB37B	4	C		AB15	PB37B	4	C	
AB16	PB30A	4	T	BDQS30	AB16	PB38A	4	T	BDQS38	AB16	PB38A	4	T	BDQS38
AA15	PB30B	4	C		AA15	PB38B	4	C		AA15	PB38B	4	C	
AB17	PB31A	4	T		AB17	PB39A	4	T		AB17	PB39A	4	T	
AA16	PB31B	4	C		AA16	PB39B	4	C		AA16	PB39B	4	C	
AB18	PB32A	4	T		AB18	PB40A	4	T		AB18	PB40A	4	T	
AA17	PB32B	4	C		AA17	PB40B	4	C		AA17	PB40B	4	C	
AB19	PB33A	4	T		AB19	PB41A	4	T		AB19	PB41A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA18	PB33B	4	C		AA18	PB41B	4	C		AA18	PB41B	4	C	
W16	NC	-			W16	NC	-			W16	PB42A	4	T	
U15	NC	-			U15	NC	-			U15	PB42B	4	C	
V16	NC	-			V16	NC	-			V16	PB43A	4	T	
U16	NC	-			U16	NC	-			U16	PB43B	4	C	
Y17	NC	-			Y17	NC	-			Y17	PB44A	4	T	
V17	NC	-			V17	NC	-			V17	PB44B	4	C	
AB20	NC	-			AB20	NC	-			AB20	PB45A	4	T	
GND	-	-			GND	-	-			GND	GND4	4		
AA19	NC	-			AA19	NC	-			AA19	PB45B	4	C	
Y16	NC	-			Y16	NC	-			Y16	PB46A	4	T	BDQS46

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
W17	NC	-			W17	NC	-			W17	PB46B	4	C	
AA20	NC	-			AA20	NC	-			AA20	PB47A	4	T	
Y19	NC	-			Y19	NC	-			Y19	PB47B	4	C	
Y18	NC	-			Y18	NC	-			Y18	PB48A	4	T	
W18	NC	-			W18	NC	-			W18	PB48B	4	C	
T17	NC	-			T17	NC	-			T17	PB49A	4	T	
U17	NC	-			U17	NC	-			U17	PB49B	4	C	
GND	GND4	4			GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3			GND	GND3	3		
W20	PR27B	3	C	VREF2_3	W20	PR36B	3	C	VREF2_3	W20	PR44B	3	C	VREF2_3
Y20	PR27A	3	T	VREF1_3	Y20	PR36A	3	T	VREF1_3	Y20	PR44A	3	T	VREF1_3
AA21	PR26B	3	C		AA21	PR35B	3	C		AA21	PR43B	3	C	
AB21	PR26A	3	T		AB21	PR35A	3	T		AB21	PR43A	3	T	
W19	PR25B	3	C		W19	PR34B	3	C		W19	PR42B	3	C	
V19	PR25A	3	T		V19	PR34A	3	T		V19	PR42A	3	T	
Y21	PR24B	3	C		Y21	PR33B	3	C		Y21	PR41B	3	C	
AA22	PR24A	3	T	RDQS24	AA22	PR33A	3	T	RDQS33	AA22	PR41A	3	T	RDQS41
V20	PR23B	3	C	RLM0_PLLC_FB_A	V20	PR32B	3	C	RLM0_PLLC_FB_A	V20	PR40B	3	C	RLM0_PLLC_FB_A
GND	GND3	3			GND	GND3	3			GND	GND3	3		
U20	PR23A	3	T	RLM0_PLLT_FB_A	U20	PR32A	3	T	RLM0_PLLT_FB_A	U20	PR40A	3	T	RLM0_PLLT_FB_A
W21	PR22B	3	C	RLM0_PLLC_IN_A	W21	PR31B	3	C	RLM0_PLLC_IN_A	W21	PR39B	3	C	RLM0_PLLC_IN_A
Y22	PR22A	3	T	RLM0_PLLT_IN_A	Y22	PR31A	3	T	RLM0_PLLT_IN_A	Y22	PR39A	3	T	RLM0_PLLT_IN_A
V21	PR21B	3	C	DI/CSSPIN	V21	PR30B	3	C	DI/CSSPIN	V21	PR38B	3	C	DI/CSSPIN
W22	PR21A	3	T	DOUT/CSON	W22	PR30A	3	T	DOUT/CSON	W22	PR38A	3	T	DOUT/CSON
U21	PR20B	3	C	BUSY/SISPI	U21	PR29B	3	C	BUSY/SISPI	U21	PR37B	3	C	BUSY/SISPI
V22	PR20A	3	T	D7/SPID0	V22	PR29A	3	T	D7/SPID0	V22	PR37A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3			R20	DONE	3		
T18	NC	-			T18	NC	-			T18	NC	-		
R17	NC	-			R17	NC	-			R17	NC	-		
R19	NC	-			R19	NC	-			R19	NC	-		
R18	NC	-			R18	NC	-			R18	NC	-		
U22	NC	-			U22	NC	-			U22	PR35B	3	C	
GND	-	-			GND	-	-			GND	GND3	3		
T22	NC	-			T22	NC	-			T22	PR35A	3	T	
R21	NC	-			R21	NC	-			R21	PR34B	3	C	
R22	NC	-			R22	NC	-			R22	PR34A	3	T	
P20	NC	-			P20	NC	-			P20	PR33B	3	C	
N20	NC	-			N20	NC	-			N20	PR33A	3	T	
P19	NC	-			P19	NC	-			P19	PR32B	3	C	
P18	NC	-			P18	NC	-			P18	PR32A	3	T	
P21	PR18B	3	C		P21	PR27B	3	C		P21	PR31B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
P22	PR18A	3	T		P22	PR27A	3	T		P22	PR31A	3	T	
N21	PR17B	3	C		N21	PR26B	3	C		N21	PR30B	3	C	

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N22	PR17A	3	T		N22	PR26A	3	T		N22	PR30A	3	T	
N19	PR16B	3	C		N19	PR25B	3	C		N19	PR29B	3	C	
N18	PR16A	3	T		N18	PR25A	3	T		N18	PR29A	3	T	
M21	PR15B	3	C		M21	PR24B	3	C		M21	PR28B	3	C	
L20	PR15A	3	T	RDQS15	L20	PR24A	3	T	RDQS24	L20	PR28A	3	T	RDQS28
L21	PR14B	3	C		L21	PR23B	3	C		L21	PR27B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
M20	PR14A	3	T		M20	PR23A	3	T		M20	PR27A	3	T	
M18	PR13B	3	C		M18	PR22B	3	C		M18	PR26B	3	C	
M19	PR13A	3	T		M19	PR22A	3	T		M19	PR26A	3	T	
M22	PR12B	3	C		M22	PR21B	3	C		M22	PR25B	3	C	
L22	PR12A	3	T		L22	PR21A	3	T		L22	PR25A	3	T	
K22	PR11B	3	C		K22	PR20B	3	C		K22	PR24B	3	C	
K21	PR11A	3	T		K21	PR20A	3	T		K21	PR24A	3	T	
J22	PR9B	2	C	PCLKC2_0	J22	PR18B	2	C	PCLKC2_0	J22	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2			GND	GND2	2		
J21	PR9A	2	T	PCLKT2_0	J21	PR18A	2	T	PCLKT2_0	J21	PR22A	2	T	PCLKT2_0
H22	PR8B	2	C		H22	PR17B	2	C		H22	PR21B	2	C	
H21	PR8A	2	T		H21	PR17A	2	T		H21	PR21A	2	T	
L19	PR7B	2	C		L19	PR16B	2	C		L19	PR20B	2	C	
L18	PR7A	2	T		L18	PR16A	2	T		L18	PR20A	2	T	
K20	PR6B	2	C		K20	PR15B	2	C		K20	PR19B	2	C	
J20	PR6A	2	T	RDQS6	J20	PR15A	2	T	RDQS15	J20	PR19A	2	T	RDQS19
K19	PR5B	2	C		K19	PR14B	2	C		K19	PR18B	2	C	
GND	-	-			GND	GND2	2			GND	GND2	2		
K18	PR5A	2	T		K18	PR14A	2	T		K18	PR18A	2	T	
G22	PR4B	2	C		G22	PR13B	2	C		G22	PR17B	2	C	
F22	PR4A	2	T		F22	PR13A	2	T		F22	PR17A	2	T	
F21	PR3B	2	C		F21	PR12B	2	C		F21	PR16B	2	C	
E22	PR3A	2	T		E22	PR12A	2	T		E22	PR16A	2	T	
E21	NC	-			E21	PR11B	2	C		E21	PR15B	2	C	
D22	NC	-			D22	PR11A	2	T		D22	PR15A	2	T	
G21	NC	-			G21	NC	-			G21	PR14B	2	C	
G20	NC	-			G20	NC	-			GND	GND2	2		
GND	-	-			-	-	-			G20	PR14A	2	T	
J18	NC	-			J18	NC	-			J18	PR13B	2	C	
H19	NC	-			H19	NC	-			H19	PR13A	2	T	
J19	NC	-			J19	NC	-			J19	PR12B	2	C	
H20	NC	-			H20	NC	-			H20	PR12A	2	T	
H17	NC	-			H17	NC	-			H17	PR11B	2	C	
H18	NC	-			H18	NC	-			H18	PR11A	2	T	
D21	NC	-			D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR9B	2	C	RUM0_PLLC_FB_A
GND	-	-			GND	GND2	2			GND	GND2	2		
C22	NC	-			C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR9A	2	T	RUM0_PLLT_FB_A
G19	NC	-			G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR8B	2	C	RUM0_PLLC_IN_A
G18	NC	-			G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR8A	2	T	RUM0_PLLT_IN_A
F20	NC	-			F20	PR7B	2	C		F20	PR7B	2	C	
F19	NC	-			F19	PR7A	2	T		F19	PR7A	2	T	
E20	NC	-			E20	PR6B	2	C		E20	PR6B	2	C	
D20	NC	-			D20	PR6A	2	T	RDQS6	D20	PR6A	2	T	RDQS6

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A4	NC	-			A4	PT9B	0	C		A4	PT9B	0	C	
B4	NC	-			B4	PT9A	0	T		B4	PT9A	0	T	
C4	NC	-			C4	PT8B	0	C		C4	PT8B	0	C	
C5	NC	-			C5	PT8A	0	T		C5	PT8A	0	T	
D6	NC	-			D6	PT7B	0	C		D6	PT7B	0	C	
B5	NC	-			B5	PT7A	0	T		B5	PT7A	0	T	
E6	NC	-			E6	PT6B	0	C		E6	PT6B	0	C	
C6	NC	-			C6	PT6A	0	T	TDQS6	C6	PT6A	0	T	TDQS6
A3	NC	-			A3	PT5B	0	C		A3	PT5B	0	C	
B3	NC	-			B3	PT5A	0	T		B3	PT5A	0	T	
F6	NC	-			F6	PT4B	0	C		F6	PT4B	0	C	
D5	NC	-			D5	PT4A	0	T		D5	PT4A	0	T	
F7	NC	-			F7	PT3B	0	C		F7	PT3B	0	C	
E8	NC	-			E8	PT3A	0	T		E8	PT3A	0	T	
G6	NC	-			G6	PT2B	0	C		G6	PT2B	0	C	
E7	NC	-			E7	PT2A	0	T		E7	PT2A	0	T	
GND	-	-			GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-			A22	GND	-		
AB1	GND	-			AB1	GND	-			AB1	GND	-		
AB22	GND	-			AB22	GND	-			AB22	GND	-		
H15	GND	-			H15	GND	-			H15	GND	-		
H8	GND	-			H8	GND	-			H8	GND	-		
J10	GND	-			J10	GND	-			J10	GND	-		
J11	GND	-			J11	GND	-			J11	GND	-		
J12	GND	-			J12	GND	-			J12	GND	-		
J13	GND	-			J13	GND	-			J13	GND	-		
J14	GND	-			J14	GND	-			J14	GND	-		
J9	GND	-			J9	GND	-			J9	GND	-		
K10	GND	-			K10	GND	-			K10	GND	-		
K11	GND	-			K11	GND	-			K11	GND	-		
K12	GND	-			K12	GND	-			K12	GND	-		
K13	GND	-			K13	GND	-			K13	GND	-		
K14	GND	-			K14	GND	-			K14	GND	-		
K9	GND	-			K9	GND	-			K9	GND	-		
L10	GND	-			L10	GND	-			L10	GND	-		
L11	GND	-			L11	GND	-			L11	GND	-		
L12	GND	-			L12	GND	-			L12	GND	-		
L13	GND	-			L13	GND	-			L13	GND	-		
L14	GND	-			L14	GND	-			L14	GND	-		
L9	GND	-			L9	GND	-			L9	GND	-		
M10	GND	-			M10	GND	-			M10	GND	-		
M11	GND	-			M11	GND	-			M11	GND	-		
M12	GND	-			M12	GND	-			M12	GND	-		
M13	GND	-			M13	GND	-			M13	GND	-		
M14	GND	-			M14	GND	-			M14	GND	-		
M9	GND	-			M9	GND	-			M9	GND	-		
N10	GND	-			N10	GND	-			N10	GND	-		
N11	GND	-			N11	GND	-			N11	GND	-		
N12	GND	-			N12	GND	-			N12	GND	-		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y13	PB40A	4	T		Y13	PB40A	4	T	
V14	PB40B	4	C	D5/SPID2	V14	PB40B	4	C	D5/SPID2
AA13	PB41A	4	T		AA13	PB41A	4	T	
GND	GND4	4			GND	GND4	4		
AB13	PB41B	4	C	D6/SPID1	AB13	PB41B	4	C	D6/SPID1
AA14	PB42A	4	T		AA14	PB42A	4	T	
Y14	PB42B	4	C		Y14	PB42B	4	C	
Y15	PB43A	4	T		Y15	PB43A	4	T	
W15	PB43B	4	C		W15	PB43B	4	C	
V15	PB44A	4	T		V15	PB44A	4	T	
T14	PB44B	4	C		T14	PB44B	4	C	
AB14	PB45A	4	T		AB14	PB45A	4	T	
GND	GND4	4			GND	GND4	4		
AB15	PB45B	4	C		AB15	PB45B	4	C	
AB16	PB46A	4	T	BDQS46	AB16	PB46A	4	T	BDQS46
AA15	PB46B	4	C		AA15	PB46B	4	C	
AB17	PB47A	4	T		AB17	PB47A	4	T	
AA16	PB47B	4	C		AA16	PB47B	4	C	
AB18	PB48A	4	T		AB18	PB48A	4	T	
AA17	PB48B	4	C		AA17	PB48B	4	C	
AB19	PB49A	4	T		AB19	PB49A	4	T	
GND	GND4	4			GND	GND4	4		
AA18	PB49B	4	C		AA18	PB49B	4	C	
W16	PB50A	4	T		W16	PB50A	4	T	
U15	PB50B	4	C		U15	PB50B	4	C	
V16	PB51A	4	T		V16	PB51A	4	T	
U16	PB51B	4	C		U16	PB51B	4	C	
Y17	PB52A	4	T		Y17	PB52A	4	T	
V17	PB52B	4	C		V17	PB52B	4	C	
AB20	PB53A	4	T		AB20	PB53A	4	T	
GND	GND4	4			GND	GND4	4		
AA19	PB53B	4	C		AA19	PB53B	4	C	
Y16	PB54A	4	T	BDQS54	Y16	PB54A	4	T	BDQS54
W17	PB54B	4	C		W17	PB54B	4	C	
AA20	PB55A	4	T		AA20	PB55A	4	T	
Y19	PB55B	4	C		Y19	PB55B	4	C	
Y18	PB56A	4	T		Y18	PB56A	4	T	
W18	PB56B	4	C		W18	PB56B	4	C	
T17	PB57A	4	T		T17	PB57A	4	T	
U17	PB57B	4	C		U17	PB57B	4	C	
GND	-	-			GND	GND4	4		
GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND4	4		
GND	-	-			GND	GND3	3		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
A7	PT27B	0	C		A7	PT27B	0	C	
A6	PT27A	0	T		A6	PT27A	0	T	
B7	PT26B	0	C		B7	PT26B	0	C	
B8	PT26A	0	T		B8	PT26A	0	T	
A5	PT25B	0	C		A5	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
B6	PT25A	0	T		B6	PT25A	0	T	
G10	PT24B	0	C		G10	PT24B	0	C	
E10	PT24A	0	T		E10	PT24A	0	T	
F10	PT23B	0	C		F10	PT23B	0	C	
D10	PT23A	0	T		D10	PT23A	0	T	
G9	PT22B	0	C		G9	PT22B	0	C	
E9	PT22A	0	T	TDQS22	E9	PT22A	0	T	TDQS22
C9	PT21B	0	C		C9	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
C8	PT21A	0	T		C8	PT21A	0	T	
F9	PT20B	0	C		F9	PT20B	0	C	
D9	PT20A	0	T		D9	PT20A	0	T	
F8	PT19B	0	C		F8	PT19B	0	C	
D7	PT19A	0	T		D7	PT19A	0	T	
D8	PT18B	0	C		D8	PT18B	0	C	
C7	PT18A	0	T		C7	PT18A	0	T	
GND	GND0	0			GND	GND0	0		
A4	PT17B	0	C		A4	PT17B	0	C	
B4	PT17A	0	T		B4	PT17A	0	T	
C4	PT16B	0	C		C4	PT16B	0	C	
C5	PT16A	0	T		C5	PT16A	0	T	
D6	PT15B	0	C		D6	PT15B	0	C	
B5	PT15A	0	T		B5	PT15A	0	T	
E6	PT14B	0	C		E6	PT14B	0	C	
C6	PT14A	0	T	TDQS14	C6	PT14A	0	T	TDQS14
A3	PT13B	0	C		A3	PT13B	0	C	
GND	GND0	0			GND	GND0	0		
B3	PT13A	0	T		B3	PT13A	0	T	
F6	PT12B	0	C		F6	PT12B	0	C	
D5	PT12A	0	T		D5	PT12A	0	T	
F7	PT11B	0	C		F7	PT11B	0	C	
E8	PT11A	0	T		E8	PT11A	0	T	
G6	PT10B	0	C		G6	PT10B	0	C	
E7	PT10A	0	T		E7	PT10A	0	T	
GND	GND0	0			GND	GND0	0		
GND	GND0	0			GND	GND0	0		
A1	GND	-			A1	GND	-		
A22	GND	-			A22	GND	-		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
GND	GND7	7			GND	GND7	7		
E3	PL2A	7	T	VREF2_7	E3	PL2A	7	T	VREF2_7
E4	PL2B	7	C	VREF1_7	E4	PL2B	7	C	VREF1_7
E5	NC	-			E5	PL6A	7	T	LDQS6
D5	NC	-			D5	PL6B	7	C	
F4	NC	-			F4	PL7A	7	T	
F5	NC	-			F5	PL7B	7	C	
C3	NC	-			C3	PL8A	7	T	
D3	NC	-			D3	PL8B	7	C	
C2	NC	-			C2	PL9A	7	T	
-	-	-			GND	GND7	7		
B2	NC	-			B2	PL9B	7	C	
B1	PL3A	7	T		B1	PL10A	7	T	
C1	PL3B	7	C		C1	PL10B	7	C	
F3	PL4A	7	T		F3	PL11A	7	T	
G3	PL4B	7	C		G3	PL11B	7	C	
D2	PL5A	7	T		D2	PL12A	7	T	
E2	PL5B	7	C		E2	PL12B	7	C	
-	-	-			GND	GND7	7		
D1	PL6A	7	T	LDQS6	D1	PL14A	7	T	LDQS14
E1	PL6B	7	C		E1	PL14B	7	C	
F2	PL7A	7	T		F2	PL15A	7	T	
G2	PL7B	7	C		G2	PL15B	7	C	
F6	PL8A	7	T	LUM0_PLLT_IN_A	F6	PL16A	7	T	LUM0_PLLT_IN_A
G6	PL8B	7	C	LUM0_PLLC_IN_A	G6	PL16B	7	C	LUM0_PLLC_IN_A
H4	PL9A	7	T	LUM0_PLLT_FB_A	H4	PL17A	7	T	LUM0_PLLT_FB_A
GND	GND7	7			GND	GND7	7		
G4	PL9B	7	C	LUM0_PLLC_FB_A	G4	PL17B	7	C	LUM0_PLLC_FB_A
H6	NC	-			H6	PL19A	7	T	
J7	NC	-			J7	PL19B	7	C	
G5	NC	-			G5	PL20A	7	T	
H5	NC	-			H5	PL20B	7	C	
H3	NC	-			H3	PL21A	7	T	
J3	NC	-			J3	PL21B	7	C	
H2	NC	-			H2	PL22A	7	T	
-	-	-			GND	GND7	7		
J2	NC	-			J2	PL22B	7	C	
J4	PL11A	7	T		J4	PL23A	7	T	LDQS23
J5	PL11B	7	C		J5	PL23B	7	C	
K4	PL12A	7	T		K4	PL24A	7	T	
K5	PL12B	7	C		K5	PL24B	7	C	
J6	PL13A	7	T		J6	PL25A	7	T	

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F484C	360	-3	fpBGA	484	COM	32.8K
LFECP33E-4F484C	360	-4	fpBGA	484	COM	32.8K
LFECP33E-5F484C	360	-5	fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208I	112	-3	PQFP	208	IND	1.5K
LFEC1E-4Q208I	112	-4	PQFP	208	IND	1.5K
LFEC1E-3T144I	97	-3	TQFP	144	IND	1.5K
LFEC1E-4T144I	97	-4	TQFP	144	IND	1.5K
LFEC1E-3T100I	67	-3	TQFP	100	IND	1.5K
LFEC1E-4T100I	67	-4	TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256I	160	-3	fpBGA	256	IND	3.1K
LFEC3E-4F256I	160	-4	fpBGA	256	IND	3.1K
LFEC3E-3Q208I	145	-3	PQFP	208	IND	3.1K
LFEC3E-4Q208I	145	-4	PQFP	208	IND	3.1K
LFEC3E-3T144I	97	-3	TQFP	144	IND	3.1K
LFEC3E-4T144I	97	-4	TQFP	144	IND	3.1K
LFEC3E-3T100I	67	-3	TQFP	100	IND	3.1K
LFEC3E-4T100I	67	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFEC6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFEC6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFEC6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFEC6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFEC6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFEC6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFEC6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFEC10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFEC10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFEC10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFEC10E-3 P208I	147	-3	PQFP	208	IND	10.2K
LFEC10E-4 P208I	147	-4	PQFP	208	IND	10.2K