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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10200
Total RAM Bits	282624
Number of I/O	288
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec10e-3fn484i

Introduction

The LatticeECP/EC family of FPGA devices is optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP™ (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP™ (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC FPGA family. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-4. Slice Diagram

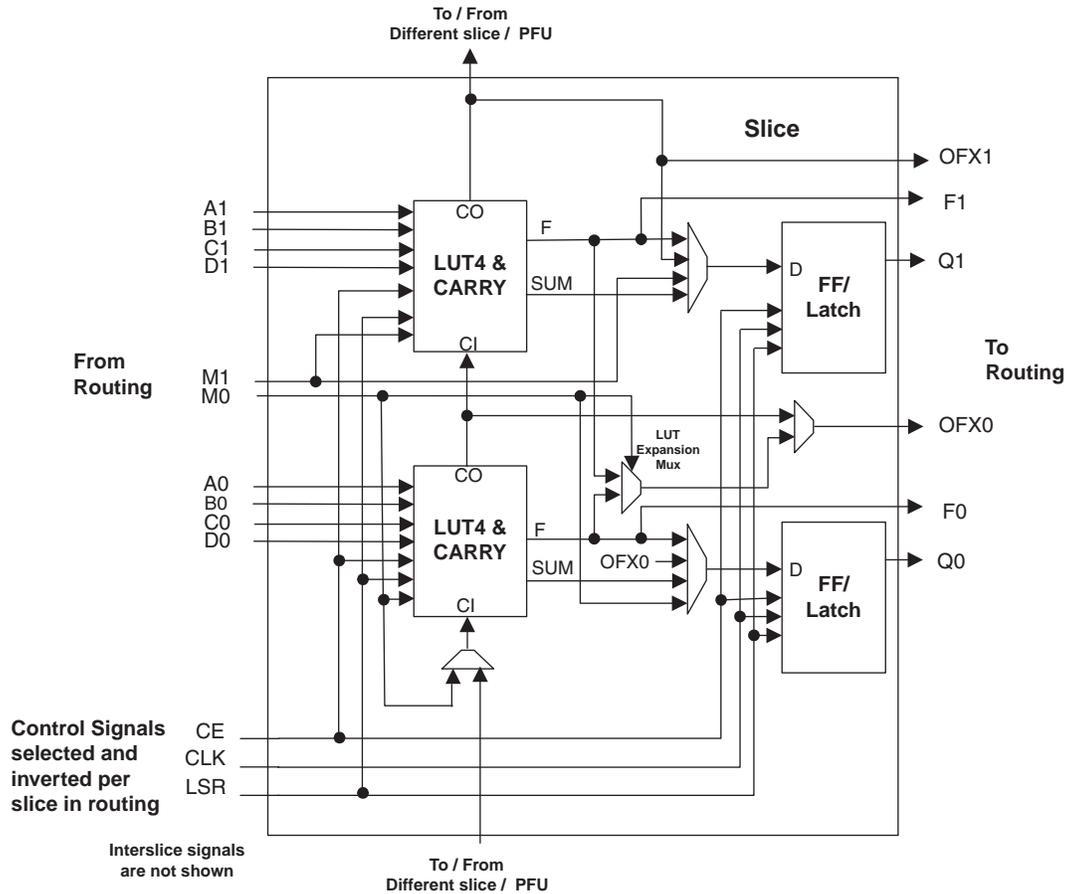


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

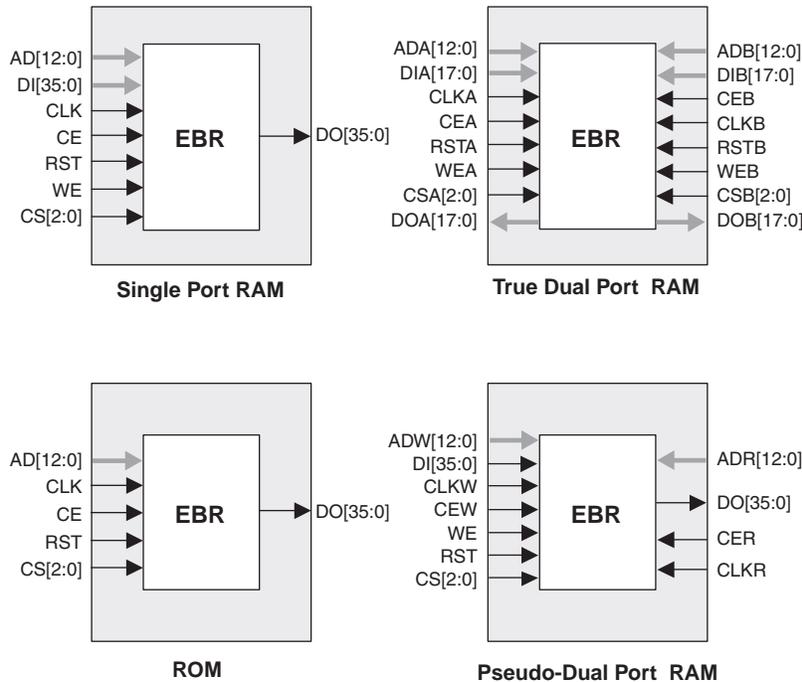
Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-15. sysMEM EBR Primitives



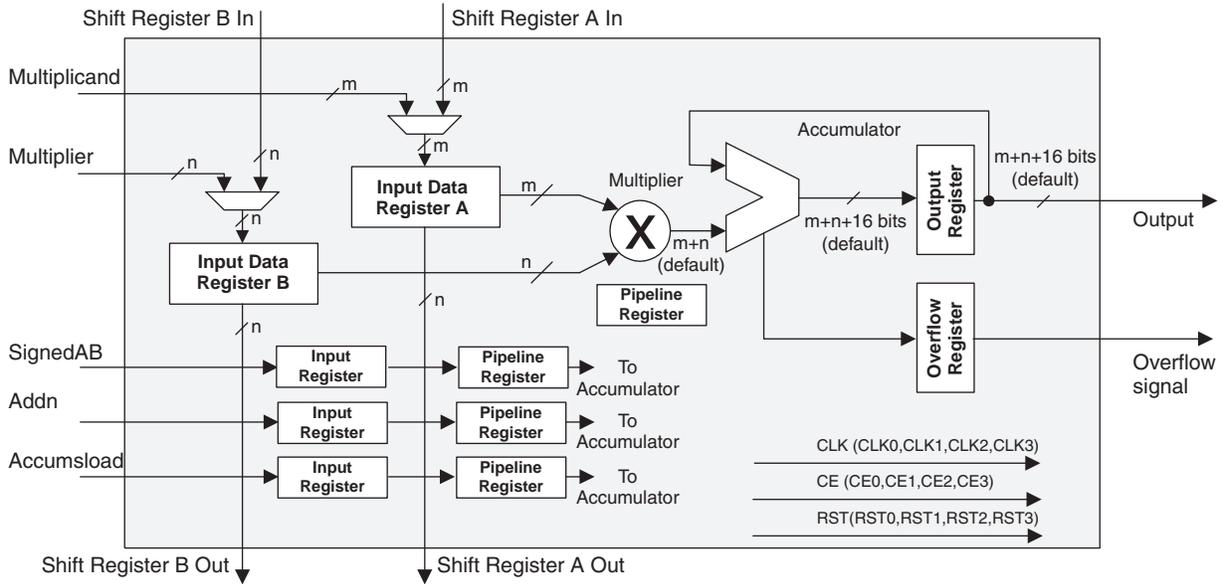
The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

Figure 2-20. MAC sysDSP Element



MULTADD sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-21 shows the MULTADD sysDSP element.

Figure 2-21. MULTADD

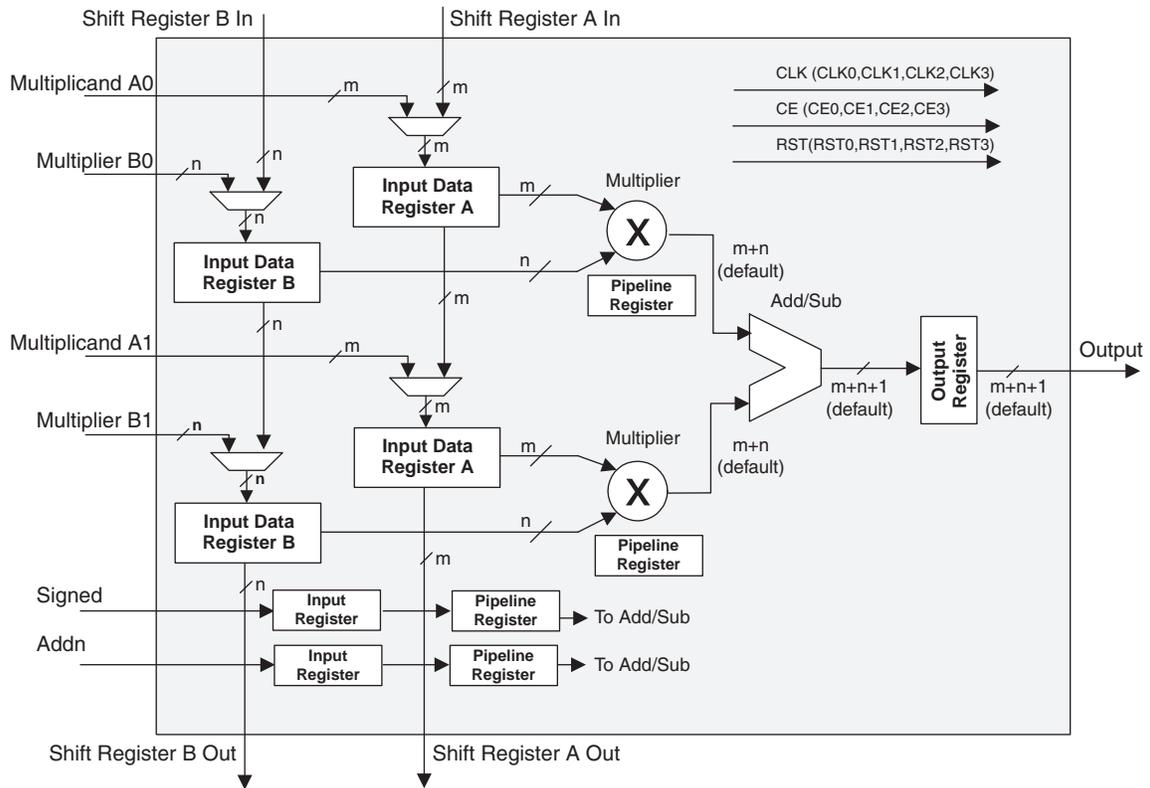


Figure 2-27. Input Register DDR Waveforms

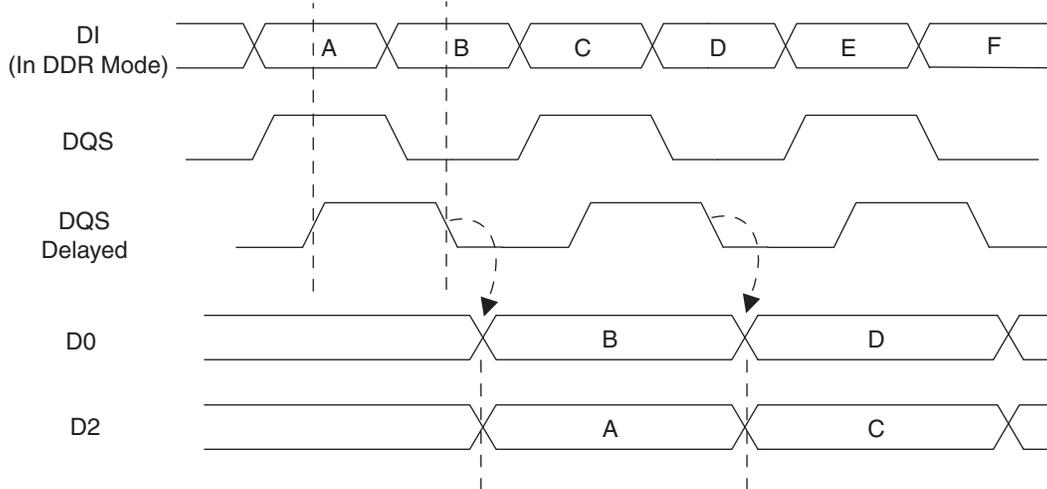
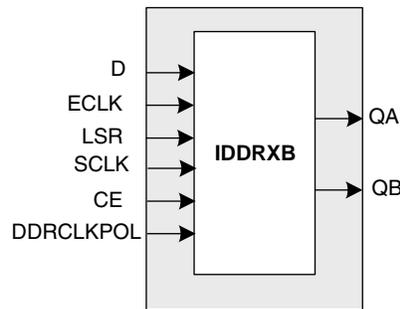


Figure 2-28. INDDRXB Primitive



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-29 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

LatticeECP/EC Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.25	—	0.31	—	0.36	ns
t _{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.40	—	0.48	—	0.56	ns
t _{LSR_PFU}	Set/Reset to Output of PFU	—	0.81	—	0.98	—	1.14	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.05	—	-0.06	—	-0.06	—	ns
t _{SUD_PFU}	Clock to D Input Setup Time	0.12	—	0.14	—	0.16	—	ns
t _{HD_PFU}	Clock to D Input Hold time	-0.03	—	-0.03	—	-0.04	—	ns
t _{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.36	—	0.44	—	0.51	ns
t _{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.48	—	0.58	—	0.68	ns
t _{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.50	—	0.60	—	0.69	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output	—	0.36	—	0.44	—	0.51	ns
t _{SUDATA_PFU}	Data Setup Time	-0.20	—	-0.24	—	-0.28	—	ns
t _{HDATA_PFU}	Data Hold Time	0.26	—	0.31	—	0.36	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.51	—	-0.62	—	-0.72	—	ns
t _{HADDR_PFU}	Address Hold Time	0.64	—	0.77	—	0.90	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.24	—	-0.29	—	-0.34	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.30	—	0.36	—	0.42	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay	—	0.56	—	0.67	—	0.78	ns
t _{OUT_PIO}	Output Buffer Delay	—	1.92	—	2.31	—	2.69	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.90	—	1.08	—	1.26	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.62	—	0.74	—	0.87	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay	—	0.33	—	0.40	—	0.46	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.10	—	-0.12	—	-0.14	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	0.12	—	0.14	—	0.17	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.18	—	0.21	—	0.25	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.15	—	-0.18	—	-0.21	—	ns
EBR Timing								
t _{CO_EBR}	Clock to Output from Address or Data	—	3.64	—	4.37	—	5.10	ns
t _{COO_EBR}	Clock to Output from EBR output Register	—	0.74	—	0.88	—	1.03	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.37	—	0.44	—	0.52	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.29	—	-0.35	—	-0.41	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.37	—	0.45	—	0.52	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.18	—	-0.22	—	-0.26	—	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.23	—	0.28	—	0.33	—	ns

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ

Notes:

1. "n" is a Row/Column PIC number
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.

LFCEP/EC6, LFCEP/EC10 Logic Signal Connections: 208 PQFP

Pin Number	LFCEP6/LFCEC6				LFCEP10/LFCEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			VCC	-		
6	NC	-			GND	-		
7	PL3B	7			PL12B	7		
8	PL4A	7	T		PL13A	7	T	
9	PL4B	7	C		PL13B	7	C	
10	PL5A	7	T		PL14A	7	T	
11	PL5B	7	C		PL14B	7	C	
12	PL6A	7	T	LDQS6	PL15A	7	T	LDQS15
13	VCCIO7	7			VCCIO7	7		
14	PL6B	7	C		PL15B	7	C	
15	PL7A	7	T		PL16A	7	T	
16	PL7B	7	C		PL16B	7	C	
17	PL8A	7	T		PL17A	7	T	
18	GND7	7			GND7	7		
19	PL8B	7	C		PL17B	7	C	
20	PL9A	7	T	PCLKT7_0	PL18A	7	T	PCLKT7_0
21	PL9B	7	C	PCLKC7_0	PL18B	7	C	PCLKC7_0
22	VCCAUX	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	VCC	-			VCC	-		
25	GND	-			GND	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL20A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A
34	PL20B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A
35	PL21A	6	T	LLM0_PLLT_FB_A	PL30A	6	T	LLM0_PLLT_FB_A
36	PL21B	6	C	LLM0_PLLC_FB_A	PL30B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL22A	6	T		PL31A	6	T	
39	PL22B	6	C		PL31B	6	C	
40	PL23A	6	T		PL32A	6	T	
41	GND6	6			GND6	6		
42	PL23B	6	C		PL32B	6	C	

LFEC3 and LFEC6/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFEC6/EC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
K2	PL11A	6	T	LLM0_PLLT_IN_A	PL20A	6	T	LLM0_PLLT_IN_A
K1	PL11B	6	C	LLM0_PLLC_IN_A	PL20B	6	C	LLM0_PLLC_IN_A
L2	PL12A	6	T	LLM0_PLLT_FB_A	PL21A	6	T	LLM0_PLLT_FB_A
L1	PL12B	6	C	LLM0_PLLC_FB_A	PL21B	6	C	LLM0_PLLC_FB_A
M2	PL13A	6	T		PL22A	6	T	
M1	PL13B	6	C		PL22B	6	C	
N1	PL14A	6	T		PL23A	6	T	
GND	GND6	6			GND6	6		
N2	PL14B	6	C		PL23B	6	C	
M4	PL15A	6	T	LDQS15	PL24A	6	T	LDQS24
M3	PL15B	6	C		PL24B	6	C	
P1	PL16A	6	T		PL25A	6	T	
R1	PL16B	6	C		PL25B	6	C	
P2	PL17A	6	T		PL26A	6	T	
P3	PL17B	6	C		PL26B	6	C	
N3	PL18A	6	T	VREF1_6	PL27A	6	T	VREF1_6
N4	PL18B	6	C	VREF2_6	PL27B	6	C	VREF2_6
GND	GND6	6			GND6	6		
GND	GND5	5			GND5	5		
P4	PB2A	5	T		PB2A	5	T	
N5	PB2B	5	C		PB2B	5	C	
P5	PB3A	5	T		PB3A	5	T	
P6	PB3B	5	C		PB3B	5	C	
R4	PB4A	5	T		PB4A	5	T	
R3	PB4B	5	C		PB4B	5	C	
T2	PB5A	5	T		PB5A	5	T	
T3	PB5B	5	C		PB5B	5	C	
R5	PB6A	5	T	BDQS6	PB6A	5	T	BDQS6
R6	PB6B	5	C		PB6B	5	C	
T4	PB7A	5	T		PB7A	5	T	
T5	PB7B	5	C		PB7B	5	C	
N6	PB8A	5	T		PB8A	5	T	
M6	PB8B	5	C		PB8B	5	C	
T6	PB9A	5	T		PB9A	5	T	
GND	GND5	5			GND5	5		
T7	PB9B	5	C		PB9B	5	C	
P7	PB10A	5	T		PB10A	5	T	
N7	PB10B	5	C		PB10B	5	C	
R7	PB11A	5	T		PB11A	5	T	
R8	PB11B	5	C		PB11B	5	C	
M7	PB12A	5	T		PB12A	5	T	
M8	PB12B	5	C		PB12B	5	C	
T8	PB13A	5	T		PB13A	5	T	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
D7	PT11B	0	C		PT11B	0	C	
C7	PT11A	0	T		PT11A	0	T	
A7	PT10B	0	C		PT10B	0	C	
A6	PT10A	0	T		PT10A	0	T	
E7	PT9B	0	C		PT9B	0	C	
GND	GND0	0			GND0	0		
E6	PT9A	0	T		PT9A	0	T	
D6	PT8B	0	C		PT8B	0	C	
C6	PT8A	0	T		PT8A	0	T	
B6	PT7B	0	C		PT7B	0	C	
B5	PT7A	0	T		PT7A	0	T	
A5	PT6B	0	C		PT6B	0	C	
A4	PT6A	0	T	TDQS6	PT6A	0	T	TDQS6
A3	PT5B	0	C		PT5B	0	C	
A2	PT5A	0	T		PT5A	0	T	
B2	PT4B	0	C		PT4B	0	C	
B3	PT4A	0	T		PT4A	0	T	
D5	PT3B	0	C		PT3B	0	C	
C5	PT3A	0	T		PT3A	0	T	
C4	PT2B	0	C		PT2B	0	C	
B4	PT2A	0	T		PT2A	0	T	
GND	GND0	0			GND0	0		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
G10	GND	-			GND	-		
G7	GND	-			GND	-		
G8	GND	-			GND	-		
G9	GND	-			GND	-		
H10	GND	-			GND	-		
H7	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J10	GND	-			GND	-		
J7	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K7	GND	-			GND	-		
K8	GND	-			GND	-		
K9	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
E12	VCC	-			VCC	-		

LFECP/EC10 and LFECP/EC15 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFECP10/LFEC10				LFECP15/LFEC15			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
N7	PB18B	5	C		PB18B	5	C	
R7	PB19A	5	T		PB19A	5	T	
R8	PB19B	5	C		PB19B	5	C	
M7	PB20A	5	T		PB20A	5	T	
M8	PB20B	5	C		PB20B	5	C	
T8	PB21A	5	T		PB21A	5	T	
GND	GND5	5			GND5	5		
T9	PB21B	5	C		PB21B	5	C	
P8	PB22A	5	T	BDQS22	PB22A	5	T	BDQS22
N8	PB22B	5	C		PB22B	5	C	
R9	PB23A	5	T		PB23A	5	T	
R10	PB23B	5	C		PB23B	5	C	
P9	PB24A	5	T	VREF2_5	PB24A	5	T	VREF2_5
N9	PB24B	5	C	VREF1_5	PB24B	5	C	VREF1_5
T10	PB25A	5	T	PCLKT5_0	PB25A	5	T	PCLKT5_0
GND	GND5	5			GND5	5		
T11	PB25B	5	C	PCLKC5_0	PB25B	5	C	PCLKC5_0
T12	PB26A	4	T	WRITEN	PB26A	4	T	WRITEN
T13	PB26B	4	C	CS1N	PB26B	4	C	CS1N
P10	PB27A	4	T	VREF1_4	PB27A	4	T	VREF1_4
N10	PB27B	4	C	CSN	PB27B	4	C	CSN
T14	PB28A	4	T	VREF2_4	PB28A	4	T	VREF2_4
T15	PB28B	4	C	D0/SPID7	PB28B	4	C	D0/SPID7
M10	PB29A	4	T	D2/SPID5	PB29A	4	T	D2/SPID5
GND	GND4	4			GND4	4		
M11	PB29B	4	C	D1/SPID6	PB29B	4	C	D1/SPID6
R11	PB30A	4	T	BDQS30	PB30A	4	T	BDQS30
P11	PB30B	4	C	D3/SPID4	PB30B	4	C	D3/SPID4
R13	PB31A	4	T		PB31A	4	T	
R14	PB31B	4	C	D4/SPID3	PB31B	4	C	D4/SPID3
P12	PB32A	4	T		PB32A	4	T	
P13	PB32B	4	C	D5/SPID2	PB32B	4	C	D5/SPID2
N11	PB33A	4	T		PB33A	4	T	
GND	GND4	4			GND4	4		
N12	PB33B	4	C	D6/SPID1	PB33B	4	C	D6/SPID1
R12	PB34A	4			PB34A	4		
GND	GND4	4			GND4	4		
GND	GND4	4			GND4	4		
-	-	-			GND4	4		
-	-	-			GND4	4		
GND	GND3	3			GND3	3		
N13	PR36B	3	C	VREF2_3	PR44B	3	C	VREF2_3
N14	PR36A	3	T	VREF1_3	PR44A	3	T	VREF1_3

**LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections:
 484 fpBGA (Cont.)**

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/EC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N13	GND	-			N13	GND	-			N13	GND	-		
N14	GND	-			N14	GND	-			N14	GND	-		
N9	GND	-			N9	GND	-			N9	GND	-		
P10	GND	-			P10	GND	-			P10	GND	-		
P11	GND	-			P11	GND	-			P11	GND	-		
P12	GND	-			P12	GND	-			P12	GND	-		
P13	GND	-			P13	GND	-			P13	GND	-		
P14	GND	-			P14	GND	-			P14	GND	-		
P9	GND	-			P9	GND	-			P9	GND	-		
R15	GND	-			R15	GND	-			R15	GND	-		
R8	GND	-			R8	GND	-			R8	GND	-		
J16	VCC	-			J16	VCC	-			J16	VCC	-		
J7	VCC	-			J7	VCC	-			J7	VCC	-		
K16	VCC	-			K16	VCC	-			K16	VCC	-		
K17	VCC	-			K17	VCC	-			K17	VCC	-		
K6	VCC	-			K6	VCC	-			K6	VCC	-		
K7	VCC	-			K7	VCC	-			K7	VCC	-		
L17	VCC	-			L17	VCC	-			L17	VCC	-		
L6	VCC	-			L6	VCC	-			L6	VCC	-		
M17	VCC	-			M17	VCC	-			M17	VCC	-		
M6	VCC	-			M6	VCC	-			M6	VCC	-		
N16	VCC	-			N16	VCC	-			N16	VCC	-		
N17	VCC	-			N17	VCC	-			N17	VCC	-		
N6	VCC	-			N6	VCC	-			N6	VCC	-		
N7	VCC	-			N7	VCC	-			N7	VCC	-		
P16	VCC	-			P16	VCC	-			P16	VCC	-		
P7	VCC	-			P7	VCC	-			P7	VCC	-		
G11	VCCIO0	0			G11	VCCIO0	0			G11	VCCIO0	0		
H10	VCCIO0	0			H10	VCCIO0	0			H10	VCCIO0	0		
H11	VCCIO0	0			H11	VCCIO0	0			H11	VCCIO0	0		
H9	VCCIO0	0			H9	VCCIO0	0			H9	VCCIO0	0		
G12	VCCIO1	1			G12	VCCIO1	1			G12	VCCIO1	1		
H12	VCCIO1	1			H12	VCCIO1	1			H12	VCCIO1	1		
H13	VCCIO1	1			H13	VCCIO1	1			H13	VCCIO1	1		
H14	VCCIO1	1			H14	VCCIO1	1			H14	VCCIO1	1		
J15	VCCIO2	2			J15	VCCIO2	2			J15	VCCIO2	2		
K15	VCCIO2	2			K15	VCCIO2	2			K15	VCCIO2	2		
L15	VCCIO2	2			L15	VCCIO2	2			L15	VCCIO2	2		
L16	VCCIO2	2			L16	VCCIO2	2			L16	VCCIO2	2		
M15	VCCIO3	3			M15	VCCIO3	3			M15	VCCIO3	3		
M16	VCCIO3	3			M16	VCCIO3	3			M16	VCCIO3	3		
N15	VCCIO3	3			N15	VCCIO3	3			N15	VCCIO3	3		
P15	VCCIO3	3			P15	VCCIO3	3			P15	VCCIO3	3		
R12	VCCIO4	4			R12	VCCIO4	4			R12	VCCIO4	4		
R13	VCCIO4	4			R13	VCCIO4	4			R13	VCCIO4	4		
R14	VCCIO4	4			R14	VCCIO4	4			R14	VCCIO4	4		
T12	VCCIO4	4			T12	VCCIO4	4			T12	VCCIO4	4		
R10	VCCIO5	5			R10	VCCIO5	5			R10	VCCIO5	5		
R11	VCCIO5	5			R11	VCCIO5	5			R11	VCCIO5	5		
R9	VCCIO5	5			R9	VCCIO5	5			R9	VCCIO5	5		

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
K3	PL21A	7	T		K3	PL33A	7	T	
K2	PL21B	7	C		K2	PL33B	7	C	
J1	PL22A	7	T	PCLKT7_0	J1	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
K1	PL22B	7	C	PCLKC7_0	K1	PL34B	7	C	PCLKC7_0
L3	XRES	6			L3	XRES	6		
L4	PL24A	6	T		L4	PL36A	6	T	
L5	PL24B	6	C		L5	PL36B	6	C	
L2	PL25A	6	T		L2	PL37A	6	T	
L1	PL25B	6	C		L1	PL37B	6	C	
M4	PL26A	6	T		M4	PL38A	6	T	
M5	PL26B	6	C		M5	PL38B	6	C	
M1	PL27A	6	T		M1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
M2	PL27B	6	C		M2	PL39B	6	C	
N3	PL28A	6	T	LDQS28	N3	PL40A	6	T	LDQS40
M3	PL28B	6	C		M3	PL40B	6	C	
N5	PL29A	6	T		N5	PL41A	6	T	
N4	PL29B	6	C		N4	PL41B	6	C	
N1	PL30A	6	T		N1	PL42A	6	T	
N2	PL30B	6	C		N2	PL42B	6	C	
P1	PL31A	6	T		P1	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
P2	PL31B	6	C		P2	PL43B	6	C	
R6	PL32A	6	T		R6	PL44A	6	T	
P5	PL32B	6	C		P5	PL44B	6	C	
P3	PL33A	6	T		P3	PL45A	6	T	
P4	PL33B	6	C		P4	PL45B	6	C	
R1	PL34A	6	T		R1	PL46A	6	T	
R2	PL34B	6	C		R2	PL46B	6	C	
R5	PL35A	6	T		R5	PL47A	6	T	
GND	GND6	6			GND	GND6	6		
R4	PL35B	6	C		R4	PL47B	6	C	
T1	PL36A	6	T	LDQS36	T1	PL48A	6	T	LDQS48
T2	PL36B	6	C		T2	PL48B	6	C	
R3	PL37A	6	T		R3	PL49A	6	T	
T3	PL37B	6	C		T3	PL49B	6	C	
GND	GND6	6			GND	GND6	6		
T5	TCK	6			T5	TCK	6		
U5	TDI	6			U5	TDI	6		
T4	TMS	6			T4	TMS	6		
U1	TDO	6			U1	TDO	6		
U2	VCCJ	6			U2	VCCJ	6		
V1	PL41A	6	T	LLM0_PLLT_IN_A	V1	PL53A	6	T	LLM0_PLLT_IN_A

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVD S	Dual Function	Ball Number	Ball Function	Bank	LVD S	Dual Function
W20	PR48B	3	C	VREF2_3	W20	PR68B	3	C	VREF2_3
Y20	PR48A	3	T	VREF1_3	Y20	PR68A	3	T	VREF1_3
GND	-	-			GND	GND3	3		
GND	-	-			GND	GND3	3		
AA21	PR47B	3	C		AA21	PR59B	3	C	
AB21	PR47A	3	T		AB21	PR59A	3	T	
W19	PR46B	3	C		W19	PR58B	3	C	
V19	PR46A	3	T		V19	PR58A	3	T	
Y21	PR45B	3	C		Y21	PR57B	3	C	
AA22	PR45A	3	T	RDQS45	AA22	PR57A	3	T	RDQS57
V20	PR44B	3	C	RLM0_PLLC_IN_A	V20	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
U20	PR44A	3	T	RLM0_PLLT_IN_A	U20	PR56A	3	T	RLM0_PLLT_IN_A
W21	PR43B	3	C	RLM0_PLLC_FB_A	W21	PR55B	3	C	RLM0_PLLC_FB_A
Y22	PR43A	3	T	RLM0_PLLT_FB_A	Y22	PR55A	3	T	RLM0_PLLT_FB_A
V21	PR42B	3	C	DI/CSSPIN	V21	PR54B	3	C	DI/CSSPIN
W22	PR42A	3	T	DOUT/CSON	W22	PR54A	3	T	DOUT/CSON
U21	PR41B	3	C	BUSY/SISPI	U21	PR53B	3	C	BUSY/SISPI
V22	PR41A	3	T	D7/SPID0	V22	PR53A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3		
GND	GND3	3			GND	GND3	3		
T18	PR37B	3	C		T18	PR49B	3	C	
R17	PR37A	3	T		R17	PR49A	3	T	
R19	PR36B	3	C		R19	PR48B	3	C	
R18	PR36A	3	T	RDQS36	R18	PR48A	3	T	RDQS48
U22	PR35B	3	C		U22	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T22	PR35A	3	T		T22	PR47A	3	T	
R21	PR34B	3	C		R21	PR46B	3	C	
R22	PR34A	3	T		R22	PR46A	3	T	
P20	PR33B	3	C		P20	PR45B	3	C	
N20	PR33A	3	T		N20	PR45A	3	T	
P19	PR32B	3	C		P19	PR44B	3	C	
P18	PR32A	3	T		P18	PR44A	3	T	
P21	PR31B	3	C		P21	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P22	PR31A	3	T		P22	PR43A	3	T	
N21	PR30B	3	C		N21	PR42B	3	C	

LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
K6	PL13B	7	C		K6	PL25B	7	C	
F1	PL14A	7	T		F1	PL26A	7	T	
GND	GND7	7			GND	GND7	7		
G1	PL14B	7	C		G1	PL26B	7	C	
H1	PL15A	7	T		H1	PL27A	7	T	
J1	PL15B	7	C		J1	PL27B	7	C	
K2	PL16A	7	T		K2	PL28A	7	T	
K1	PL16B	7	C		K1	PL28B	7	C	
K3	PL17A	7	T		K3	PL29A	7	T	
L3	PL17B	7	C		L3	PL29B	7	C	
L2	PL18A	7	T		L2	PL30A	7	T	
GND	GND7	7			GND	GND7	7		
L1	PL18B	7	C		L1	PL30B	7	C	
M3	PL19A	7	T	LDQS19	M3	PL31A	7	T	LDQS31
M4	PL19B	7	C		M4	PL31B	7	C	
M1	PL20A	7	T		M1	PL32A	7	T	
M2	PL20B	7	C		M2	PL32B	7	C	
L4	PL21A	7	T		L4	PL33A	7	T	
L5	PL21B	7	C		L5	PL33B	7	C	
N2	PL22A	7	T	PCLKT7_0	N2	PL34A	7	T	PCLKT7_0
GND	GND7	7			GND	GND7	7		
N1	PL22B	7	C	PCLKC7_0	N1	PL34B	7	C	PCLKC7_0
N3	XRES	6			N3	XRES	6		
P1	PL24A	6	T		P1	PL36A	6	T	
P2	PL24B	6	C		P2	PL36B	6	C	
L7	PL25A	6	T		L7	PL37A	6	T	
L6	PL25B	6	C		L6	PL37B	6	C	
N4	PL26A	6	T		N4	PL38A	6	T	
N5	PL26B	6	C		N5	PL38B	6	C	
R1	PL27A	6	T		R1	PL39A	6	T	
GND	GND6	6			GND	GND6	6		
R2	PL27B	6	C		R2	PL39B	6	C	
P4	PL28A	6	T	LDQS28	P4	PL40A	6	T	LDQS40
P3	PL28B	6	C		P3	PL40B	6	C	
M5	PL29A	6	T		M5	PL41A	6	T	
M6	PL29B	6	C		M6	PL41B	6	C	
T1	PL30A	6	T		T1	PL42A	6	T	
T2	PL30B	6	C		T2	PL42B	6	C	
R4	PL31A	6	T		R4	PL43A	6	T	
GND	GND6	6			GND	GND6	6		
R3	PL31B	6	C		R3	PL43B	6	C	
N6	PL32A	6	T		N6	PL44A	6	T	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AF22	PB51A	4	T		AF22	PB51A	4	T	
AB17	PB51B	4	C		AB17	PB51B	4	C	
AE22	PB52A	4	T		AE22	PB52A	4	T	
AA18	PB52B	4	C		AA18	PB52B	4	C	
AE19	PB53A	4	T		AE19	PB53A	4	T	
GND	GND4	4			GND	GND4	4		
AE20	PB53B	4	C		AE20	PB53B	4	C	
AA19	PB54A	4	T	BDQS54	AA19	PB54A	4	T	BDQS54
Y18	PB54B	4	C		Y18	PB54B	4	C	
AF23	PB55A	4	T		AF23	PB55A	4	T	
AA20	PB55B	4	C		AA20	PB55B	4	C	
AC18	PB56A	4	T		AC18	PB56A	4	T	
AB18	PB56B	4	C		AB18	PB56B	4	C	
AF24	PB57A	4	T		AF24	PB57A	4	T	
-	-	-			GND	GND4	4		
AE23	PB57B	4	C		AE23	PB57B	4	C	
AD19	NC	-			AD19	PB58A	4	T	
AD20	NC	-			AD20	PB58B	4	C	
AC19	NC	-			AC19	PB59A	4	T	
AB19	NC	-			AB19	PB59B	4	C	
AD21	NC	-			AD21	PB60A	4	T	
AC20	NC	-			AC20	PB60B	4	C	
AF25	NC	-			AF25	PB61A	4	T	
-	-	-			GND	GND4	4		
AE25	NC	-			AE25	PB61B	4	C	
AB21	NC	-			AB21	PB62A	4	T	BDQS62
AB20	NC	-			AB20	PB62B	4	C	
AE24	NC	-			AE24	PB63A	4	T	
AD23	NC	-			AD23	PB63B	4	C	
AD22	NC	-			AD22	PB64A	4	T	
AC21	NC	-			AC21	PB64B	4	C	
AC22	NC	-			AC22	PB65A	4	T	
AB22	NC	-			AB22	PB65B	4	C	
GND	GND4	4			GND	GND4	4		
GND	GND3	3			GND	GND3	3		
AC23	PR48B	3	C	VREF2_3	AC23	PR68B	3	C	VREF2_3
AC24	PR48A	3	T	VREF1_3	AC24	PR68A	3	T	VREF1_3
AD24	NC	-			AD24	PR67B	3	C	
AD25	NC	-			AD25	PR67A	3	T	
AE26	NC	-			AE26	PR66B	3	C	
AD26	NC	-			AD26	PR66A	3	T	
Y20	NC	-			Y20	PR65B	3	C	

LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y19	NC	-			Y19	PR65A	3	T	RDQS65
AA23	NC	-			AA23	PR64B	3	C	
-	-	-			GND	GND3	3		
AA22	NC	-			AA22	PR64A	3	T	
AB23	NC	-			AB23	PR63B	3	C	
AB24	NC	-			AB24	PR63A	3	T	
Y21	NC	-			Y21	PR62B	3	C	
AA21	NC	-			AA21	PR62A	3	T	
Y23	NC	-			Y23	PR61B	3	C	
Y22	NC	-			Y22	PR61A	3	T	
AA24	NC	-			AA24	PR60B	3	C	
-	-	-			GND	GND3	3		
Y24	NC	-			Y24	PR60A	3	T	
AC25	PR47B	3	C		AC25	PR59B	3	C	
AC26	PR47A	3	T		AC26	PR59A	3	T	
AB25	PR46B	3	C		AB25	PR58B	3	C	
AA25	PR46A	3	T		AA25	PR58A	3	T	
AB26	PR45B	3	C		AB26	PR57B	3	C	
AA26	PR45A	3	T	RDQS45	AA26	PR57A	3	T	RDQS57
W23	PR44B	3	C	RLM0_PLLC_IN_A	W23	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
W24	PR44A	3	T	RLM0_PLLT_IN_A	W24	PR56A	3	T	RLM0_PLLT_IN_A
W22	PR43B	3	C	RLM0_PLLC_FB_A	W22	PR55B	3	C	RLM0_PLLC_FB_A
W21	PR43A	3	T	RLM0_PLLT_FB_A	W21	PR55A	3	T	RLM0_PLLT_FB_A
Y25	PR42B	3	C	DI/CSSPIN	Y25	PR54B	3	C	DI/CSSPIN
Y26	PR42A	3	T	DOUT/CSON	Y26	PR54A	3	T	DOUT/CSON
W25	PR41B	3	C	BUSY/SISPI	W25	PR53B	3	C	BUSY/SISPI
W26	PR41A	3	T	D7/SPID0	W26	PR53A	3	T	D7/SPID0
V24	CFG2	3			V24	CFG2	3		
V21	CFG1	3			V21	CFG1	3		
V23	CFG0	3			V23	CFG0	3		
V22	PROGRAMN	3			V22	PROGRAMN	3		
V20	CCLK	3			V20	CCLK	3		
V25	INITN	3			V25	INITN	3		
U20	DONE	3			U20	DONE	3		
V26	PR39B	3	C		V26	PR51B	3	C	
GND	GND3	3			GND	GND3	3		
U26	PR39A	3	T		U26	PR51A	3	T	
U24	PR38B	3	C		U24	PR50B	3	C	
U25	PR38A	3	T		U25	PR50A	3	T	
U23	PR37B	3	C		U23	PR49B	3	C	
U22	PR37A	3	T		U22	PR49A	3	T	

LFCEP/EC20, LFCEP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFCEP/EC20					LFCEP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
D13	PT32B	0	C	VREF1_0	D13	PT32B	0	C	VREF1_0
C13	PT32A	0	T	VREF2_0	C13	PT32A	0	T	VREF2_0
A13	PT31B	0	C		A13	PT31B	0	C	
B13	PT31A	0	T		B13	PT31A	0	T	
F13	PT30B	0	C		F13	PT30B	0	C	
F12	PT30A	0	T	TDQS30	F12	PT30A	0	T	TDQS30
A12	PT29B	0	C		A12	PT29B	0	C	
GND	GND0	0			GND	GND0	0		
B12	PT29A	0	T		B12	PT29A	0	T	
A11	PT28B	0	C		A11	PT28B	0	C	
B11	PT28A	0	T		B11	PT28A	0	T	
D12	PT27B	0	C		D12	PT27B	0	C	
C12	PT27A	0	T		C12	PT27A	0	T	
B10	PT26B	0	C		B10	PT26B	0	C	
A10	PT26A	0	T		A10	PT26A	0	T	
G12	PT25B	0	C		G12	PT25B	0	C	
GND	GND0	0			GND	GND0	0		
A9	PT25A	0	T		A9	PT25A	0	T	
E12	PT24B	0	C		E12	PT24B	0	C	
B9	PT24A	0	T		B9	PT24A	0	T	
F11	PT23B	0	C		F11	PT23B	0	C	
A8	PT23A	0	T		A8	PT23A	0	T	
D11	PT22B	0	C		D11	PT22B	0	C	
C11	PT22A	0	T	TDQS22	C11	PT22A	0	T	TDQS22
B8	PT21B	0	C		B8	PT21B	0	C	
GND	GND0	0			GND	GND0	0		
B7	PT21A	0	T		B7	PT21A	0	T	
E11	PT20B	0	C		E11	PT20B	0	C	
A7	PT20A	0	T		A7	PT20A	0	T	
G11	PT19B	0	C		G11	PT19B	0	C	
C7	PT19A	0	T		C7	PT19A	0	T	
G10	PT18B	0	C		G10	PT18B	0	C	
C6	PT18A	0	T		C6	PT18A	0	T	
C10	PT17B	0	C		C10	PT17B	0	C	
GND	GND0	0			GND	GND0	0		
D10	PT17A	0	T		D10	PT17A	0	T	
F10	PT16B	0	C		F10	PT16B	0	C	
A6	PT16A	0	T		A6	PT16A	0	T	
E10	PT15B	0	C		E10	PT15B	0	C	
C9	PT15A	0	T		C9	PT15A	0	T	
G9	PT14B	0	C		G9	PT14B	0	C	
D9	PT14A	0	T	TDQS14	D9	PT14A	0	T	TDQS14

LatticeECP Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP6E-3F484C	224	-3	fpBGA	484	COM	6.1K
LFCEP6E-4F484C	224	-4	fpBGA	484	COM	6.1K
LFCEP6E-5F484C	224	-5	fpBGA	484	COM	6.1K
LFCEP6E-3F256C	195	-3	fpBGA	256	COM	6.1K
LFCEP6E-4F256C	195	-4	fpBGA	256	COM	6.1K
LFCEP6E-5F256C	195	-5	fpBGA	256	COM	6.1K
LFCEP6E-3Q208C	147	-3	PQFP	208	COM	6.1K
LFCEP6E-4Q208C	147	-4	PQFP	208	COM	6.1K
LFCEP6E-5Q208C	147	-5	PQFP	208	COM	6.1K
LFCEP6E-3T144C	97	-3	TQFP	144	COM	6.1K
LFCEP6E-4T144C	97	-4	TQFP	144	COM	6.1K
LFCEP6E-5T144C	97	-5	TQFP	144	COM	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP10E-3F484C	288	-3	fpBGA	484	COM	10.2K
LFCEP10E-4F484C	288	-4	fpBGA	484	COM	10.2K
LFCEP10E-5F484C	288	-5	fpBGA	484	COM	10.2K
LFCEP10E-3F256C	195	-3	fpBGA	256	COM	10.2K
LFCEP10E-4F256C	195	-4	fpBGA	256	COM	10.2K
LFCEP10E-5F256C	195	-5	fpBGA	256	COM	10.2K
LFCEP10E-3Q208C	147	-3	PQFP	208	COM	10.2K
LFCEP10E-4Q208C	147	-4	PQFP	208	COM	10.2K
LFCEP10E-5Q208C	147	-5	PQFP	208	COM	10.2K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP15E-3F484C	352	-3	fpBGA	484	COM	15.3K
LFCEP15E-4F484C	352	-4	fpBGA	484	COM	15.3K
LFCEP15E-5F484C	352	-5	fpBGA	484	COM	15.3K
LFCEP15E-3F256C	195	-3	fpBGA	256	COM	15.3K
LFCEP15E-4F256C	195	-4	fpBGA	256	COM	15.3K
LFCEP15E-5F256C	195	-5	fpBGA	256	COM	15.3K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP20E-3F672C	400	-3	fpBGA	672	COM	19.7K
LFCEP20E-4F672C	400	-4	fpBGA	672	COM	19.7K
LFCEP20E-5F672C	400	-5	fpBGA	672	COM	19.7K
LFCEP20E-3F484C	360	-3	fpBGA	484	COM	19.7K
LFCEP20E-4F484C	360	-4	fpBGA	484	COM	19.7K
LFCEP20E-5F484C	360	-5	fpBGA	484	COM	19.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFCEP33E-3F672C	496	-3	fpBGA	672	COM	32.8K
LFCEP33E-4F672C	496	-4	fpBGA	672	COM	32.8K
LFCEP33E-5F672C	496	-5	fpBGA	672	COM	32.8K

LatticeECP Commercial (Continued)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFECP33E-3F484C	360	-3	fpBGA	484	COM	32.8K
LFECP33E-4F484C	360	-4	fpBGA	484	COM	32.8K
LFECP33E-5F484C	360	-5	fpBGA	484	COM	32.8K

LatticeEC Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC1E-3Q208I	112	-3	PQFP	208	IND	1.5K
LFEC1E-4Q208I	112	-4	PQFP	208	IND	1.5K
LFEC1E-3T144I	97	-3	TQFP	144	IND	1.5K
LFEC1E-4T144I	97	-4	TQFP	144	IND	1.5K
LFEC1E-3T100I	67	-3	TQFP	100	IND	1.5K
LFEC1E-4T100I	67	-4	TQFP	100	IND	1.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC3E-3F256I	160	-3	fpBGA	256	IND	3.1K
LFEC3E-4F256I	160	-4	fpBGA	256	IND	3.1K
LFEC3E-3Q208I	145	-3	PQFP	208	IND	3.1K
LFEC3E-4Q208I	145	-4	PQFP	208	IND	3.1K
LFEC3E-3T144I	97	-3	TQFP	144	IND	3.1K
LFEC3E-4T144I	97	-4	TQFP	144	IND	3.1K
LFEC3E-3T100I	67	-3	TQFP	100	IND	3.1K
LFEC3E-4T100I	67	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC6E-3F484I	224	-3	fpBGA	484	IND	6.1K
LFEC6E-4F484I	224	-4	fpBGA	484	IND	6.1K
LFEC6E-3F256I	195	-3	fpBGA	256	IND	6.1K
LFEC6E-4F256I	195	-4	fpBGA	256	IND	6.1K
LFEC6E-3Q208I	147	-3	PQFP	208	IND	6.1K
LFEC6E-4Q208I	147	-4	PQFP	208	IND	6.1K
LFEC6E-3T144I	97	-3	TQFP	144	IND	6.1K
LFEC6E-4T144I	97	-4	TQFP	144	IND	6.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFEC10E-3F484I	288	-3	fpBGA	484	IND	10.2K
LFEC10E-4F484I	288	-4	fpBGA	484	IND	10.2K
LFEC10E-3F256I	195	-3	fpBGA	256	IND	10.2K
LFEC10E-4F256I	195	-4	fpBGA	256	IND	10.2K
LFEC10E-3 P208I	147	-3	PQFP	208	IND	10.2K
LFEC10E-4 P208I	147	-4	PQFP	208	IND	10.2K