Lattice Semiconductor Corporation - LFEC10E-4FN256I Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10200
Total RAM Bits	282624
Number of I/O	195
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfec10e-4fn256i

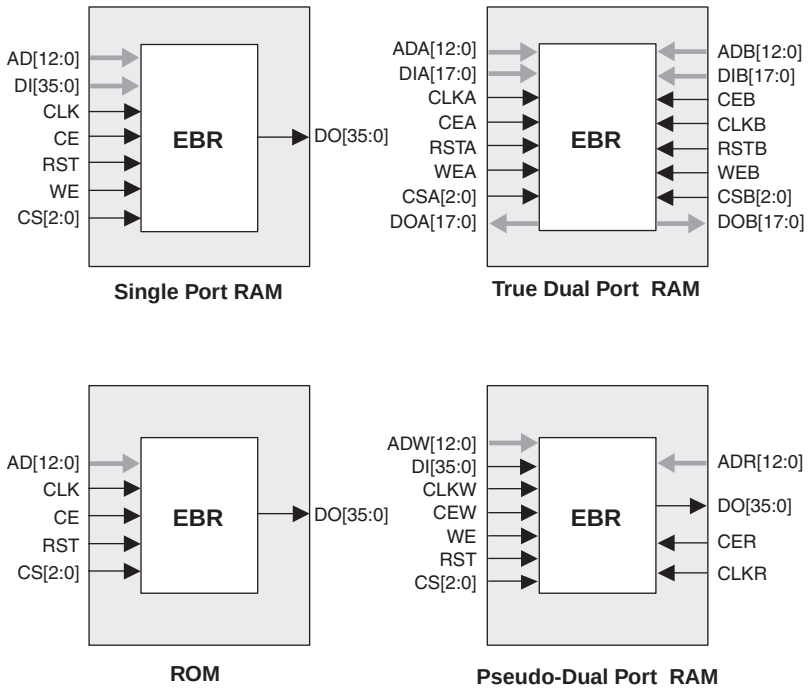
Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-15. sysMEM EBR Primitives



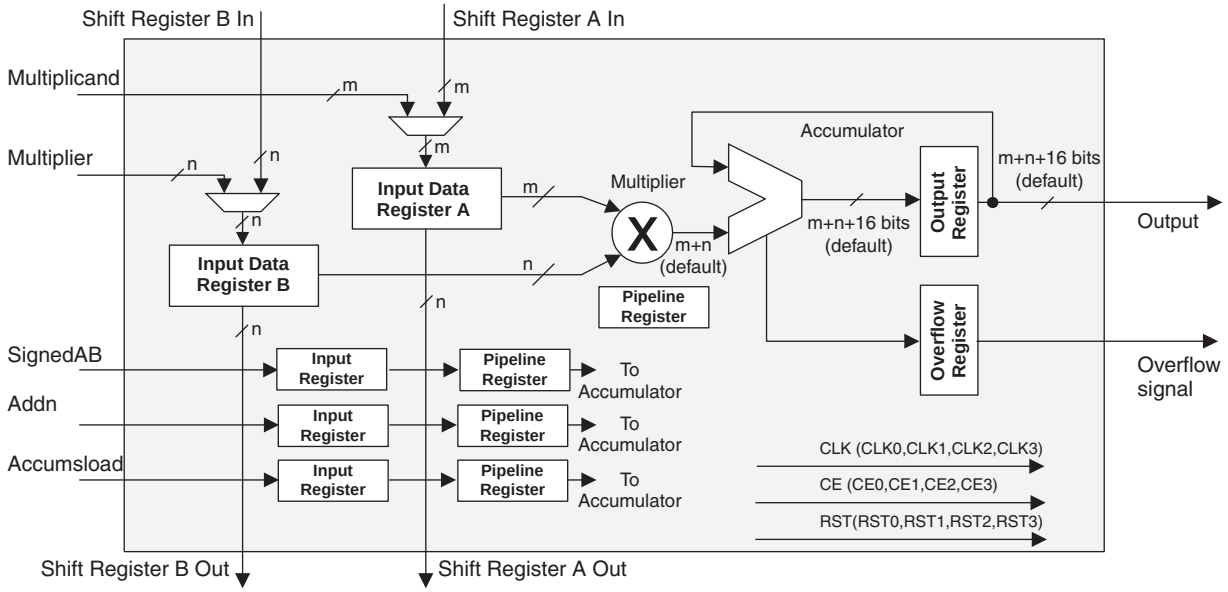
The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

Figure 2-20. MAC sysDSP Element



MULTADD sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-21 shows the MULTADD sysDSP element.

Figure 2-21. MULTADD

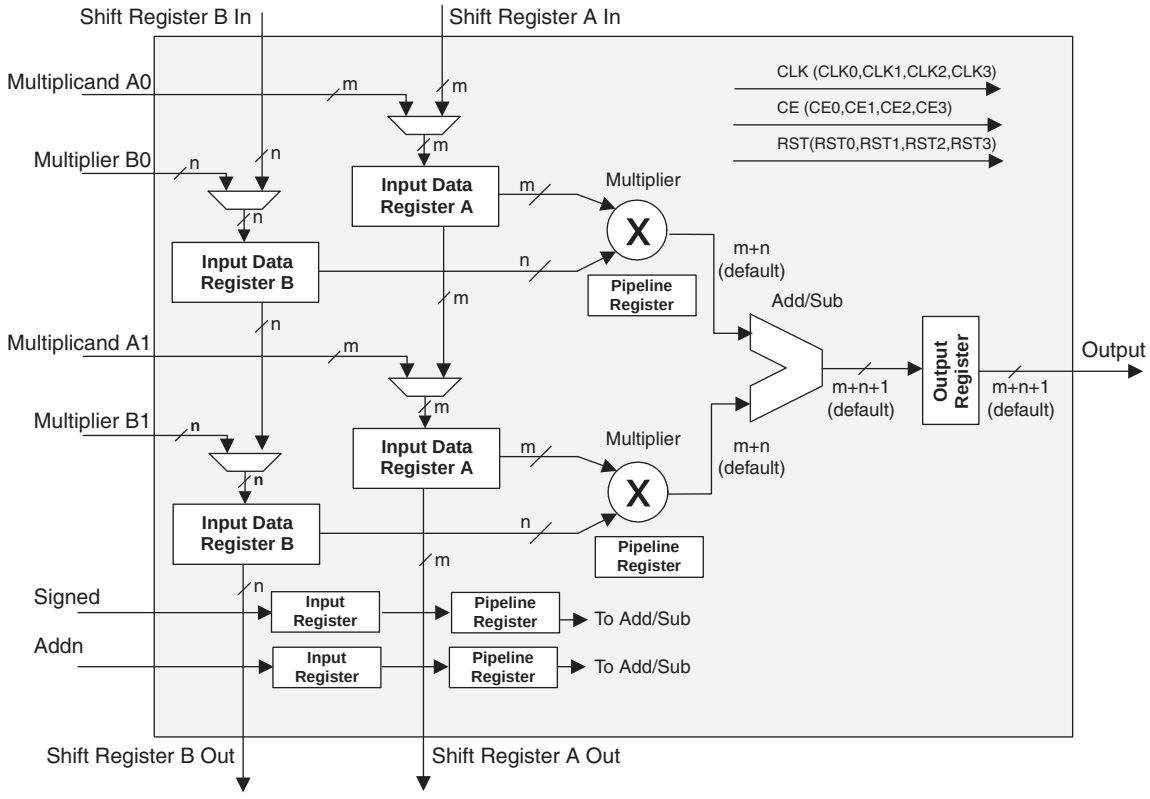
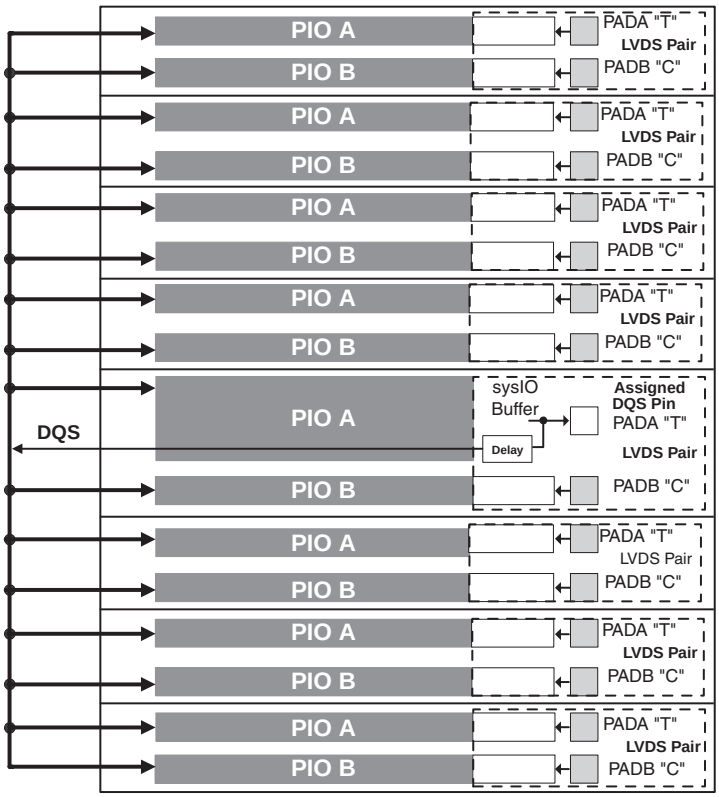


Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block FFs.
CLK0, CLK1	Control from the core	System clocks for input and output blocks.
LSR	Control from the core	Local Set/Reset.
GSRN	Control from routing	Global Set/Reset (active low).
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs.
DQS	Input to PIO	DQS signal from logic (routing) to PIO.
INDD	Input to the core	Unregistered data input to core.
INFF	Input to the core	Registered input on positive edge of the clock (CLK0).
IPOS0, IPOS1	Input to the core	DDRX registered inputs to the core.
ONEG0	Control from the core	Output signals from the core for SDR and DDR operation.
OPOS0,	Control from the core	Output signals from the core for DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation.
TD	Tristate control from the core	Tristate signal from the core used in SDR operation.
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block.

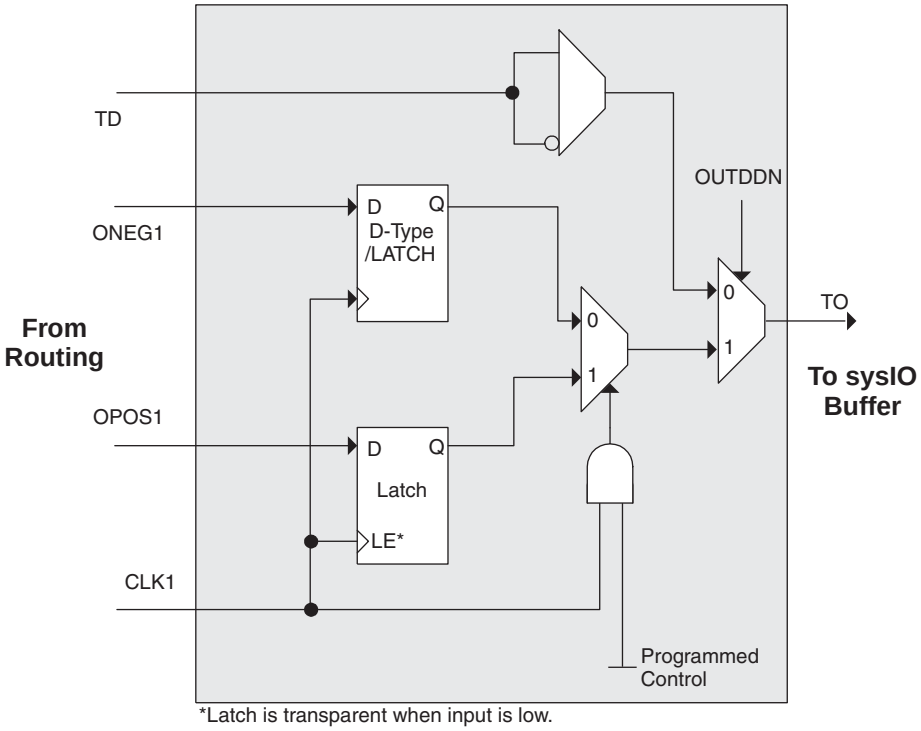
Figure 2-25. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Figure 2-31. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeEC devices provide this capability. In addition to these registers, the LatticeEC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-32 and 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-33. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-32. DQS Local Bus.

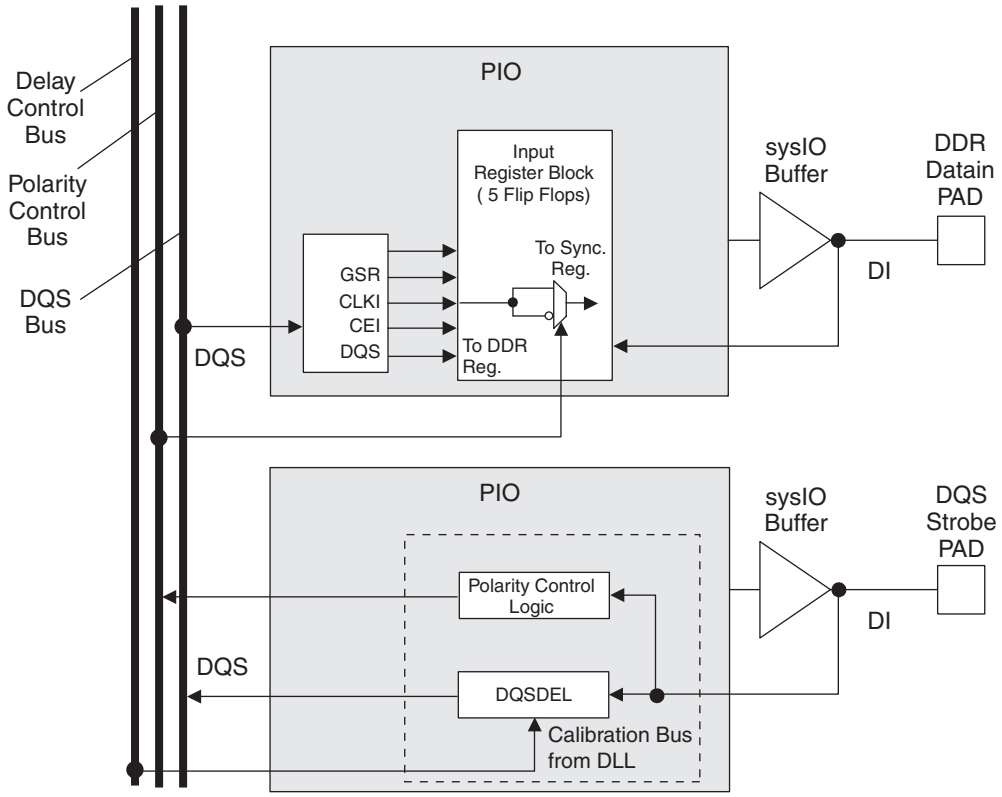
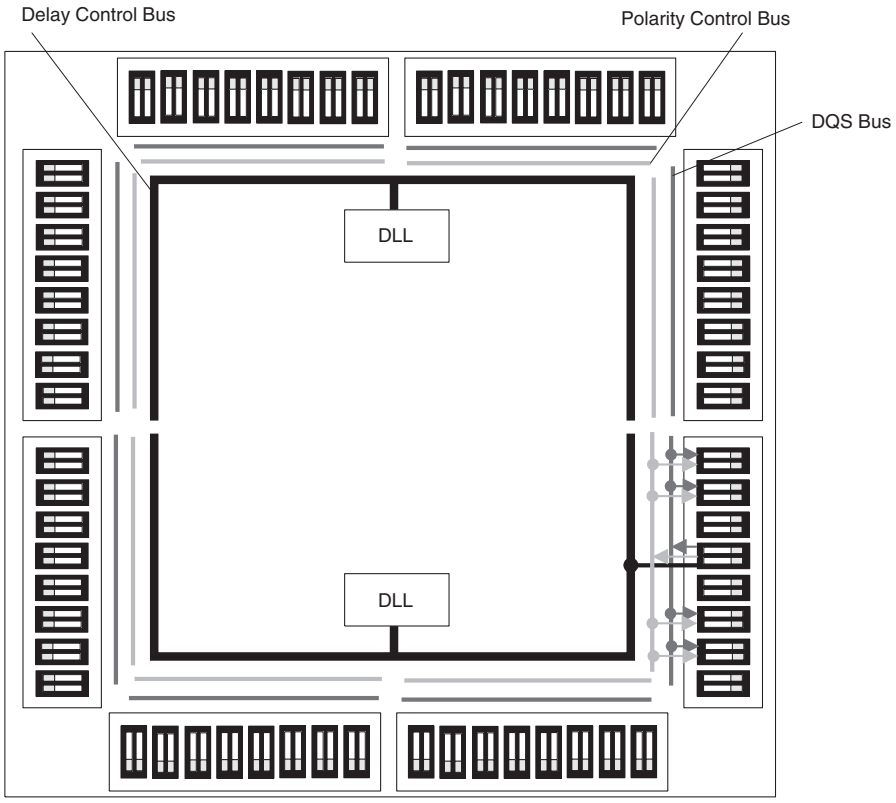


Figure 2-33. DLL Calibration Bus and DQS/DQS Transition Distribution



LVPECL

The LatticeECP/EC devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

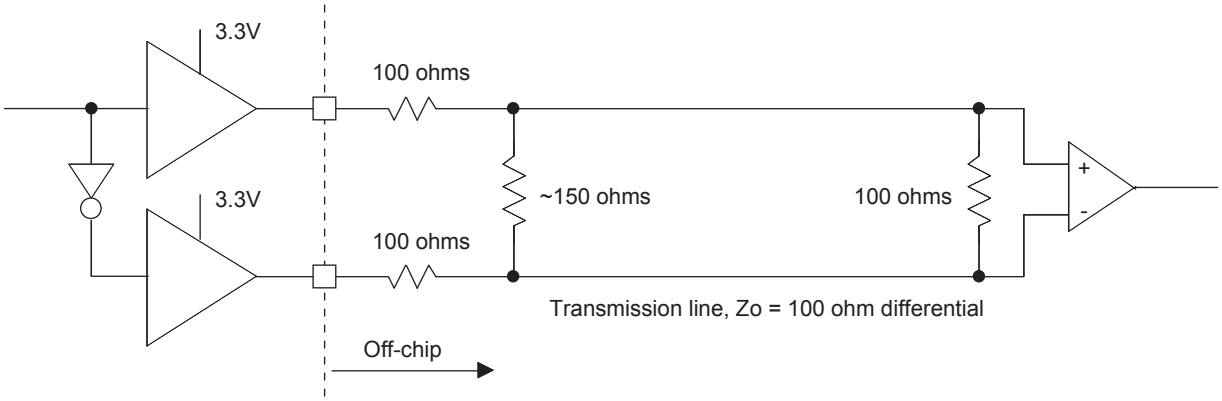


Table 3-3. LVPECL DC Conditions[1]

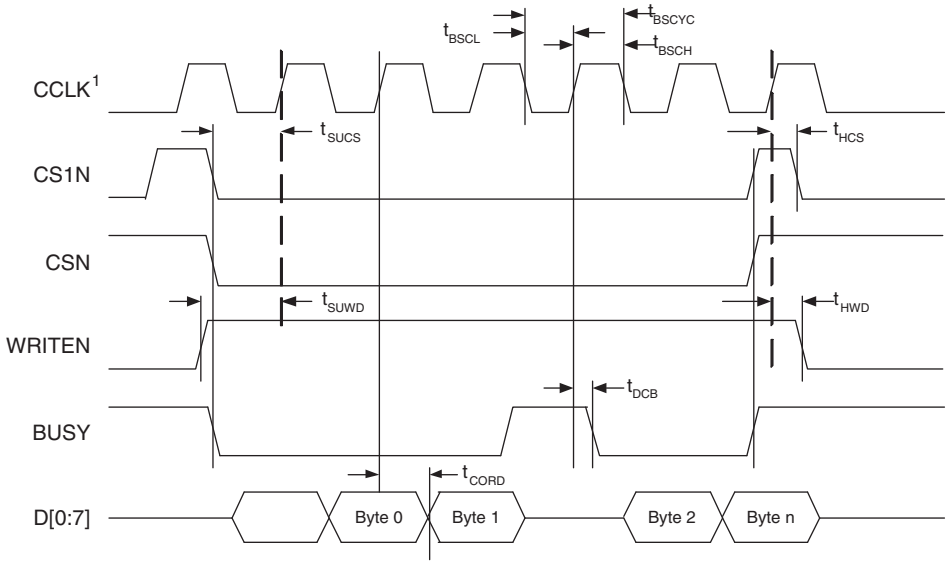
Over Recommended Operating Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	100	ohm
R_P	Driver parallel resistor	150	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	85.7	ohm
I_{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

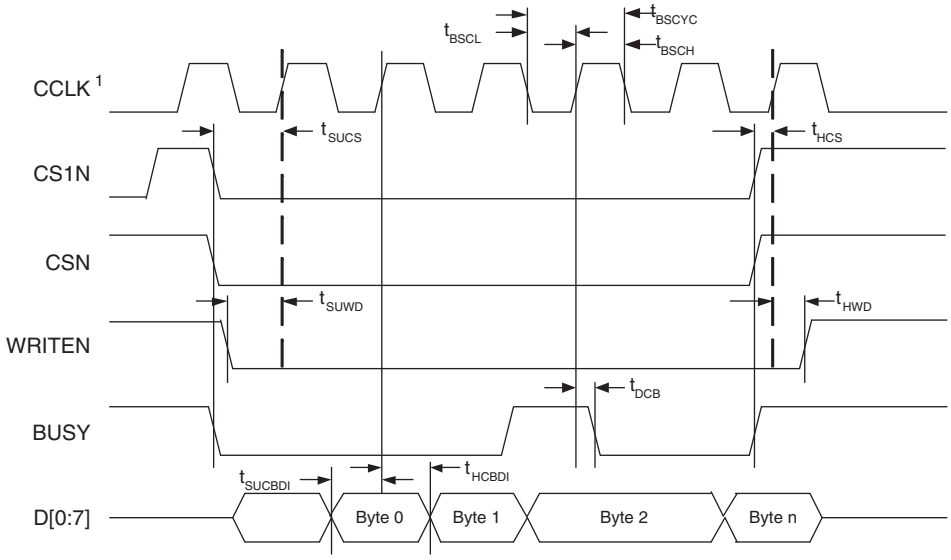
For further information about LVPECL, BLVDS and other differential interfaces please see the list of technical information at the end of this data sheet.

Figure 3-12. sysCONFIG Parallel Port Read Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-13. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ

Notes:
1. “n” is a Row/Column PIC number
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

LFEC1, LFEC3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	LFEC1				LFEC3			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
82	PT11B	1	C	VREF2_1	PT19B	1	C	VREF2_1
83	PT11A	1	T	VREF1_1	PT19A	1	T	VREF1_1
84	PT10B	1	C		PT18B	1	C	
85	PT10A	1	T		PT18A	1	T	
86	VCCIO1	1			VCCIO1	1		
87	VCCAUX	-			VCCAUX	-		
88	PT9B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
89	GND0	0			GND0	0		
90	PT9A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
91	PT8B	0	C	VREF1_0	PT16B	0	C	VREF1_0
92	PT8A	0	T	VREF2_0	PT16A	0	T	VREF2_0
93	PT7B	0			PT15B	0		
94	PT6B	0	C		PT14B	0	C	
95	PT6A	0	T	TDQS6	PT14A	0	T	TDQS14
96	PT4B	0	C		PT12B	0	C	
97	PT4A	0	T		PT12A	0	T	
98	PT2B	0	C		PT10B	0	C	
99	PT2A	0	T		PT10A	0	T	
100	VCCIO0	0			VCCIO0	0		

*Double bonded to the pin.

LFEC1, LFEC3, LFECP/EC6 Logic Signal Connections: 144 TQFP

Pin Number	LFEC1				LFEC3				LFECP6/EC6			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1	VCCIO7	7			VCCIO7	7			VCCIO7	7		
2	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
3	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
4	PL3A	7	T		PL7A	7	T		PL7A	7	T	
5	PL3B	7	C		PL7B	7	C		PL7B	7	C	
6	PL4A	7	T		PL8A	7	T		PL8A	7	T	
7	PL4B	7	C		PL8B	7	C		PL8B	7	C	
8	PL5A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0	PL9A	7	T	PCLKT7_0
9	PL5B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0	PL9B	7	C	PCLKC7_0
10	XRES	6			XRES	6			XRES	6		
11	NC	-			NC	-			VCC	-		
12	NC	-			NC	-			GND	-		
13	VCC	-			VCC	-			VCC	-		
14	TCK	6			TCK	6			TCK	6		
15	GND	-			GND	-			GND	-		
16	TDI	6			TDI	6			TDI	6		
17	TMS	6			TMS	6			TMS	6		
18	TDO	6			TDO	6			TDO	6		
19	VCCJ	6			VCCJ	6			VCCJ	6		
20	PL7A	6	T	LLM0_PLLT_IN_A	PL11A	6	T	LLM0_PLLT_IN_A	PL20A	6	T	LLM0_PLLT_IN_A
21	PL7B	6	C	LLM0_PLLC_IN_A	PL11B	6	C	LLM0_PLLC_IN_A	PL20B	6	C	LLM0_PLLC_IN_A
22	PL8A	6	T	LLM0_PLLT_FB_A	PL12A	6	T	LLM0_PLLT_FB_A	PL21A	6	T	LLM0_PLLT_FB_A
23	PL8B	6	C	LLM0_PLLC_FB_A	PL12B	6	C	LLM0_PLLC_FB_A	PL21B	6	C	LLM0_PLLC_FB_A
24	VCCIO6	6			VCCIO6	6			VCCIO6	6		
25	PL9A	6	T		PL13A	6	T		PL22A	6	T	
26	PL9B	6	C		PL13B	6	C		PL22B	6	C	
27	PL10A	6	T		PL14A	6	T		PL23A	6	T	
28	GND6	6			GND6	6			GND6	6		
29	PL10B	6	C		PL14B	6	C		PL23B	6	C	
30	PL11A	6	T	LDQS11	PL15A	6	T	LDQS15	PL24A	6	T	LDQS24
31	PL11B	6	C		PL15B	6	C		PL24B	6	C	
32	PL12A	6	T		PL16A	6	T		PL25A	6	T	
33	PL12B	6	C		PL16B	6	C		PL25B	6	C	
34	PL14A	6	T	VREF1_6	PL18A	6	T	VREF1_6	PL27A	6	T	VREF1_6
35	PL14B	6	C	VREF2_6	PL18B	6	C	VREF2_6	PL27B	6	C	VREF2_6
36	VCCIO6	6			VCCIO6	6			VCCIO6	6		
37*	GND5 GND6	-			GND5 GND6	-			GND5 GND6	-		
38	VCCIO5	5			VCCIO5	5			VCCIO5	5		
39	PB2A	5	T		PB10A	5	T		PB10A	5	T	
40	PB2B	5	C		PB10B	5	C		PB10B	5	C	
41	PB3A	5	T		PB11A	5	T		PB11A	5	T	
42	PB3B	5	C		PB11B	5	C		PB11B	5	C	
43	PB5B	5			PB13B	5			PB13B	5		
44	VCCIO5	5			VCCIO5	5			VCCIO5	5		
45	PB6A	5	T	BDQS6	PB14A	5	T	BDQS14	PB14A	5	T	BDQS14
46	PB6B	5	C		PB14B	5	C		PB14B	5	C	
47	PB7A	5	T		PB15A	5	T		PB15A	5	T	
48	PB7B	5	C		PB15B	5	C		PB15B	5	C	
49	PB8A	5	T	VREF2_5	PB16A	5	T	VREF2_5	PB16A	5	T	VREF2_5

LFECP/EC6, LFECP/EC10 Logic Signal Connections: 208 PQFP

Pin Number	LFECP6/LFEC6				LFECP10/LFEC10			
	Pin Function	Bank	LVDS	Dual Function	Pin Function	Bank	LVDS	Dual Function
1*	GND0 GND7	-			GND0 GND7	-		
2	VCCIO7	7			VCCIO7	7		
3	PL2A	7	T	VREF2_7	PL2A	7	T	VREF2_7
4	PL2B	7	C	VREF1_7	PL2B	7	C	VREF1_7
5	NC	-			VCC	-		
6	NC	-			GND	-		
7	PL3B	7			PL12B	7		
8	PL4A	7	T		PL13A	7	T	
9	PL4B	7	C		PL13B	7	C	
10	PL5A	7	T		PL14A	7	T	
11	PL5B	7	C		PL14B	7	C	
12	PL6A	7	T	LDQS6	PL15A	7	T	LDQS15
13	VCCIO7	7			VCCIO7	7		
14	PL6B	7	C		PL15B	7	C	
15	PL7A	7	T		PL16A	7	T	
16	PL7B	7	C		PL16B	7	C	
17	PL8A	7	T		PL17A	7	T	
18	GND7	7			GND7	7		
19	PL8B	7	C		PL17B	7	C	
20	PL9A	7	T	PCLKT7_0	PL18A	7	T	PCLKT7_0
21	PL9B	7	C	PCLKC7_0	PL18B	7	C	PCLKC7_0
22	VCCAUX	-			VCCAUX	-		
23	XRES	6			XRES	6		
24	VCC	-			VCC	-		
25	GND	-			GND	-		
26	VCC	-			VCC	-		
27	TCK	6			TCK	6		
28	GND	-			GND	-		
29	TDI	6			TDI	6		
30	TMS	6			TMS	6		
31	TDO	6			TDO	6		
32	VCCJ	6			VCCJ	6		
33	PL20A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A
34	PL20B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A
35	PL21A	6	T	LLM0_PLLT_FB_A	PL30A	6	T	LLM0_PLLT_FB_A
36	PL21B	6	C	LLM0_PLLC_FB_A	PL30B	6	C	LLM0_PLLC_FB_A
37	VCCIO6	6			VCCIO6	6		
38	PL22A	6	T		PL31A	6	T	
39	PL22B	6	C		PL31B	6	C	
40	PL23A	6	T		PL32A	6	T	
41	GND6	6			GND6	6		
42	PL23B	6	C		PL32B	6	C	

LFEC3 and LFECP/EC6 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFEC3				LFECP6/LFEC6			
	Ball Function	Bank	LVDS	Dual Function	Ball Function	Bank	LVDS	Dual Function
C16	PR4B	2	C		PR4B	2	C	
B16	PR4A	2	T		PR4A	2	T	
C15	PR3B	2	C		PR3B	2	C	
C14	PR3A	2	T		PR3A	2	T	
D14	PR2B	2	C	VREF1_2	PR2B	2	C	VREF1_2
D13	PR2A	2	T	VREF2_2	PR2A	2	T	VREF2_2
GND	GND2	2			GND2	2		
GND	GND1	1			GND1	1		
-	-	-			GND1	1		
B13	NC	-			PT26B	1	C	
C13	NC	-			PT26A	1	T	
C12	PT25B	1	C		PT25B	1	C	
-	-	-			GND1	1		
D12	PT25A	1	T		PT25A	1	T	
A15	PT24B	1	C		PT24B	1	C	
B14	PT24A	1	T		PT24A	1	T	
D11	PT23B	1	C		PT23B	1	C	
C11	PT23A	1	T		PT23A	1	T	
E10	PT22B	1	C		PT22B	1	C	
E11	PT22A	1	T	TDQS22	PT22A	1	T	TDQS22
A14	PT21B	1	C		PT21B	1	C	
GND	GND1	1			GND1	1		
A13	PT21A	1	T		PT21A	1	T	
D10	PT20B	1	C		PT20B	1	C	
C10	PT20A	1	T		PT20A	1	T	
A12	PT19B	1	C	VREF2_1	PT19B	1	C	VREF2_1
B12	PT19A	1	T	VREF1_1	PT19A	1	T	VREF1_1
A11	PT18B	1	C		PT18B	1	C	
B11	PT18A	1	T		PT18A	1	T	
A10	PT17B	0	C	PCLKC0_0	PT17B	0	C	PCLKC0_0
GND	GND0	0			GND0	0		
B10	PT17A	0	T	PCLKT0_0	PT17A	0	T	PCLKT0_0
C9	PT16B	0	C	VREF1_0	PT16B	0	C	VREF1_0
B9	PT16A	0	T	VREF2_0	PT16A	0	T	VREF2_0
E9	PT15B	0	C		PT15B	0	C	
D9	PT15A	0	T		PT15A	0	T	
D8	PT14B	0	C		PT14B	0	C	
C8	PT14A	0	T	TDQS14	PT14A	0	T	TDQS14
A9	PT13B	0	C		PT13B	0	C	
GND	GND0	0			GND0	0		
A8	PT13A	0	T		PT13A	0	T	
B8	PT12B	0	C		PT12B	0	C	
B7	PT12A	0	T		PT12A	0	T	

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
N22	PR17A	3	T		N22	PR26A	3	T		N22	PR30A	3	T	
N19	PR16B	3	C		N19	PR25B	3	C		N19	PR29B	3	C	
N18	PR16A	3	T		N18	PR25A	3	T		N18	PR29A	3	T	
M21	PR15B	3	C		M21	PR24B	3	C		M21	PR28B	3	C	
L20	PR15A	3	T	RDQS15	L20	PR24A	3	T	RDQS24	L20	PR28A	3	T	RDQS28
L21	PR14B	3	C		L21	PR23B	3	C		L21	PR27B	3	C	
GND	GND3	3			GND	GND3	3			GND	GND3	3		
M20	PR14A	3	T		M20	PR23A	3	T		M20	PR27A	3	T	
M18	PR13B	3	C		M18	PR22B	3	C		M18	PR26B	3	C	
M19	PR13A	3	T		M19	PR22A	3	T		M19	PR26A	3	T	
M22	PR12B	3	C		M22	PR21B	3	C		M22	PR25B	3	C	
L22	PR12A	3	T		L22	PR21A	3	T		L22	PR25A	3	T	
K22	PR11B	3	C		K22	PR20B	3	C		K22	PR24B	3	C	
K21	PR11A	3	T		K21	PR20A	3	T		K21	PR24A	3	T	
J22	PR9B	2	C	PCLKC2_0	J22	PR18B	2	C	PCLKC2_0	J22	PR22B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2			GND	GND2	2		
J21	PR9A	2	T	PCLKT2_0	J21	PR18A	2	T	PCLKT2_0	J21	PR22A	2	T	PCLKT2_0
H22	PR8B	2	C		H22	PR17B	2	C		H22	PR21B	2	C	
H21	PR8A	2	T		H21	PR17A	2	T		H21	PR21A	2	T	
L19	PR7B	2	C		L19	PR16B	2	C		L19	PR20B	2	C	
L18	PR7A	2	T		L18	PR16A	2	T		L18	PR20A	2	T	
K20	PR6B	2	C		K20	PR15B	2	C		K20	PR19B	2	C	
J20	PR6A	2	T	RDQS6	J20	PR15A	2	T	RDQS15	J20	PR19A	2	T	RDQS19
K19	PR5B	2	C		K19	PR14B	2	C		K19	PR18B	2	C	
GND	-	-			GND	GND2	2			GND	GND2	2		
K18	PR5A	2	T		K18	PR14A	2	T		K18	PR18A	2	T	
G22	PR4B	2	C		G22	PR13B	2	C		G22	PR17B	2	C	
F22	PR4A	2	T		F22	PR13A	2	T		F22	PR17A	2	T	
F21	PR3B	2	C		F21	PR12B	2	C		F21	PR16B	2	C	
E22	PR3A	2	T		E22	PR12A	2	T		E22	PR16A	2	T	
E21	NC	-			E21	PR11B	2	C		E21	PR15B	2	C	
D22	NC	-			D22	PR11A	2	T		D22	PR15A	2	T	
G21	NC	-			G21	NC	-			G21	PR14B	2	C	
G20	NC	-			G20	NC	-			GND	GND2	2		
GND	-	-			-	-	-			G20	PR14A	2	T	
J18	NC	-			J18	NC	-			J18	PR13B	2	C	
H19	NC	-			H19	NC	-			H19	PR13A	2	T	
J19	NC	-			J19	NC	-			J19	PR12B	2	C	
H20	NC	-			H20	NC	-			H20	PR12A	2	T	
H17	NC	-			H17	NC	-			H17	PR11B	2	C	
H18	NC	-			H18	NC	-			H18	PR11A	2	T	
D21	NC	-			D21	PR9B	2	C	RUM0_PLLC_FB_A	D21	PR9B	2	C	RUM0_PLLC_FB_A
GND	-	-			GND	GND2	2			GND	GND2	2		
C22	NC	-			C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR9A	2	T	RUM0_PLLT_FB_A
G19	NC	-			G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR8B	2	C	RUM0_PLLC_IN_A
G18	NC	-			G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR8A	2	T	RUM0_PLLT_IN_A
F20	NC	-			F20	PR7B	2	C		F20	PR7B	2	C	
F19	NC	-			F19	PR7A	2	T		F19	PR7A	2	T	
E20	NC	-			E20	PR6B	2	C		E20	PR6B	2	C	
D20	NC	-			D20	PR6A	2	T	RDQS6	D20	PR6A	2	T	RDQS6

LFECP/EC6, LFECP/EC10, LFECP/EC15 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP6/LFEC6					LFECP10/LFEC10					LFECP/LFEC15				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C21	NC	-			C21	PR5B	2	C		C21	PR5B	2	C	
C20	NC	-			C20	PR5A	2	T		C20	PR5A	2	T	
F18	NC	-			F18	PR4B	2	C		F18	PR4B	2	C	
E18	NC	-			E18	PR4A	2	T		E18	PR4A	2	T	
B22	NC	-			B22	PR3B	2	C		B22	PR3B	2	C	
B21	NC	-			B21	PR3A	2	T		B21	PR3A	2	T	
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1			GND	GND1	1		
G17	NC	-			G17	NC	-			G17	PT49B	1	C	
F17	NC	-			F17	NC	-			F17	PT49A	1	T	
D18	NC	-			D18	NC	-			D18	PT48B	1	C	
C18	NC	-			C18	NC	-			C18	PT48A	1	T	
C19	NC	-			C19	NC	-			C19	PT47B	1	C	
B20	NC	-			B20	NC	-			B20	PT47A	1	T	
D17	NC	-			D17	NC	-			D17	PT46B	1	C	
C16	NC	-			C16	NC	-			C16	PT46A	1	T	TDQS46
B19	NC	-			B19	NC	-			B19	PT45B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A20	NC	-			A20	NC	-			A20	PT45A	1	T	
E17	NC	-			E17	NC	-			E17	PT44B	1	C	
C17	NC	-			C17	NC	-			C17	PT44A	1	T	
F16	NC	-			F16	NC	-			F16	PT43B	1	C	
E16	NC	-			E16	NC	-			E16	PT43A	1	T	
F15	NC	-			F15	NC	-			F15	PT42B	1	C	
D16	NC	-			D16	NC	-			D16	PT42A	1	T	
B18	PT33B	1	C		B18	PT41B	1	C		B18	PT41B	1	C	
GND	-	-			GND	-	-			GND	GND1	1		
A19	PT33A	1	T		A19	PT41A	1	T		A19	PT41A	1	T	
B17	PT32B	1	C		B17	PT40B	1	C		B17	PT40B	1	C	
A18	PT32A	1	T		A18	PT40A	1	T		A18	PT40A	1	T	
B16	PT31B	1	C		B16	PT39B	1	C		B16	PT39B	1	C	
A17	PT31A	1	T		A17	PT39A	1	T		A17	PT39A	1	T	
B15	PT30B	1	C		B15	PT38B	1	C		B15	PT38B	1	C	
A16	PT30A	1	T	TDQS30	A16	PT38A	1	T	TDQS38	A16	PT38A	1	T	TDQS38
A15	PT29B	1	C		A15	PT37B	1	C		A15	PT37B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
A14	PT29A	1	T		A14	PT37A	1	T		A14	PT37A	1	T	
G14	PT28B	1	C		G14	PT36B	1	C		G14	PT36B	1	C	
E15	PT28A	1	T		E15	PT36A	1	T		E15	PT36A	1	T	
D15	PT27B	1	C		D15	PT35B	1	C		D15	PT35B	1	C	
C15	PT27A	1	T		C15	PT35A	1	T		C15	PT35A	1	T	
C14	PT26B	1	C		C14	PT34B	1	C		C14	PT34B	1	C	
B14	PT26A	1	T		B14	PT34A	1	T		B14	PT34A	1	T	
A13	PT25B	1	C		A13	PT33B	1	C		A13	PT33B	1	C	
GND	GND1	1			GND	GND1	1			GND	GND1	1		
B13	PT25A	1	T		B13	PT33A	1	T		B13	PT33A	1	T	
E14	PT24B	1	C		E14	PT32B	1	C		E14	PT32B	1	C	
C13	PT24A	1	T		C13	PT32A	1	T		C13	PT32A	1	T	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
W20	PR48B	3	C	VREF2_3	W20	PR68B	3	C	VREF2_3
Y20	PR48A	3	T	VREF1_3	Y20	PR68A	3	T	VREF1_3
GND	-	-			GND	GND3	3		
GND	-	-			GND	GND3	3		
AA21	PR47B	3	C		AA21	PR59B	3	C	
AB21	PR47A	3	T		AB21	PR59A	3	T	
W19	PR46B	3	C		W19	PR58B	3	C	
V19	PR46A	3	T		V19	PR58A	3	T	
Y21	PR45B	3	C		Y21	PR57B	3	C	
AA22	PR45A	3	T	RDQS45	AA22	PR57A	3	T	RDQS57
V20	PR44B	3	C	RLM0_PLLC_IN_A	V20	PR56B	3	C	RLM0_PLLC_IN_A
GND	GND3	3			GND	GND3	3		
U20	PR44A	3	T	RLM0_PLLT_IN_A	U20	PR56A	3	T	RLM0_PLLT_IN_A
W21	PR43B	3	C	RLM0_PLLC_FB_A	W21	PR55B	3	C	RLM0_PLLC_FB_A
Y22	PR43A	3	T	RLM0_PLLT_FB_A	Y22	PR55A	3	T	RLM0_PLLT_FB_A
V21	PR42B	3	C	DI/CSSPIN	V21	PR54B	3	C	DI/CSSPIN
W22	PR42A	3	T	DOUT/CSON	W22	PR54A	3	T	DOUT/CSON
U21	PR41B	3	C	BUSY/SISPI	U21	PR53B	3	C	BUSY/SISPI
V22	PR41A	3	T	D7/SPID0	V22	PR53A	3	T	D7/SPID0
T19	CFG2	3			T19	CFG2	3		
U19	CFG1	3			U19	CFG1	3		
U18	CFG0	3			U18	CFG0	3		
V18	PROGRAMN	3			V18	PROGRAMN	3		
T20	CCLK	3			T20	CCLK	3		
T21	INITN	3			T21	INITN	3		
R20	DONE	3			R20	DONE	3		
GND	GND3	3			GND	GND3	3		
T18	PR37B	3	C		T18	PR49B	3	C	
R17	PR37A	3	T		R17	PR49A	3	T	
R19	PR36B	3	C		R19	PR48B	3	C	
R18	PR36A	3	T	RDQS36	R18	PR48A	3	T	RDQS48
U22	PR35B	3	C		U22	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T22	PR35A	3	T		T22	PR47A	3	T	
R21	PR34B	3	C		R21	PR46B	3	C	
R22	PR34A	3	T		R22	PR46A	3	T	
P20	PR33B	3	C		P20	PR45B	3	C	
N20	PR33A	3	T		N20	PR45A	3	T	
P19	PR32B	3	C		P19	PR44B	3	C	
P18	PR32A	3	T		P18	PR44A	3	T	
P21	PR31B	3	C		P21	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P22	PR31A	3	T		P22	PR43A	3	T	
N21	PR30B	3	C		N21	PR42B	3	C	

LFECP/EC20 and LFECP/EC33 Logic Signal Connections: 484 fpBGA (Cont.)

LFECP20/LFEC20					LFECP/LFEC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
C22	PR9A	2	T	RUM0_PLLT_FB_A	C22	PR17A	2	T	RUM0_PLLT_FB_A
G19	PR8B	2	C	RUM0_PLLC_IN_A	G19	PR16B	2	C	RUM0_PLLC_IN_A
G18	PR8A	2	T	RUM0_PLLT_IN_A	G18	PR16A	2	T	RUM0_PLLT_IN_A
F20	PR7B	2	C		F20	PR15B	2	C	
F19	PR7A	2	T		F19	PR15A	2	T	
E20	PR6B	2	C		E20	PR14B	2	C	
D20	PR6A	2	T	RDQS6	D20	PR14A	2	T	RDQS14
C21	PR5B	2	C		C21	PR13B	2	C	
GND	-	-			GND	GND2	2		
C20	PR5A	2	T		C20	PR13A	2	T	
F18	PR4B	2	C		F18	PR12B	2	C	
E18	PR4A	2	T		E18	PR12A	2	T	
B22	PR3B	2	C		B22	PR11B	2	C	
B21	PR3A	2	T		B21	PR11A	2	T	
GND	-	-			GND	GND2	2		
E19	PR2B	2	C	VREF1_2	E19	PR2B	2	C	VREF1_2
D19	PR2A	2	T	VREF2_2	D19	PR2A	2	T	VREF2_2
GND	GND2	2			GND	GND2	2		
GND	GND1	1			GND	GND1	1		
GND	-	-			GND	GND1	1		
G17	PT57B	1	C		G17	PT57B	1	C	
GND	-	-			GND	GND1	1		
F17	PT57A	1	T		F17	PT57A	1	T	
D18	PT56B	1	C		D18	PT56B	1	C	
C18	PT56A	1	T		C18	PT56A	1	T	
C19	PT55B	1	C		C19	PT55B	1	C	
B20	PT55A	1	T		B20	PT55A	1	T	
D17	PT54B	1	C		D17	PT54B	1	C	
C16	PT54A	1	T	TDQS54	C16	PT54A	1	T	TDQS54
B19	PT53B	1	C		B19	PT53B	1	C	
GND	GND1	1			GND	GND1	1		
A20	PT53A	1	T		A20	PT53A	1	T	
E17	PT52B	1	C		E17	PT52B	1	C	
C17	PT52A	1	T		C17	PT52A	1	T	
F16	PT51B	1	C		F16	PT51B	1	C	
E16	PT51A	1	T		E16	PT51A	1	T	
F15	PT50B	1	C		F15	PT50B	1	C	
D16	PT50A	1	T		D16	PT50A	1	T	
B18	PT49B	1	C		B18	PT49B	1	C	
GND	GND1	1			GND	GND1	1		
A19	PT49A	1	T		A19	PT49A	1	T	
B17	PT48B	1	C		B17	PT48B	1	C	
A18	PT48A	1	T		A18	PT48A	1	T	
B16	PT47B	1	C		B16	PT47B	1	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
Y6	NC	-			Y6	PL62A	6	T	
W7	NC	-			W7	PL62B	6	C	
AA4	NC	-			AA4	PL63A	6	T	
AB3	NC	-			AB3	PL63B	6	C	
AC2	NC	-			AC2	PL64A	6	T	
-	-	-			GND	GND6	6		
AC3	NC	-			AC3	PL64B	6	C	
AA5	NC	-			AA5	PL65A	6	T	LDQS65
AB5	NC	-			AB5	PL65B	6	C	
AD3	NC	-			AD3	PL66A	6	T	
AD2	NC	-			AD2	PL66B	6	C	
AE1	NC	-			AE1	PL67A	6	T	
AD1	NC	-			AD1	PL67B	6	C	
AB4	PL48A	6	T	VREF1_6	AB4	PL68A	6	T	VREF1_6
AC4	PL48B	6	C	VREF2_6	AC4	PL68B	6	C	VREF2_6
GND	GND6	6			GND	GND6	6		
GND	GND5	5			GND	GND5	5		
AB6	PB2A	5	T		AB6	PB2A	5	T	
AA6	PB2B	5	C		AA6	PB2B	5	C	
AC7	PB3A	5	T		AC7	PB3A	5	T	
Y8	PB3B	5	C		Y8	PB3B	5	C	
AB7	PB4A	5	T		AB7	PB4A	5	T	
AA7	PB4B	5	C		AA7	PB4B	5	C	
AC6	PB5A	5	T		AC6	PB5A	5	T	
AC5	PB5B	5	C		AC5	PB5B	5	C	
AB8	PB6A	5	T	BDQS6	AB8	PB6A	5	T	BDQS6
AC8	PB6B	5	C		AC8	PB6B	5	C	
AE2	PB7A	5	T		AE2	PB7A	5	T	
AA8	PB7B	5	C		AA8	PB7B	5	C	
AF2	PB8A	5	T		AF2	PB8A	5	T	
Y9	PB8B	5	C		Y9	PB8B	5	C	
AD5	PB9A	5	T		AD5	PB9A	5	T	
GND	GND5	5			GND	GND5	5		
AD4	PB9B	5	C		AD4	PB9B	5	C	
AD8	PB10A	5	T		AD8	PB10A	5	T	
AC9	PB10B	5	C		AC9	PB10B	5	C	
AE3	PB11A	5	T		AE3	PB11A	5	T	
AB9	PB11B	5	C		AB9	PB11B	5	C	
AF3	PB12A	5	T		AF3	PB12A	5	T	
AD9	PB12B	5	C		AD9	PB12B	5	C	
AE4	PB13A	5	T		AE4	PB13A	5	T	
GND	GND5	5			GND	GND5	5		

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
AC13	PB32B	5	C	VREF1_5	AC13	PB32B	5	C	VREF1_5
AF14	PB33A	5	T	PCLKT5_0	AF14	PB33A	5	T	PCLKT5_0
GND	GND5	5			GND	GND5	5		
AE14	PB33B	5	C	PCLKC5_0	AE14	PB33B	5	C	PCLKC5_0
AA13	PB34A	4	T	WRITEN	AA13	PB34A	4	T	WRITEN
AB13	PB34B	4	C	CS1N	AB13	PB34B	4	C	CS1N
AD14	PB35A	4	T	VREF1_4	AD14	PB35A	4	T	VREF1_4
AA14	PB35B	4	C	CSN	AA14	PB35B	4	C	CSN
AC14	PB36A	4	T	VREF2_4	AC14	PB36A	4	T	VREF2_4
AB14	PB36B	4	C	D0/SPID7	AB14	PB36B	4	C	D0/SPID7
AF15	PB37A	4	T	D2/SPID5	AF15	PB37A	4	T	D2/SPID5
GND	GND4	4			GND	GND4	4		
AE15	PB37B	4	C	D1/SPID6	AE15	PB37B	4	C	D1/SPID6
AD15	PB38A	4	T	BDQS38	AD15	PB38A	4	T	BDQS38
AC15	PB38B	4	C	D3/SPID4	AC15	PB38B	4	C	D3/SPID4
AF16	PB39A	4	T		AF16	PB39A	4	T	
Y14	PB39B	4	C	D4/SPID3	Y14	PB39B	4	C	D4/SPID3
AE16	PB40A	4	T		AE16	PB40A	4	T	
AB15	PB40B	4	C	D5/SPID2	AB15	PB40B	4	C	D5/SPID2
AF17	PB41A	4	T		AF17	PB41A	4	T	
GND	GND4	4			GND	GND4	4		
AE17	PB41B	4	C	D6/SPID1	AE17	PB41B	4	C	D6/SPID1
Y15	PB42A	4	T		Y15	PB42A	4	T	
AA15	PB42B	4	C		AA15	PB42B	4	C	
AD17	PB43A	4	T		AD17	PB43A	4	T	
Y16	PB43B	4	C		Y16	PB43B	4	C	
AD18	PB44A	4	T		AD18	PB44A	4	T	
AC16	PB44B	4	C		AC16	PB44B	4	C	
AE18	PB45A	4	T		AE18	PB45A	4	T	
GND	GND4	4			GND	GND4	4		
AF18	PB45B	4	C		AF18	PB45B	4	C	
AD16	PB46A	4	T	BDQS46	AD16	PB46A	4	T	BDQS46
AB16	PB46B	4	C		AB16	PB46B	4	C	
AF19	PB47A	4	T		AF19	PB47A	4	T	
AA16	PB47B	4	C		AA16	PB47B	4	C	
AA17	PB48A	4	T		AA17	PB48A	4	T	
Y17	PB48B	4	C		Y17	PB48B	4	C	
AF21	PB49A	4	T		AF21	PB49A	4	T	
GND	GND4	4			GND	GND4	4		
AF20	PB49B	4	C		AF20	PB49B	4	C	
AE21	PB50A	4	T		AE21	PB50A	4	T	
AC17	PB50B	4	C		AC17	PB50B	4	C	

LFECP/EC20, LFECP/EC33 Logic Signal Connections: 672 fpBGA (Cont.)

LFEC20/LFECP20					LFECP/EC33				
Ball Number	Ball Function	Bank	LVDS	Dual Function	Ball Number	Ball Function	Bank	LVDS	Dual Function
U21	PR36B	3	C		U21	PR48B	3	C	
T21	PR36A	3	T	RDQS36	T21	PR48A	3	T	RDQS48
T25	PR35B	3	C		T25	PR47B	3	C	
GND	GND3	3			GND	GND3	3		
T26	PR35A	3	T		T26	PR47A	3	T	
T22	PR34B	3	C		T22	PR46B	3	C	
T23	PR34A	3	T		T23	PR46A	3	T	
T24	PR33B	3	C		T24	PR45B	3	C	
R23	PR33A	3	T		R23	PR45A	3	T	
R25	PR32B	3	C		R25	PR44B	3	C	
R24	PR32A	3	T		R24	PR44A	3	T	
R26	PR31B	3	C		R26	PR43B	3	C	
GND	GND3	3			GND	GND3	3		
P26	PR31A	3	T		P26	PR43A	3	T	
R21	PR30B	3	C		R21	PR42B	3	C	
R22	PR30A	3	T		R22	PR42A	3	T	
P25	PR29B	3	C		P25	PR41B	3	C	
P24	PR29A	3	T		P24	PR41A	3	T	
P23	PR28B	3	C		P23	PR40B	3	C	
P22	PR28A	3	T	RDQS28	P22	PR40A	3	T	RDQS40
N26	PR27B	3	C		N26	PR39B	3	C	
GND	GND3	3			GND	GND3	3		
M26	PR27A	3	T		M26	PR39A	3	T	
N21	PR26B	3	C		N21	PR38B	3	C	
P21	PR26A	3	T		P21	PR38A	3	T	
N23	PR25B	3	C		N23	PR37B	3	C	
N22	PR25A	3	T		N22	PR37A	3	T	
N25	PR24B	3	C		N25	PR36B	3	C	
N24	PR24A	3	T		N24	PR36A	3	T	
L26	PR22B	2	C	PCLKC2_0	L26	PR34B	2	C	PCLKC2_0
GND	GND2	2			GND	GND2	2		
K26	PR22A	2	T	PCLKT2_0	K26	PR34A	2	T	PCLKT2_0
M22	PR21B	2	C		M22	PR33B	2	C	
M23	PR21A	2	T		M23	PR33A	2	T	
M25	PR20B	2	C		M25	PR32B	2	C	
M24	PR20A	2	T		M24	PR32A	2	T	
M21	PR19B	2	C		M21	PR31B	2	C	
L21	PR19A	2	T	RDQS19	L21	PR31A	2	T	RDQS31
L22	PR18B	2	C		L22	PR30B	2	C	
GND	GND2	2			GND	GND2	2		
L23	PR18A	2	T		L23	PR30A	2	T	
L25	PR17B	2	C		L25	PR29B	2	C	

Date	Version	Section	Change Summary
December 2004	01.4	Architecture	Updated Hot Socketing Recommended Power Up Sequence section.
		Pinout Information	Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Pin Information
			Added LFEC1, LFEC3, LFECP/EC10, LFECP/EC15 to Power Supply and NC Connections
			Added LFEC1 and LFEC3 100 TQFP Pinout
			Added LFEC1 and LFEC3 144 TQFP Pinout
			Added LFEC1, LFEC3 and LFECP/EC10 208 PQFP Pinout
			Added LFEC3, LFECP/EC10 and LFECP/EC15 256 fpBGA Pinout
			Added LFECP/EC10 and LFECP/EC15 484 fpBGA Pinout
		Ordering Information	Added Lead-Free Package Designators
			Added Lead-Free Ordering Part Numbers
		Supplemental Information	Updated list of technical notes.
April 2005	01.5	Architecture	EBR memory support section has been updated with clarification.
			Updated sysIO buffer pair section.
		DC & Switching Characteristics	Hot Socketing Specification has been updated.
			DC Electrical Characteristics table (I_{IL}, I_{IH}) has been updated.
			Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			External Switching Characteristics section has been updated.
			Removed t_{RSTW} spec. from PLL Parameter table.
			t_{RST} specifications have been updated.
			sysCONFIG Port Timing Specifications (t_{BSCL}, t_{IODISS}, t_{PRGMRJ}) have been updated.
		Pinout Information	Added LFECP/EC33 Pinout Information
			Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
			484-fpBGA logic connection has been updated (Ball # J6, J17, P6 and P17 for ECP/EC33 are now called VCCPLL).
			672-fpBGA logic connection has been updated (Ball # K19, L8, U19, U8 for ECP/EC33 are now called VCCPLL).
May 2005	01.6	Introduction	ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.
		Architecture	Table 2-10 has been updated (ECP/EC33 EBR SRAM Bits and Blocks have been updated to 498K and 54 respectively.)
			Recommended Power Up Sequence section has been removed.
		DC & Switching Characteristics	Supply Current (Standby) table has been updated.
			Initialization Supply Current table has been updated.
			Vos test condition has been updated to (VOP+VOM)/2.
			Register-to-Register performance table has been updated (rev. G 0.27).
			External switching characteristics have been updated (rev. G 0.27).
			Internal timing parameters have been updated (rev. G 0.27).
			Timing adders have been updated (rev. G 0.27).
			sysCONFIG port timing specifications have been updated.
		Pinout Information	Pin Information Summary table has been updated.
			Power Supply and NC Connection table has been updated.
		Ordering Information	OPN list has been updated.